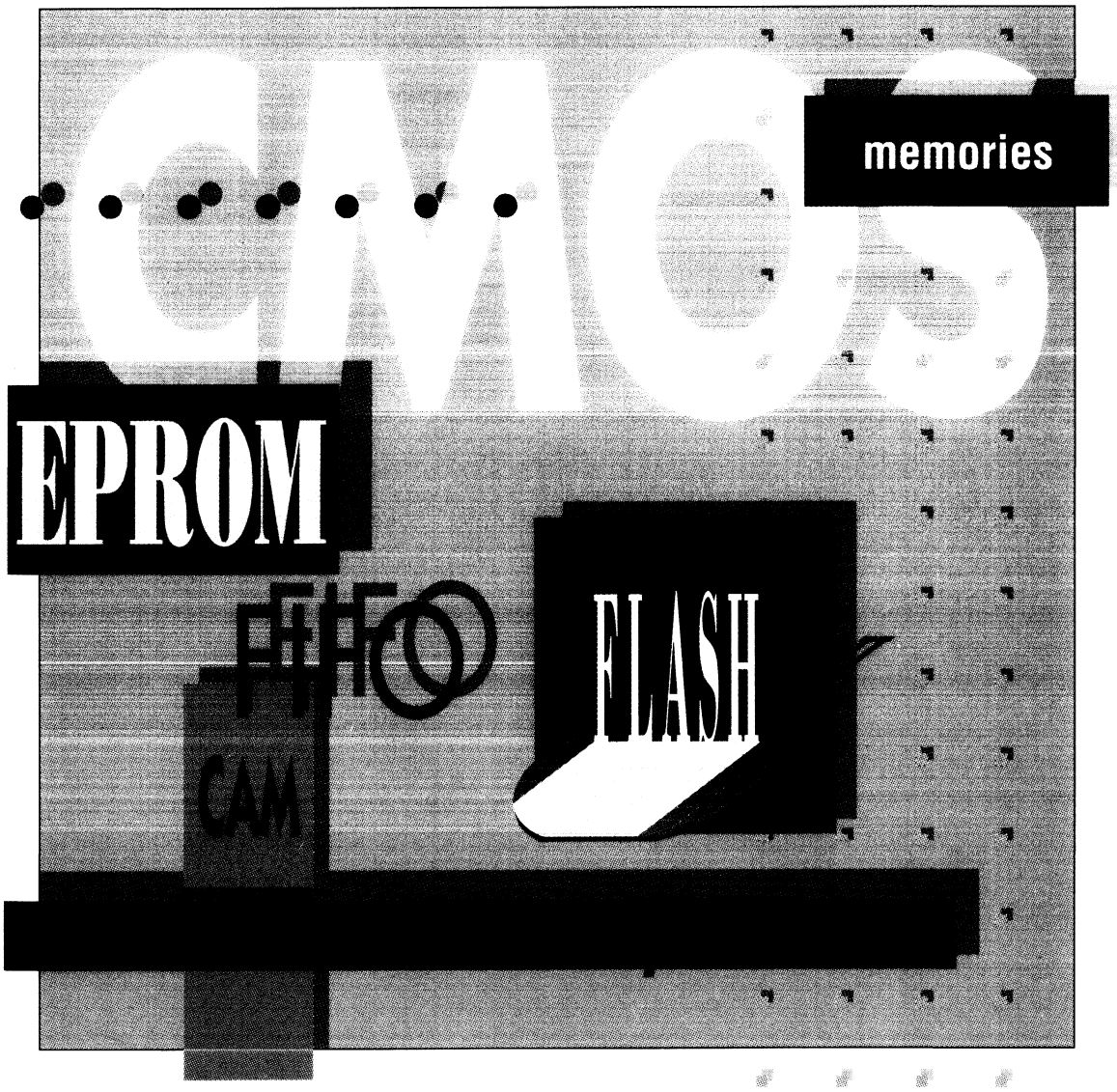
CMOS Memory Products

1991 Data Book/Handbook

Advanced
Micro
Devices



Advanced Micro Devices

CMOS Memory Products

1991 Data Book/Handbook

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Advanced Micro Devices continues to focus on memory product development. Over the past few years our entire product line has been converted to the industry's most advanced CMOS process. Our technology leadership is evidenced by the world's fastest EPROMs in every density as well as the industry's smallest die sizes.

Our EPROM product portfolio is the broadest available. CMOS EPROMs in production today span all densities from 64K through 4 Megabits with 8 Megabit parts on the way. A choice of speeds ranging from 35 ns to 250 ns allows you to maximize the performance of systems based on todays highest speed processors. We also offer several application specific memories; a 1 Megabit burst mode EPROM, an ultra low power 512K EPROM, a Content Addressable Memory (CAM) and a full line of First-in First-out memories (FIFOs).

The progression of technology now allows us to offer Flash memories for cost effective solutions that require in-system reprogrammability. Densities from 256K through 2 Megabit are now in production. They are 100% compatible with today's 12 V Flash standard.

AMD has become the non-volatile memory leader. We hope to be your supplier of choice.

Rich Forte
Vice President
High Performance Memories

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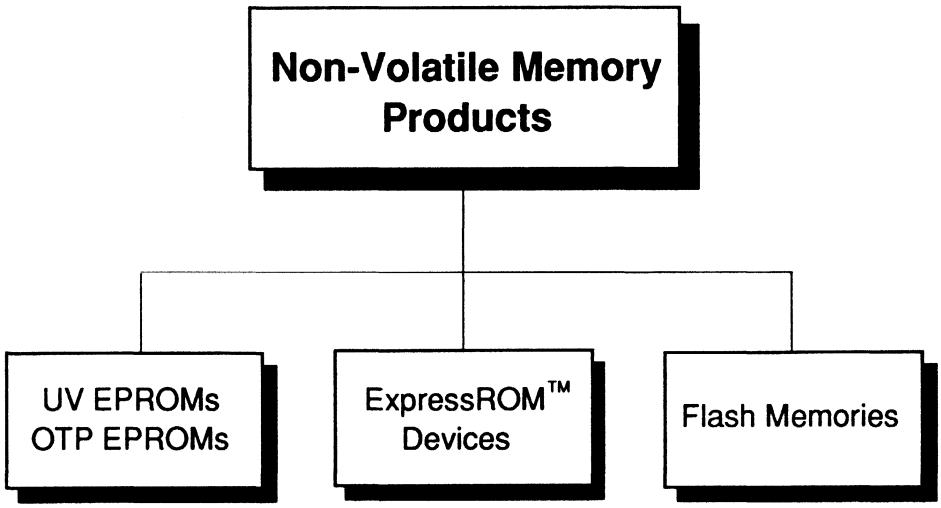


Introduction

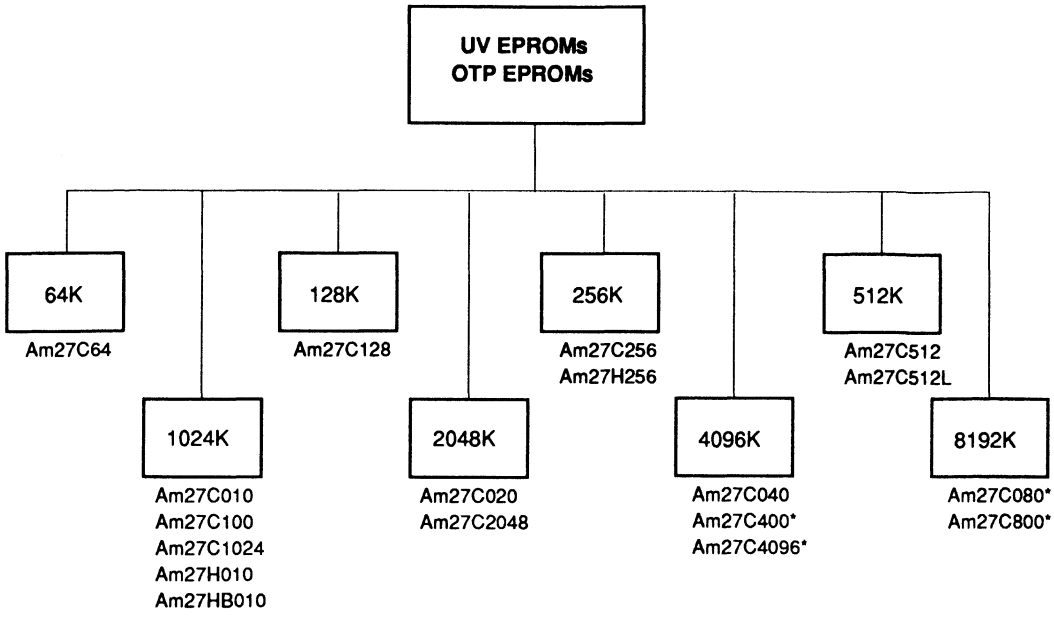
The Non-Volatile Memory Division manufactures a broad range of high performance memory products. These products include traditional windowed EPROMs, plastic OTP EPROMs, Express-ROM devices, and Flash Memories. They offer the system designer an extensive choice of economical alternatives for program storage.

NVD's EPROM offerings are manufactured with a state-of-the-art CMOS process yielding access times as fast as 35 ns. Products in production range from 64K to 4 megabits. Also available are low-power and high-speed burst devices. EPROMs are available in both windowed-ceramic and One-Time-Programmable (OTP) plastic packages.

A new concept from AMD is the ExpressROM device. These are quick-turn ROMs produced from EPROM wafers. Lead times of these devices are typically half that of ROMs.

Flash memories will be the designer's choice for reprogrammable non-volatile memory in the 90's. AMD has introduced Flash devices with densities ranging from 256K to 2 megabits.

AMD is committed to leadership in high-performance CMOS non-volatile memories. These products offer industry-leading speeds and densities that will contribute to the competitive advantages of your design.



UV EPROMs & OTP EPROMs

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count (DIP/PLCC)	Supply Voltage
Am27C64-55	8K x 8	55	C	D, L	28/32	5 V ± 5%
Am27C64-75	8K x 8	70	C	D, L	28/32	5 V ± 5%
Am27C64-70	8K x 8	70	C	D, L	28/32	5 V ± 10%
Am27C64-95[3]	8K x 8	90	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C64-90	8K x 8	90	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C64-125[3]	8K x 8	120	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C64-120	8K x 8	120	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C64-155[3]	8K x 8	150	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C64-150	8K x 8	150	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C64-205[3]	8K x 8	200	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C64-200	8K x 8	200	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C64-255	8K x 8	250	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C64-250[3]	8K x 8	250	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C64-305[3]	8K x 8	300	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C64-300[3]	8K x 8	300	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C128-55	16K x 8	55	C	D, L	28/32	5 V ± 5%
Am27C128-75	16K x 8	70	C	D, L	28/32	5 V ± 5%
Am27C128-70	16K x 8	70	C	D, L	28/32	5 V ± 10%
Am27C128-95[3]	16K x 8	90	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C128-90	16K x 8	90	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C128-125[3]	16K x 8	120	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C128-120	16K x 8	120	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C128-155[3]	16K x 8	150	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C128-150	16K x 8	150	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C128-205[3]	16K x 8	200	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C128-200	16K x 8	200	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C128-255	16K x 8	250	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C128-250[3]	16K x 8	250	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C128-305[3]	16K x 8	300	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C128-300[3]	16K x 8	300	C, I, E, M	D, L, P, J	28/32	5 V ± 10%

* Contact the local AMD sales office for the availability of this device.

Notes: see page 1-10

UV EPROMs & OTP EPROMs *(Cont.)*

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count (DIP/PLCC)	Supply Voltage
Am27H256-35	32K x 8	35	C	D, L	28/32	5 V ± 10%
Am27H256-35V05	32K x 8	35	C	D, L	28/32	5 V ± 5%
Am27H256-45	32K x 8	45	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27H256-55	32K x 8	55	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27H256-70	32K x 8	70	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C256-55	32K x 8	55	C	D, L	28/32	5 V ± 5%
Am27C256-75	32K x 8	70	C	D, L	28/32	5 V ± 5%
Am27C256-70	32K x 8	70	C	D, L	28/32	5 V ± 10%
Am27C256-95[3]	32K x 8	90	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C256-90	32K x 8	90	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C256-105[3]	32K x 8	100	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C256-100	32K x 8	100	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C256-125[3]	32K x 8	120	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C256-120	32K x 8	120	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C256-155[3]	32K x 8	150	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C256-150	32K x 8	150	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C256-175[3]	32K x 8	170	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C256-170[3]	32K x 8	170	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C256-205[3]	32K x 8	200	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C256-200	32K x 8	200	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C256-255	32K x 8	250	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C256-250[3]	32K x 8	250	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C256-305[3]	32K x 8	300	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C256-300[3]	32K x 8	300	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C512-75	64K x 8	70	C	D, L	28/32	5 V ± 5%
Am27C512-95	64K x 8	90	C, I	D, L	28/32	5 V ± 5%
Am27C512-90	64K x 8	90	C, I, E, M	D, L	28/32	5 V ± 10%
Am27C512-125	64K x 8	120	C, I	D, L	28/32	5 V ± 5%
Am27C512-120	64K x 8	120	C, I, E, M	D, L	28/32	5 V ± 10%
Am27C512-155[3]	64K x 8	150	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C512-150	64K x 8	150	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C512-175[3]	64K x 8	170	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C512-170[3]	64K x 8	170	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C512-205[3]	64K x 8	200	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C512-200	64K x 8	200	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C512-255	64K x 8	250	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C512-250[3]	64K x 8	250	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C512-305[3]	64K x 8	300	C, I	D, L, P, J	28/32	5 V ± 5%
Am27C512-300[3]	64K x 8	300	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C512L-75	64K x 8	70	C	D, L	28/32	5 V ± 5%
Am27C512L-95	64K x 8	90	C, I	D, L	28/32	5 V ± 5%
Am27C512L-90	64K x 8	90	C, I	D, L	28/32	5 V ± 10%
Am27C512L-120	64K x 8	120	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C512L-125	64K x 8	120	C, I	D, L	28/32	5 V ± 5%
Am27C512L-150	64K x 8	150	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C512L-200	64K x 8	200	C, I, E, M	D, L, P, J	28/32	5 V ± 10%
Am27C512L-250	64K x 8	250	M	D, L	28/32	5 V ± 10%
Am27C512L-255	64K x 8	250	C, I	D, L, P, J	28/32	5 V ± 5%
Am27H010-45	128K x 8	45	C	D, L	32/32	5 V ± 10%
Am27H010-45V05	128K x 8	45	C	D, L	32/32	5 V ± 5%
Am27H010-55	128K x 8	55	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27H010-70	128K x 8	70	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27H010-90	128K x 8	90	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27H010-90V05	128K x 8	90	C, I, E, M	D, L, P, J	32/32	5 V ± 5%
Am27C010-95[4]	128K x 8	90	C	D, L	32/32	5 V ± 5%
Am27C010-90[4]	128K x 8	90	C	D, L	32/32	5 V ± 10%
Am27C010-105	128K x 8	100	C	D, L	32/32	5 V ± 5%

* Contact the local AMD sales office for the availability of this device.

Notes: see page 1-10

UV EPROMs & OTP EPROMs *(Cont.)*

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count (DIP/PLCC)	Supply Voltage
Am27C010-125	128K x 8	120	C, I	D, L	32/32	5 V ± 5%
Am27C010-120	128K x 8	120	C, I	D, L	32/32	5 V ± 10%
Am27C010-155[3]	128K x 8	150	C, I	D, L	32/32	5 V ± 5%
Am27C010-150	128K x 8	150	C, I, E, M	D, L	32/32	5 V ± 10%
Am27C010-175[3]	128K x 8	170	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C010-170[3]	128K x 8	170	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C010-205[3]	128K x 8	200	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C010-200	128K x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C010-255	128K x 8	250	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C010-250[3]	128K x 8	250	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C010-305[3]	128K x 8	300	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C010-300[3]	128K x 8	300	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27HB010-50V05	128K x 8	50	C, I	D, L	32/32	5 V ± 5%
Am27HB010-50	128K x 8	50	C, I	D, L	32/32	5 V ± 10%
Am27HB010-60V05	128K x 8	60	C	P, J	32/32	5 V ± 5%
Am27HB010-60	128K x 8	60	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27HB010-90	128K x 8	90	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C100-105	128K x 8	100	C	D, L	32/32	5 V ± 5%
Am27C100-125	128K x 8	120	C, I	D, L	32/32	5 V ± 5%
Am27C100-120	128K x 8	120	C, I	D, L	32/32	5 V ± 10%
Am27C100-155[3]	128K x 8	150	C, I	D, L	32/32	5 V ± 5%
Am27C100-150	128K x 8	150	C, I, E, M	D, L	32/32	5 V ± 10%
Am27C100-175[3]	128K x 8	170	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C100-170[3]	128K x 8	170	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C100-205[3]	128K x 8	200	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C100-200	128K x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C100-255	128K x 8	250	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C100-250[3]	128K x 8	250	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C100-305[3]	128K x 8	300	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C100-300[3]	128K x 8	300	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C1024-105	64K x 16	100	C, I	D, L	40/44	5 V ± 5%
Am27C1024-125	64K x 16	120	C, I	D, L	40/44	5 V ± 5%
Am27C1024-120	64K x 16	120	C, I, E, M	D, L	40/44	5 V ± 10%
Am27C1024-155[3]	64K x 16	150	C, I	D, L	40/44	5 V ± 5%
Am27C1024-150	64K x 16	150	C, I, E, M	D, L	40/44	5 V ± 10%
Am27C1024-175[3]	64K x 16	170	C, I	D, L	40/44	5 V ± 5%
Am27C1024-170[3]	64K x 16	170	C, I, E, M	D, L	40/44	5 V ± 10%
Am27C1024-205[3]	64K x 16	200	C, I	D, L, P, J	40/44	5 V ± 5%
Am27C1024-200	64K x 16	200	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C1024-255	64K x 16	250	C, I	D, L, P, J	40/44	5 V ± 5%
Am27C1024-250[3]	64K x 16	250	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C1024-305[3]	64K x 16	300	C, I	D, L, P, J	40/44	5 V ± 5%
Am27C1024-300[3]	64K x 16	300	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C020-105	256K x 8	100	C	D, L	32/32	5 V ± 5%
Am27C020-125	256K x 8	120	C, I	D, L	32/32	5 V ± 5%
Am27C020-120	256K x 8	120	C, I	D, L	32/32	5 V ± 10%
Am27C020-155[3]	256K x 8	150	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C020-150	256K x 8	150	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C020-175[3]	256K x 8	170	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C020-170[3]	256K x 8	170	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C020-205[3]	256K x 8	200	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C020-200	256K x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C020-255	256K x 8	250	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C020-250[3]	256K x 8	250	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C020-305[3]	256K x 8	300	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C020-300[3]	256K x 8	300	C, I, E, M	D, L, P, J	32/32	5 V ± 10%

* Contact the local AMD sales office for the availability of this device.

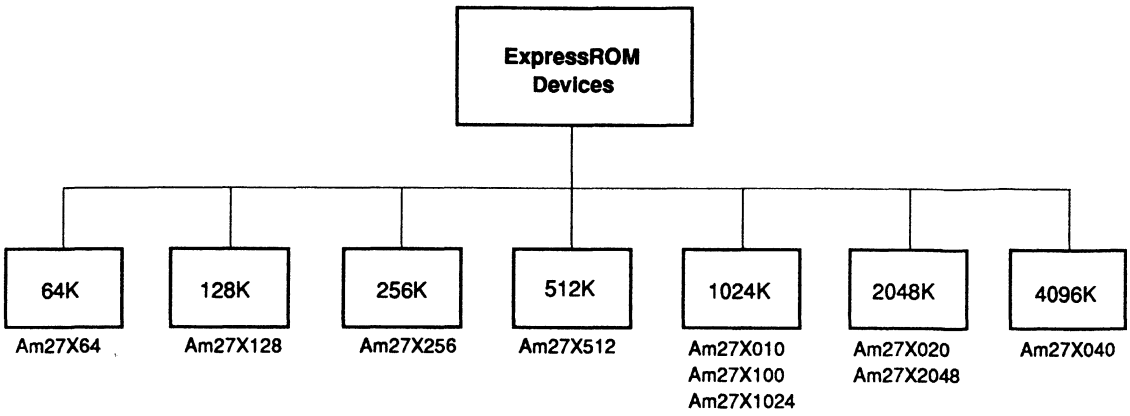
Notes: see page 1-10

UV EPROMs & OTP EPROMs *(Cont.)*

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count (DIP/PLCC)	Supply Voltage
Am27C2048-105*	128K x 16	100	C	D, L	40/44	5 V ± 5%
Am27C2048-125	128K x 16	120	C, I	D, L	40/44	5 V ± 5%
Am27C2048-120*	128K x 16	120	C, I	D, L	40/44	5 V ± 10%
Am27C2048-155[3]	128K x 16	150	C, I	D, L, P, J	40/44	5 V ± 5%
Am27C2048-150	128K x 16	150	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C2048-175[3]	128K x 16	170	C, I	D, L, P, J	40/44	5 V ± 5%
Am27C2048-170[3]	128K x 16	170	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C2048-205[3]	128K x 16	200	C, I	D, L, P, J	40/44	5 V ± 5%
Am27C2048-200	128K x 16	200	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C2048-255	128K x 16	250	C, I	D, L, P, J	40/44	5 V ± 5%
Am27C2048-250[3]	128K x 16	250	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C2048-305[3]	128K x 16	300	C, I	D, L, P, J	40/44	5 V ± 5%
Am27C2048-300[3]	128K x 16	300	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C040-95*	512K x 8	90	C	D, L	32/32	5 V ± 5%
Am27C040-90*	512K x 8	90	C	D, L	32/32	5 V ± 10%
Am27C040-125*	512K x 8	120	C, I	D, L	32/32	5 V ± 5%
Am27C040-120*	512K x 8	120	C, I	D, L	32/32	5 V ± 10%
Am27C040-155	512K x 8	150	C, I	D, L	32/32	5 V ± 5%
Am27C040-150	512K x 8	150	C, I, E, M	D, L	32/32	5 V ± 10%
Am27C040-205[3]	512K x 8	200	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C040-200	512K x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C040-255	512K x 8	250	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C040-250[3]	512K x 8	250	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C400-95*	512K x 8/256K x 16	90	C, I	D	40	5 V ± 5%
Am27C400-90*	512K x 8/256K x 16	90	C, I	D	40	5 V ± 10%
Am27C400-125*	512K x 8/256K x 16	120	C, I	D	40	5 V ± 5%
Am27C400-120*	512K x 8/256K x 16	120	C, I	D	40	5 V ± 10%
Am27C400-155*	512K x 8/256K x 16	150	C, I	D	40	5 V ± 5%
Am27C400-150*	512K x 8/256K x 16	150	C, I	D	40	5 V ± 10%
Am27C400-200*	512K x 8/256K x 16	200	C, I	D	40	5 V ± 10%
Am27C400-255*	512K x 8/256K x 16	250	C, I	D	40	5 V ± 5%
Am27C4096-95*	256K x 16	90	C	D, L	40/44	5 V ± 5%
Am27C4096-90*	256K x 16	90	C	D, L	40/44	5 V ± 10%
Am27C4096-105*	256K x 16	100	C, I	D, L	40/44	5 V ± 5%
Am27C4096-100*	256K x 16	100	C, I	D, L	40/44	5 V ± 10%
Am27C4096-125*	256K x 16	120	C, I	P, J	40/44	5 V ± 5%
Am27C4096-120*	256K x 16	120	C, I, E, M	D, L	40/44	5 V ± 10%
Am27C4096-150*	256K x 16	150	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C4096-200*	256K x 16	200	C, I, E, M	D, L, P, J	40/44	5 V ± 10%
Am27C4096-255*	256K x 16	250	C, I	D, L, P, J	40/44	5 V ± 5%
Am27C4096-250*	256K x 16	250	M	D, L, P, J	40/44	5 V ± 10%
Am27C080-125*	1 Megabit x 8	120	C, I	D, L	32/32	5 V ± 5%
Am27C080-120*	1 Megabit x 8	120	C, I	D, L	32/32	5 V ± 10%
Am27C080-150*	1 Megabit x 8	150	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C080-200*	1 Megabit x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am27C080-250*	1 Megabit x 8	250	M	D, L	32/32	5 V ± 10%
Am27C080-255*	1 Megabit x 8	250	C, I	D, L, P, J	32/32	5 V ± 5%
Am27C800-125*	1 Megabit x 8/512K x 16	120	C, I	D, L	42/44	5 V ± 5%
Am27C800-120*	1 Megabit x 8/512K x 16	120	C, I	D, L	42/44	5 V ± 10%
Am27C800-150*	1 Megabit x 8/512K x 16	150	C, I, E, M	D, L, P, J	42/44	5 V ± 10%
Am27C800-200*	1 Megabit x 8/512K x 16	200	C, I, E, M	D, L, P, J	42/44	5 V ± 10%
Am27C800-250*	1 Megabit x 8/512K x 16	250	M	D, L	42/44	5 V ± 10%
Am27C800-255*	1 Megabit x 8/512K x 16	250	C, I	D, L, P, J	42/44	5 V ± 5%

* Contact the local AMD sales office for the availability of this device.

Notes: see page 1-10



ExpressROM Devices

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count (PDIP/PLCC)	Supply Voltage
Am27X64-105	8K x 8	100	C, I	P, J	28/32	5 V ± 5%
Am27X64-125	8K x 8	120	C, I	P, J	28/32	5 V ± 5%
Am27X64-120	8K x 8	120	C, I	P, J	28/32	5 V ± 10%
Am27X64-155[3]	8K x 8	150	C, I	P, J	28/32	5 V ± 5%
Am27X64-150	8K x 8	150	C, I	P, J	28/32	5 V ± 10%
Am27X64-175[3]	8K x 8	170	C, I	P, J	28/32	5 V ± 5%
Am27X64-170[3]	8K x 8	170	C, I	P, J	28/32	5 V ± 10%
Am27X64-205[3]	8K x 8	200	C, I	P, J	28/32	5 V ± 5%
Am27X64-200	8K x 8	200	C, I	P, J	28/32	5 V ± 10%
Am27X64-255[3]	8K x 8	250	C, I	P, J	28/32	5 V ± 5%
Am27X64-250	8K x 8	250	C, I	P, J	28/32	5 V ± 10%
Am27X128-105	16K x 8	100	C, I	P, J	28/32	5 V ± 5%
Am27X128-125	16K x 8	120	C, I	P, J	28/32	5 V ± 5%
Am27X128-120	16K x 8	120	C, I	P, J	28/32	5 V ± 10%
Am27X128-155[3]	16K x 8	150	C, I	P, J	28/32	5 V ± 5%
Am27X128-150	16K x 8	150	C, I	P, J	28/32	5 V ± 10%
Am27X128-175[3]	16K x 8	170	C, I	P, J	28/32	5 V ± 5%
Am27X128-170[3]	16K x 8	170	C, I	P, J	28/32	5 V ± 10%
Am27X128-205[3]	16K x 8	200	C, I	P, J	28/32	5 V ± 5%
Am27X128-200	16K x 8	200	C, I	P, J	28/32	5 V ± 10%
Am27X128-255[3]	16K x 8	250	C, I	P, J	28/32	5 V ± 5%
Am27X128-250	16K x 8	250	C, I	P, J	28/32	5 V ± 10%
Am27X256-105	32K x 8	100	C, I	P, J	28/32	5 V ± 5%
Am27X256-125	32K x 8	120	C, I	P, J	28/32	5 V ± 5%
Am27X256-120	32K x 8	120	C, I	P, J	28/32	5 V ± 10%
Am27X256-155[3]	32K x 8	150	C, I	P, J	28/32	5 V ± 5%
Am27X256-150	32K x 8	150	C, I	P, J	28/32	5 V ± 10%
Am27X256-175[3]	32K x 8	170	C, I	P, J	28/32	5 V ± 5%
Am27X256-170[3]	32K x 8	170	C, I	P, J	28/32	5 V ± 10%
Am27X256-205[3]	32K x 8	200	C, I	P, J	28/32	5 V ± 5%

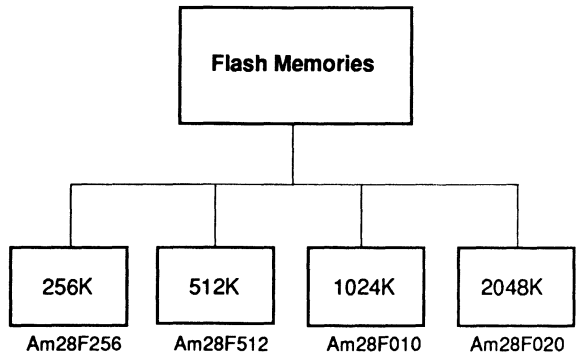
Notes: see page 1-10

ExpressROM Devices *(Cont.)*

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count (PDIP/PLCC)	Supply Voltage
Am27X256-200	32K x 8	200	C, I	P, J	28/32	5 V ± 10%
Am27X256-255[3]	32K x 8	250	C, I	P, J	28/32	5 V ± 5%
Am27X256-250	32K x 8	250	C, I	P, J	28/32	5 V ± 10%
Am27X512-125	64K x 8	120	C, I	P, J	28/32	
Am27X512-155	64K x 8	150	C, I	P, J	28/32	5 V ± 5%
Am27X512-150	64K x 8	150	C, I	P, J	28/32	5 V ± 10%
Am27X512-175[3]	64K x 8	170	C, I	P, J	28/32	5 V ± 5%
Am27X512-170[3]	64K x 8	170	C, I	P, J	28/32	5 V ± 10%
Am27X512-205[3]	64K x 8	200	C, I	P, J	28/32	5 V ± 5%
Am27X512-200	64K x 8	200	C, I	P, J	28/32	5 V ± 10%
Am27X512-255[3]	64K x 8	250	C, I	P, J	28/32	5 V ± 5%
Am27X512-250	64K x 8	250	C, I	P, J	28/32	5 V ± 10%
Am27X010-125	128K x 8	120	C, I	P, J	32/32	5 V ± 5%
Am27X010-155	128K x 8	150	C, I	P, J	32/32	5 V ± 5%
Am27X010-150	128K x 8	150	C, I	P, J	32/32	5 V ± 10%
Am27X010-175[3]	128K x 8	170	C, I	P, J	32/32	5 V ± 5%
Am27X010-205[3]	128K x 8	200	C, I	P, J	32/32	5 V ± 5%
Am27X010-200	128K x 8	200	C, I	P, J	32/32	5 V ± 10%
Am27X010-255[3]	128K x 8	250	C, I	P, J	32/32	5 V ± 5%
Am27X010-250	128K x 8	250	C, I	P, J	32/32	5 V ± 10%
Am27X100-125	128K x 8	120	C, I	P, J	32/32	5 V ± 5%
Am27X100-155	128K x 8	150	C, I	P, J	32/32	5 V ± 5%
Am27X100-150	128K x 8	150	C, I	P, J	32/32	5 V ± 10%
Am27X100-175[3]	128K x 8	170	C, I	P, J	32/32	5 V ± 5%
Am27X100-205[3]	128K x 8	200	C, I	P, J	32/32	5 V ± 5%
Am27X100-200	128K x 8	200	C, I	P, J	32/32	5 V ± 10%
Am27X100-255[3]	128K x 8	250	C, I	P, J	32/32	5 V ± 5%
Am27X100-250	128K x 8	250	C, I	P, J	32/32	5 V ± 10%
Am27X1024-175	64K x 16	170	C, I	P, J	40/44	5 V ± 5%
Am27X1024-205	64K x 16	200	C, I	P, J	40/44	5 V ± 5%
Am27X1024-200	64K x 16	200	C, I	P, J	40/44	5 V ± 10%
Am27X1024-255[3]	64K x 16	250	C, I	P, J	40/44	5 V ± 5%
Am27X1024-250	64K x 16	250	C, I	P, J	40/44	5 V ± 10%
Am27X020-155	256K x 8	150	C, I	P, J*	32/32	5 V ± 5%
Am27X020-175[3]	256K x 8	170	C, I	P, J*	32/32	5 V ± 5%
Am27X020-170[3]	256K x 8	170	C, I	P, J*	32/32	5 V ± 10%
Am27X020-205	256K x 8	200	C, I	P, J*	32/32	5 V ± 5%
Am27X020-200	256K x 8	200	C, I	P, J*	32/32	5 V ± 10%
Am27X020-255[3]	256K x 8	250	C, I	P, J*	32/32	5 V ± 5%
Am27X020-250	256K x 8	250	C, I	P, J*	32/32	5 V ± 10%
Am27X2048-155	128K x 16	150	C, I	P, J	40/44	5 V ± 5%
Am27X2048-175[3]	128K x 16	170	C, I	P, J	40/44	5 V ± 5%
Am27X2048-170[3]	128K x 16	170	C, I	P, J	40/44	5 V ± 10%
Am27X2048-205	128K x 16	200	C, I	P, J	40/44	5 V ± 5%
Am27X2048-200	128K x 16	200	C, I	P, J	40/44	5 V ± 10%
Am27X2048-255[3]	128K x 16	250	C, I	P, J	40/44	5 V ± 5%
Am27X2048-250	128K x 16	250	C, I	P, J	40/44	5 V ± 10%
Am27X040-125	512K x 8	120	C, I	P, J*	32/32	5 V ± 5%
Am27X040-155	512K x 8	150	C, I	P, J*	32/32	5 V ± 5%
Am27X040-150	512K x 8	150	C, I	P, J*	32/32	5 V ± 10%
Am27X040-200	512K x 8	200	C, I	P, J*	32/32	5 V ± 10%
Am27X040-250	512K x 8	250	C, I	P, J*	32/32	5 V ± 10%

* Contact the local AMD sales office for the availability of this device family.

Notes: see page 1-10



Am28Fxxx Family

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count (DIP/LCC, PLCC) and TSOP	Supply Voltage
Am28F256-95	32K x 8	90	C, I	P, J	32/32	5 V ± 5%
Am28F256-90	32K x 8	90	C, I	P, J	32/32	5 V ± 10%
Am28F256-120	32K x 8	120	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F256-150	32K x 8	150	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F256-200	32K x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F512-95	64K x 8	90	C	P, J	32/32	5 V ± 5%
Am28F512-90	64K x 8	90	C, I	P, J	32/32	5 V ± 10%
Am28F512-120	64K x 8	120	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F512-150	64K x 8	150	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F512-200	64K x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F010-95	128K x 8	90	C, I	P, J	32/32	5 V ± 5%
Am28F010-90	128K x 8	90	C, I	P, J	32/32	5 V ± 10%
Am28F010-120	128K x 8	120	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F010-150	128K x 8	150	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F010-200	128K x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F020-95	256K x 8	90	C, I	P, J	32/32	5 V ± 5%
Am28F020-90	256K x 8	90	C, I	P, J	32/32	5 V ± 10%
Am28F020-120	256K x 8	120	C, I, E, M	D, P, J	32/32	5 V ± 10%
Am28F020-150	256K x 8	150	C, I, E, M	D, P, J	32/32	5 V ± 10%
Am28F020-200	256K x 8	200	C, I, E, M	D, P, J	32/32	5 V ± 10%

Notes:

[1] Temp Range
- C = Commercial (0° to +70°C)
- I = Industrial (-40° to +85°)
- E = Extended Commercial (-55° to +125°C)
- M = Military (-55° to +125°C – most products available in both APL and DESC versions)

[2] Package Type
- C = Ceramic DIP
- L = Rectangular Ceramic Leadless Chip Carrier
- P = Plastic DIP
- J = Rectangular Plastic Leaded Chip Carrier

Flash Memories also available in Thin Small Outline Package (TSOP). Please consult factory for availabliity.

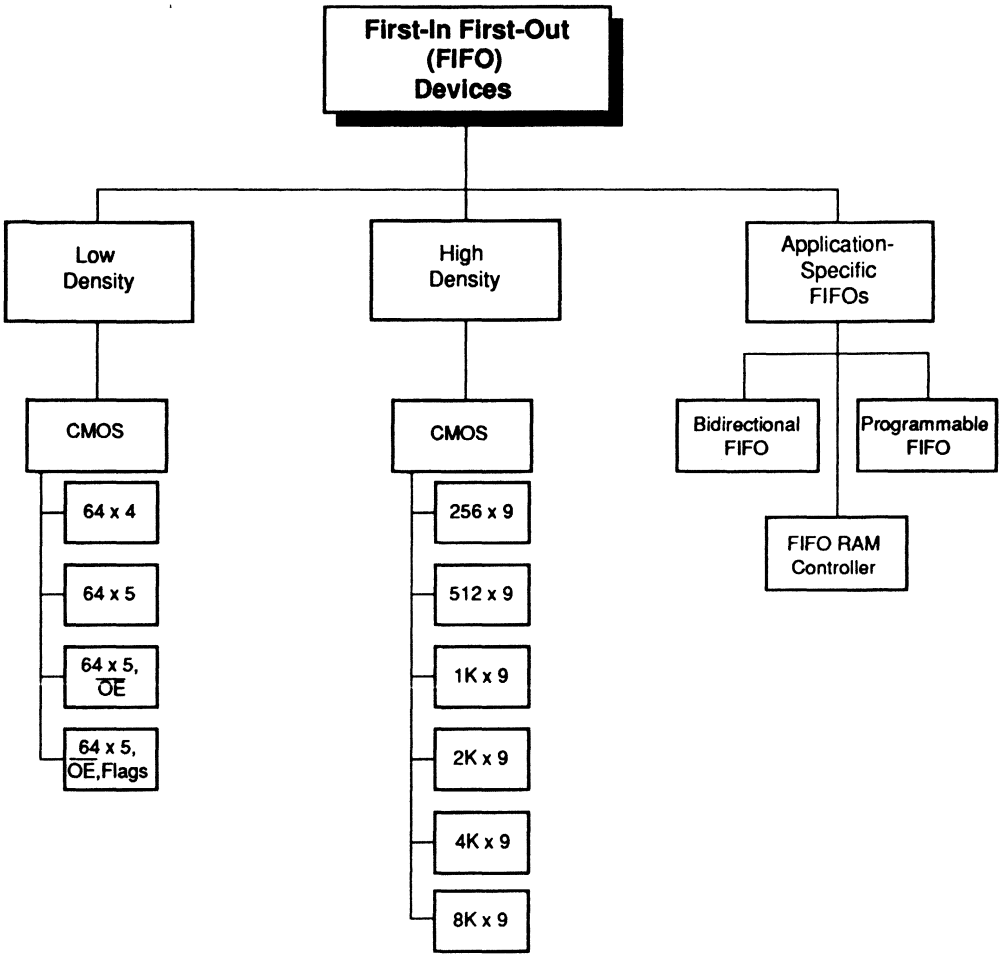
[3] These part numbers are not recommended for new designs. Alternative part types with improved margins are offered with no price premium. Please refer to the following table:

Part number	Recommended part
Am27Cxxx-95	Am27Cxxx-90
Am27Cxxx-105	Am27Cxxx-100
Am27Cxxx-125	Am27Cxxx-120
Am27Cxxx-155	Am27Cxxx-150
Am27Cxxx-170	Am27Cxxx-150
Am27Cxxx-175	Am27Cxxx-150
Am27Cxxx-205	Am27Cxxx-200
Am27Cxxx-250	Am27Cxxx-200
Am27Cxxx-305	Am27Cxxx-255
Am27Cxxx-300	Am27Cxxx-200

Note: ExpressROM equivalent part numbers begin with AM27X

[4] TheAm27C010-90 and Am27C010-95 are no longer in production. Order part number Am27H010-90 or Am27H010-90V05.

First-In First-Out Devices Selector Guide



Features and Benefits

Low Density CMOS FIFOs (64 x 4/5)

- Shift rates to 35 MHz
- Zero standby power consumption
- Ram-based technology with fast access times
- Three-state output and status flags
- Expandable in width and depth

High-Density CMOS FIFOs (256, 512, 1K, 2K, 4K, 8K x 9)

- Data Rates 0 to 40 MHz for standard products and 0 to 25 MHz for APL products
- Low power consumption – 100-mA max for – 15ms
- Status flags — Half-full, Empty, Full
- Asynchronous and simultaneous read/write
- Expandable in width and depth

FIFO IC Selector Guide

Low-Density FIFOs

Tech-nology	Part Number	Organ-ization	Type	Max Data Rate MHz	Max I_{CC} mA	Package Type	Pin Count	Features
C	67C401-10	64 x 4	C	10	35	N,J	16	TPO Low Power, RAM Based
C	67C401-15	64 x 4	C	15	45	N,J	16	TPO Low Power, RAM Based
C	67C4013-10	64 x 4	C	10	35	N,J	16	TSO Low Power, RAM Based
C	67C4013-15	64 x 4	C	15	45	N,J	16	TSO Low Power, RAM Based
C	67C402-10	64 x 5	C	10	35	N,J	18	TPO Low Power, RAM Based
C	67C402-15	64 x 5	C	15	45	N,J	18	TPO Low Power, RAM Based
C	67C4023-10	64 x 5	C	10	35	N,J	18	TSO Low Power, RAM Based
C	67C4023-15	64 x 5	C	15	45	N,J	18	TSO Low Power, RAM Based
C	67C4033-10	64 x 5	C	10	35	N,J	20	TSO Low Power, RAM Based, Status Flags, $\overline{OE}$
C	67C4033-15	64 x 5	C	15	45	N,J	20	TSO Low Power, RAM Based, Status Flags, $\overline{OE}$
C	67C401-25	64 x 4	C	25	60	N,J	16	TPO Low Power, RAM Based
C	67C401-35	64 x 4	C	35	60	N,J	16	TPO Low Power, RAM Based
C	67C4013-25	64 x 4	C	25	60	N,J	16	TSO Low Power, RAM Based
C	67C4013-35	64 x 4	C	35	60	N,J	16	TSO Low Power, RAM Based
C	67C402-25	64 x 5	C	25	60	N,J	18	TPO Low Power, RAM Based
C	67C402-35	64 x 5	C	35	60	N,J	18	TPO Low Power, RAM Based
C	67C4023-25	64 x 5	C	25	60	N,J	18	TSO Low Power, RAM Based
C	67C4023-35	64 x 5	C	35	60	N,J	18	TSO Low Power, RAM Based

Notes: Technology: C = CMOS; Type: C = Cascadable, S = Standalone; Package Type: N = Plastic DIP, J = Ceramic DIP; Features: TSO = Three-State Output, TPO = Totem-Pole Output

High-Density FIFOs

Tech-nology	Part Number	Organ-ization	Type	Max Data Rate MHz	Max I_{CC} mA	Package Type	Pin Count	Features
C	7200-80	256 x 9	C	10	60	PC, JC, RC	28, 32 (JC)	TSO Access Time = 80 ns, Status Flags
C	7200-65	256 x 9	C	12	60	PC, JC, RC	28, 32 (JC)	TSO Access Time = 65 ns, Status Flags
C	7200-50	256 x 9	C	15	60	PC, JC, RC	28, 32 (JC)	TSO Access Time = 50 ns, Status Flags
C	7200-35	256 x 9	C	22	60	PC, JC, RC	28, 32 (JC)	TSO Access Time = 35 ns, Status Flags
C	7200-25	256 x 9	C	28.5	70	PC, JC, RC	28, 32 (JC)	TSO Access Time = 25 ns, Status Flags
C	7201-80	512 x 9	C	10	60	PC, JC, RC	28, 32 (JC)	TSO Access Time = 80 ns, Status Flags
C	7201-65	512 x 9	C	12	60	PC, JC, RC	28, 32 (JC)	TSO Access Time = 65 ns, Status Flags
C	7201-50	512 x 9	C	15	70	PC, JC, RC	28, 32 (JC)	TSO Access Time = 50 ns, Status Flags
C	7201-35	512 x 9	C	22	80	PC, JC, RC	28, 32 (JC)	TSO Access Time = 35 ns, Status Flags
C	7201-25	512 x 9	C	28.5	90	PC, JC, RC	28, 32 (JC)	TSO Access Time = 25 ns, Status Flags
C	7202A-50	1K x 9	C	15	60	PC, JC, RC	28, 32 (JC)	TSO Access Time = 50 ns, Status Flags
C	7202A-35	1K x 9	C	22	60	PC, JC, RC	28, 32 (JC)	TSO Access Time = 35 ns, Status Flags
C	7202A-25	1K x 9	C	28.5	70	PC, JC, RC	28, 32 (JC)	TSO Access Time = 25 ns, Status Flags
C	7202A-15	1K x 9	C	40	100	JC, RC	28, 32 (JC)	TSO Access Time = 15 ns, Status Flags
C	7203A-50	2K x 9	C	15	60	PC, JC, RC	28, 32 (JC)	TSO Access Time = 50 ns, Status Flags
C	7203A-35	2K x 9	C	22	60	PC, JC, RC	28, 32 (JC)	TSO Access Time = 35 ns, Status Flags
C	7203A-25	2K x 9	C	28.5	70	PC, JC, RC	28, 32 (JC)	TSO Access Time = 25 ns, Status Flags
C	7203A-15	2K x 9	C	40	100	JC, RC	28, 32 (JC)	TSO Access Time = 15 ns, Status Flags
C	7204A-50	4K x 9	C	15	60	PC, JC, RC	28, 32 (JC)	TSO Access Time = 50 ns, Status Flags
C	7204A-35	4K x 9	C	22	60	PC, JC, RC	28, 32 (JC)	TSO Access Time = 35 ns, Status Flags
C	7204A-25	4K x 9	C	28.5	70	PC, JC, RC	28, 32 (JC)	TSO Access Time = 25 ns, Status Flags
C	7204A-15	4K x 9	C	40	100	JC, RC	28, 32 (JC)	TSO Access Time = 15 ns, Status Flags
C	7205A-35	8K x 9	C	22.2	80	RC	28	TSO Access Time = 35 ns, Status Flags
C	7205A-25	8K x 9	C	28.5	90	RC	28	TSO Access Time = 25 ns, Status Flags
C	7205A-15	8K x 9	C	40	100	RC	28	TSO Access Time = 15 ns, Status Flags

Notes: Technology: B = Bipolar, C = CMOS; Type: C = Cascadable, S = Standalone; Package Type: PC = 600 MIL Plastic DIP, JC = Plastic Leaded Chip, RC = 300 mil Plastic Dip; Features: TSO = Three-State Output

Application-Specific FIFOs

Technology	Part Number	Organization	Type	Max Data Rate MHz	Max I_{cc} mA	Package Type	Pin Count	Features
C	Am4701	Dual 512 x 8	S	17	100	PC, JC	28, 32 (JC)	TSO Access Time = 30 ns, 35 ns, Programmable Flags
C	Am4601	512 x 9	S	28.5	100	RC, JC	28, 32 (JC)	TSO Access Time = 25 ns, 35 ns Programmable Flags
B	674219	512 x 64K	S	10	350	J	40	TSO FIFO RAM Controller, 16-Bit SRAM Address, Status Flags

Notes: Technology:
B = Bipolar
C = CMOS

Type:
C = Cascadable
S = Standalone

Package Type:
PC, RC = Plastic DIP
JC = Plastic Leaded Chip

Features:
TSO = Three-State Output

FIFO Cross Reference Guide

LOW DENSITY CMOS

AMD	CYPRESS	IDT	SAMSUNG
67C401-10J	CY7C401-10DC	IDT72401L10D	
67C401-10N	CY7C401-10PC	IDT72401L10P	
67C401-15J	CY7C401-15DC	IDT72401L15D	
67C401-15N	CY7C401-15PC	IDT72401L15P	
67C401-25N	CY7C401-25PC	IDT72401L25P	
67C401-35J	CY7C401-25PC	IDT72401L25P	
67C4013-10J	CY7C403-10DC	IDT72403L10D	
67C4013-10N	CY7C403-10PC	IDT72403L10P	
67C4013-15J	CY7C403-10DC	IDT72403l15D	
67C4013-15N	CY7C403-15PC	IDT72043L15P	
67C4013-25N	CY7C403-15DC	IDT72043L25D	
67C4013-25N	CY7C403-25PC	IDT72043L25P	
67C402-10J	CY7C402-5/-10DC	IDT72402L10D	
67C402-10N	CY7C402-5/-10PC	IDT72402L10P	
67C402-15J	CY7C402-15DC	IDT72402L15D	
67C402-15N	CY7C402-15PC	IDT72402L15P	
67C402-25N	CY7C402-25PC	IDT72402L25P	
67C4023-10J	CY7C404-5/-10DC	IDT72404L10D	
67C4023-10N	CY7C404-5/-10PC	IDT72404L10P	
67C4023-15J	CY7C404-15DC	IDT72404L15D	
67C4023-15N	CY7C404-15PC	IDT72404L15P	
67C4023-25N	CY7C404-25PC	IDT72404L25P	

HIGH DENSITY CMOS

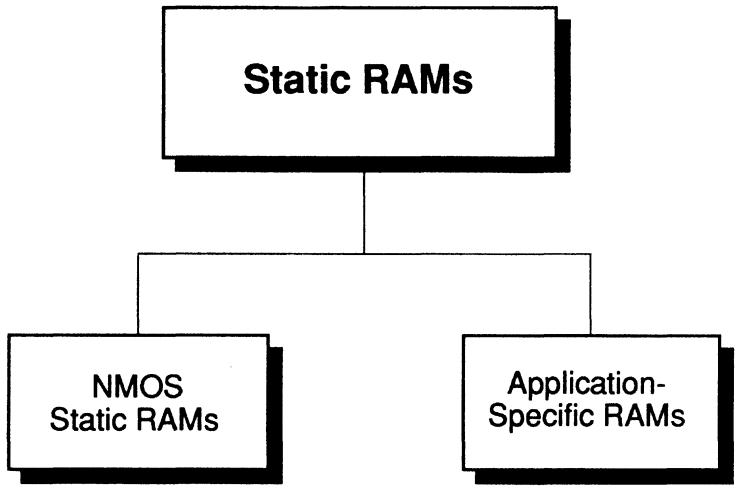
AMD	CYPRESS	IDT	SAMSUNG
Am7200-25JC		IDT7200S/L25J	
Am7200-25PC		IDT7200S/L25P	
Am7200-25RC		IDT7200S/L25TP	
Am7200-35JC		IDT7200S/L35J	
Am7200-35PC		IDT7200S/L35P	
Am7200-35RC		IDT7200S/L35TP	
Am7200-50JC		IDT7200S/L50J	
Am7200-50PC		IDT7200S/L50P	
Am7200-50RC		IDT7200S/L50TP	
Am7200-65JC		IDT7200S/L65J	
Am7200-65PC		IDT7200S/L65P	
Am7200-65RC		IDT7200S/L65TP	
Am7200-80JC		IDT7200S/L80J/120J	
Am7200-80PC		IDT7200S/L80P/120P	
Am7200-80RC		IDT7200S/L80TP/120TP	
Am7201-25JC	CY7C421-25JC	IDT7201SA/LA25J	KM75C01AJ-25
Am7201-25PC	CY7C420-25PC	IDT7201SA/LA25P	KM75C01AP-25
Am7201-25RC	CY7C421-25PC	IDT7201SA/LA25TP	KM75C01AN-25
Am7201-35JC	CY7C421-40JC	IDT7201SA/LA35J	KM75C01AJ-35
Am7201-35PC	CY7C420-40PC	IDT7201SA/LA35P	KM75C01AP-35
Am7201-35RC	CY7C421-40PC	IDT7201SA/LA35TP	KM75C01AN-35
Am7201-50JC		IDT7201S/L/SA/LA50J	KM75C01AJ-50
Am7201-50PC		IDT7201S/L/SA/LA50P	KM75C01AP-50
Am7201-50RC		IDT7201S/L/SA/LA50TP	KM75C01AN-50

FIFO Cross Reference Guide

HIGH DENSITY CMOS (Continued)

AMD	CYPRESS	IDT	SAMSUNG
Am7201-65JC	CY7C421-65JC	IDT7201S/L/SA/LA65J	
Am7201-65PC	CY7C420-65PC	IDT7201S/L/SA/LA65P	
Am7201-65RC	CY7C421-65PC	IDT7201S/L/SA/LA65TP	
Am7201-80JC		IDT7201S/L/SA/LA80J/120J	KM75C01AJ-80
Am7201-80PC		IDT7201S/L/SA/LA80P/120P	KM75C01AP-80
Am7201-80RC		IDT7201S/L/SA/LA80TP/120TP	KM75C01AN-80
Am7202A-15JC			
Am7202A-15RC			
Am7202A-25JC	CY7C425-25JC	IDT7202SA/LA25J	KM75C02AJ-25
Am7202A-25PC	CY7C424-25PC	IDT7202SA/LA25P	KM75C02AP-25
Am7202A-25RC	CY7C425-25PC	IDT7202SA/LA25TP	KM75C02AN-25
Am7202A-35JC	CY7C425-40JC	IDT7202SA/LA35J	KM75C02AJ-35
Am7202A-35PC	CY7C424-40PC	IDT7202SA/LA35P	KM75C02AP-35
Am7202A-35RC	CY7C425-40PC	IDT7202SA/LA/35TP	KM75C02AN-35
Am7202A-50JC		IDT7202S/L/SA/LA50J	KM75C03AJ-50
Am7202A-50PC		IDT7202S/L/SA/LA50P	KM75C02AP-50
Am7202A-50RC		IDT7202S/L/SA/LA80TP/120TP	KM75C02AN-50
Am7203A-15JC			
Am7203A-15RC			
Am7203A-25JC	CY7C429-25JC		KM75C03AJ-25
Am7203A-25PC	CY7C428-25PC		KM75C03AP-25
Am7203A-25RC	CY7C429-25PC		KM75C03AN-25
Am7203A-35JC	CY7C429-40JC	IDT7203S/L35J	KM75C03AJ-35
Am7203A-35PC	CY7C428-40PC	IDT7203S/L35P	KM75C03AP-35
Am7203A-35RC	CY7C429-40PC		KM75C03AN-35
Am7203A-50JC		IDT7203S/L50/65/80J	KM75C03AJ-50
Am7203A-50PC		IDT7203S/L50/65/80P	KM75C03AP-50
Am7203A-50RC			KM75C03AN-50
Am7204A-15JC			
Am7204A-15RC			
Am7204A-25JC	CY7C433-25JC		
Am7204A-25PC	CY7C432-25PC		
Am7204A-25RC	CY7C433-25PC		
Am7204A-35JC	CY7C433-40JC	IDT7204S/L35J	
Am7204A-35PC	CY7C432-40PC	IDT7204S/L35P	
Am7204A-35RC	CY7C433-40PC	IDT7204S/L35TP	
Am7204A-50JC		IDT7204S/L50/65/80J	
Am7204A-50PC		IDT7204S/L50/65/80P	
Am7204A-50RC		IDT7204S/L50/65/80TP	
Am7205A-15RC			
Am7205A-25RC		IDT7205L25TP	
Am7205A-35RC		IDT7205L50TP	

Static RAMs Selector Guide*

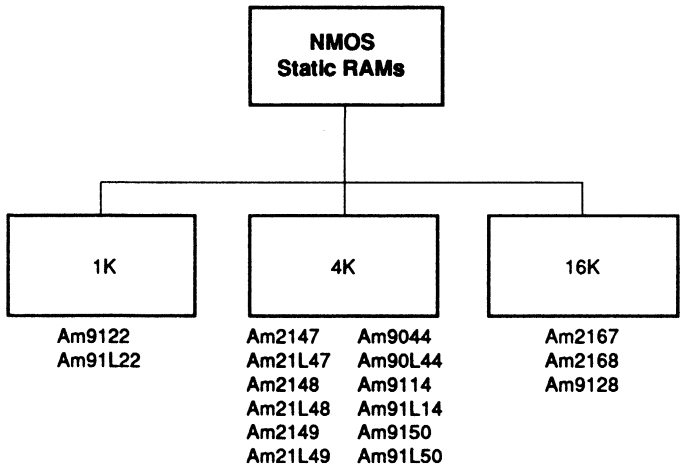


Introduction

AMD's current product offerings in Static RAMs are comprised of NMOS and application-specific Static RAMs. The NMOS product offering ranges from 1K to 16K densities.

One of the ASIC RAM products currently in production is the Am99C10A, a proprietary high performance CMOS Content Addressable Memory (CAM) with a capacity of 256 words and 48 bits per word. The Am99C10A is optimized for address decoding in Local Area Network (LAN) and bridging applications.

*Other than the Am99C10A which is featured in Section 5, there are no Static RAM data sheets in this book. You may obtain a data sheet for a specific device by contacting your local AMD representative or calling the 800 literature number–(800)222-9323.



NMOS Static RAMs

1K Static RAMs

Part Number	Organization	Access Time (ns)	Power Dissipation (mW)		Pin Count	Supply Voltage	Temp Range[1]	Package Type[2]
			Standby	Active				
Am9122-25	256 x 4	25	N/A	600	22	5 V	C	D, P
Am9122-35	256 x 4	35	N/A	600	22	5 V	C, M	D, P
Am91L22-35	256 x 4	35	N/A	400	22	5 V	C	D, P
Am91L22-45	256 x 4	45	N/A	400	22	5 V	C, M	D, P

4K Static RAMs

Part Number	Organization	Access Time (ns)	Power Dissipation (mW)		Pin Count	Supply Voltage	Temp Range[1]	Package Type[2]
			Standby	Active				
Am2147-35	4096 x 1	35	150	900	18	5 V	C	D, L, P
Am2147-45	4096 x 1	45	150	900	18	5 V	C, M	D, L, F, P
Am2147-55	4096 x 1	55	150	900	18	5 V	C, M	D, L, F, P
Am2147-70	4096 x 1	70	100	800	18	5 V	C, M	D, L, F, P
Am21L47-45	4096 x 1	45	75	625	18	5 V	C	D, L, P
Am21L47-55	4096 x 1	55	75	625	18	5 V	C	D, L, P
Am21L47-70	4096 x 1	70	75	625	18	5 V	C	D, L, P
Am2148-35	1024 x 4	35	150	900	18	5 V	C	D, L, P
Am2148-45	1024 x 4	45	150	900	18	5 V	C, M	D, L, P
Am2148-55	1024 x 4	55	150	900	18	5 V	C, M	D, L, P
Am2148-70	1024 x 4	70	150	900	18	5 V	C, M	D, L, P
Am21L48-45	1024 x 4	45	100	625	18	5 V	C	D, L, P
Am21L48-55	1024 x 4	55	100	625	18	5 V	C	D, L, P
Am21L48-70	1024 x 4	70	100	625	18	5 V	C	D, L, P

Notes: see page 1-10

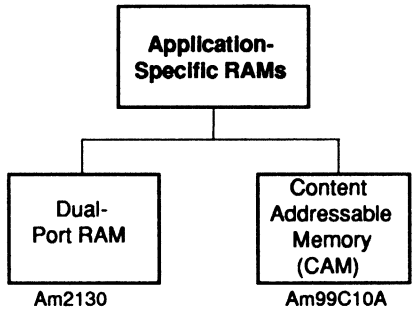
4K Static RAMs *(Cont.)*

Part Number	Organization	Access Time (ns)	Power Dissipation (mW)		Pin Count	Supply Voltage	Temp Range[1]	Package Type[2]
			Standby	Active				
Am2149-35	1024 x 4	35	N/A	900	18	5 V	C	D, L, P
Am2149-45	1024 x 4	45	N/A	900	18	5 V	C, M	D, L, P
Am2149-55	1024 x 4	55	N/A	900	18	5 V	C, M	D, L, P
Am2149-70	1024 x 4	70	N/A	900	18	5 V	C, M	D, L, P
Am21L49-45	1024 x 4	45	N/A	625	18	5 V	C	D, L, P
Am21L49-55	1024 x 4	55	N/A	625	18	5 V	C	D, L, P
Am21L49-70	1024 x 4	70	N/A	625	18	5 V	C	D, L, P
Am9044B	4096 x 1	450	N/A	350	18	5 V	C, M	D, P
Am90L44B	4096 x 1	450	N/A	250	18	5 V	C, M	D, P
Am9044C	4096 x 1	300	N/A	350	18	5 V	C, M	D, P
Am90L44C	4096 x 1	300	N/A	250	18	5 V	C, M	D, P
Am9044D	4096 x 1	250	N/A	350	18	5 V	C, M	D, P
Am90L44D	4096 x 1	250	N/A	250	18	5 V	C, M	D, P
Am9044E	4096 x 1	200	N/A	350	18	5 V	C	D, P
Am90L44E	4096 x 1	200	N/A	250	18	5 V	C	D, P
Am9114B	1024 x 4	450	N/A	350	18	5 V	C, M	D, P
Am91L14B	1024 x 4	450	N/A	250	18	5 V	C, M	D, P
Am9114C	1024 x 4	300	N/A	350	18	5 V	C, M	D, P
Am91L14C	1024 x 4	300	N/A	250	18	5 V	C, M	D, P
Am9114E	1024 x 4	200	N/A	350	18	5 V	C, M	D, P
Am91L14E	1024 x 4	200	N/A	250	18	5 V	C, M	D, P
Am9150-20	1024 x 4	20	N/A	900	24	5 V	C	D, L, P
Am9150-25	1024 x 4	25	N/A	900	24	5 V	C, M	D, L, P
Am9150-35	1024 x 4	35	N/A	900	24	5 V	C, M	D, L, P
Am9150-45	1024 x 4	45	N/A	900	24	5 V	C, M	D, L, P
Am91L50-20	1024 x 4	20	N/A	650	24	5 V	C	D, P
Am91L50-25	1024 x 4	25	N/A	650	24	5 V	C	D, P
Am91L50-35	1024 x 4	35	N/A	650	24	5 V	C	D, P
Am91L50-45	1024 x 4	45	N/A	650	24	5 V	C	D, P

16K Static RAMs

Part Number	Organization	Access Time (ns)	Power Dissipation (mW)		Pin Count	Supply Voltage	Temp Range[1]	Package Type[2]
			Standby	Active				
Am2167-35	16384 x 1	35	100	600	20	5 V	C	D, P, L
Am2167-45	16384 x 1	45	100	600	20	5 V	C, M	D, P, L
Am2167-55	16384 x 1	55	100	600	20	5 V	C, M	D, P, L
Am2167-70	16384 x 1	70	100	600	20	5 V	C, M	D, P, L
Am2168-35	4096 x 4	35	150	600	20	5 V	C	D, P
Am2168-45	4096 x 4	45	150	600	20	5 V	C, M	D, P, L
Am2168-55	4096 x 4	55	150	600	20	5 V	C, M	D, P, L
Am2168-70	4096 x 4	70	150	600	20	5 V	C, M	D, P,
Am9128-10	2048 x 8	100	75	600	24	5 V	C	D, P
Am9128-12	2048 x 8	120	150	750	24	5 V	M	D
Am9128-15	2048 x 8	150	75	500	24	5 V	C, M	D, P
Am9128-20	2048 x 8	200	150	700	24	5 V	C, M	D, P
Am9128-70	2048 x 8	70	150	700	24	5 V	C	D, P
Am9128-90	2048 x 8	90	150	900	24	5 V	M	D

Notes: see page 2-21



Application-Specific RAMs

Dual Port RAM

Part Number	Organization	Access Time (ns)	Power Dissipation (mW)		Pin Count DIP/PLCC	Supply Voltage	Temp Range[1]	Package Type[2]
			Standby	Active				
Am2130-55	1024 x 8	55	605/220	935	48/52	5 V	C, M	D, P, J
Am2130-70	1024 x 8	70	605/220	935	48/52	5 V	C, M	D, P, J
Am2130-100	1024 x 8	100	605/220	935	48/52	5 V	C, M	D, P, J
Am2130-120	1024 x 8	120	605/220	935	48/52	5 V	C, M	D, P, J

Content Addressable Memory (CAM)

Part Number	Organization	Access Time (ns)	Power Dissipation (mW)		Pin Count DIP/PLCC	Supply Voltage	Temp Range[1]	Package Type[2]
			Standby	Active				
Am99C10A-10	256 x 48	100	55	715	28/32	5 V	C	D, P, J
Am99C10A-70	256 x 48	70	55	715	28/32	5 V	C	D, P, J

Notes: see page 1-10

SECTION 2
CMOS Erasable Programmable Read Only Memories (EPROMs)

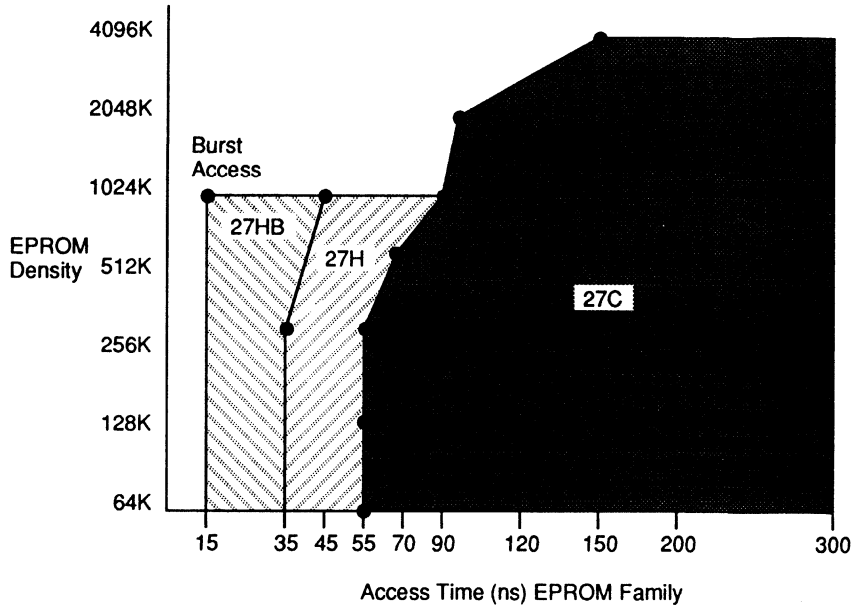
An Introduction to Electrically Erasable Read Only Memories (EPROMs)

Advanced Micro Devices has consistently improved the CMOS process used to manufacture EPROMs to remain the technology leader in the marketplace. In addition to providing lower cost and higher density EPROM solutions, AMD's advanced CMOS process creates the highest performance devices in the industry. The devices that achieve high speed through process technology identified as "Am27C". This family provides the designer with a broad range of speeds and densities for most designs. AMD has also introduced a family of CMOS EPROMs that have been designed especially for speed. This "Am27H" family supports 35 ns and 45 ns speeds at the 256K and 1 Megabit densities, respectively. These are truly the fastest EPROMs in the world.

These high speed "commodity" EPROMs and ultra-high performance "27H" EPROMs allow the systems designer to maximize microprocessor efficiency by matching clock speed with access time. This performance edge also benefits digital signal processor (DSP) and other users by doing away with the need for expensive shadow RAM.

AMD's product portfolio also includes two application specific EPROMs. For RISC processor applications, the 27HB010 1 Megabit 'burst access mode' EPROM offers a 15 ns sequential access capability. For portable systems with power sensitive requirements, AMD offers the Am27C512L. This device is functionally identical to the Am27C512 but offers an 88 percent power savings. The Am27C512L operates on a miserly 5 mA of current (worst case) in the active mode at speeds of 5 MHz.

EPROM Speed Selector Overview



High Speed EPROMs and Microprocessors

With the advent of the current generation of high speed microprocessors and their increasing use in embedded control systems it is becoming more and more important to match clock speed with memory access time. The impact of a slow memory can have a drastic effect on system performance and cost. Until recently the designer's only choices have been to use PROMs or copy the contents of slow EPROMs into faster DRAMs or SRAMs. Both of these solutions are expensive in terms of both device cost and board area. Advanced Micro Devices manufactures a full line of high speed EPROMs that enable the designer to produce systems that allow microprocessors to achieve maximum performance.

The standard method of interfacing to slow EPROMs is by adding wait states to the memory access cycle. At first this may not seem to be a problem. However, with a typical memory cycle requiring 3 CPU cycles, each additional cycle is a 30% reduction in speed! The performance of an expensive 25 MHz processor can easily be reduced to that of a 16 MHz version simply by adding 2 wait states. This magnitude of performance degradation is not acceptable in the competitive market of today.

Table 1

CPU Clock Frequency	Wait States	EPROM Access Time	Memory Access Cycle Time
33 MHz	0	35 ns	90 ns
33 MHz	1	70 ns	120 ns
25 MHz	0	45 ns	120 ns
25 MHz	1	90 ns	160 ns
20 MHz	0	55 ns	150 ns
20 MHz	1	120 ns	200 ns
16 MHz	0	70 ns	190 ns
16 MHz	1	150 ns	250 ns

The table above lists CPU clock speed and the required EPROM access time for the given wait states. It should be noted that by inserting just one wait state (see Memory Access Cycle Time above) the performance of the CPU is degraded to that of the slower clock speed with zero wait states. Considering the cost premium for the faster CPU, the simple insertion of a wait state can undermine the cost/performance ratio of the final system.

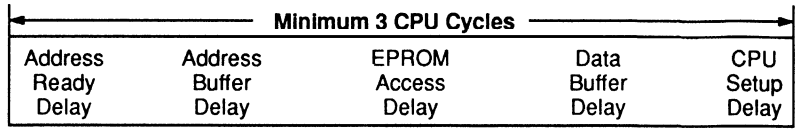
There have been two traditional engineering solutions to this problem:

- utilize a combination of slow EPROM and faster DRAM and/or SRAM, and
- utilize interleaving banks of memory

Both of the above solutions do work but at the expense of increasing cost to achieve the desired performance. The increased cost comes in the form of:

- inefficient utilization of memory due to duplication
- payment of premium prices for high speed SRAM/DRAM, and
- increase of real estate and decreased reliability due to higher component count.

Advanced Micro Devices offers a better solution by eliminating wait states. High speed (45–120 ns) EPROMs are available, and designing a system using them is very easy. Don't add wait states! Most manufacturers have a formula listed in their design manuals that is used to calculate the EPROM access time required. They suggest that you vary the number of wait states in the formula until you hit on the access time of an EPROM that they manufacture. May we suggest that you use zero wait states in their formula and choose an EPROM listed in this data book.



CPU Memory Access Delay Path

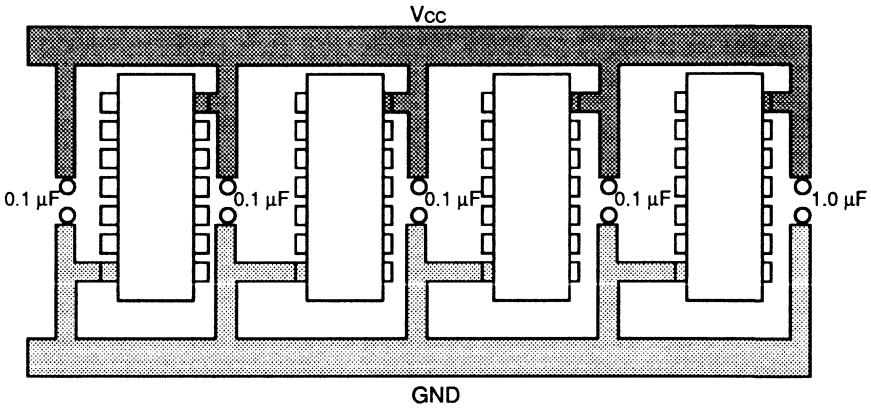
Board Layout and Bypassing Methods for High Speed EPROMs

Now that you have made the decision to get maximum performance from your microprocessor here are a few tips to make sure that your design goes to production smoothly. These tips are general system tips and are not unique to EPROMs. They can be used in any high speed design.

As system speed increases so does the power supply noise, which can disrupt the system if left unchecked. There are some simple methods for reducing noise that can be used as guidelines when designing and laying out systems. The extent to which these tips are used in your design will depend on PC board size, total power supply capacity, length of feed lines from the power supply, presence of a ground plane in the PC board, clock speed, etc. There is no way to come up with an exact formula to minimize noise, so it is best to start with a standard setup and then modify it to fit the current design.

Rule of thumb number 1:

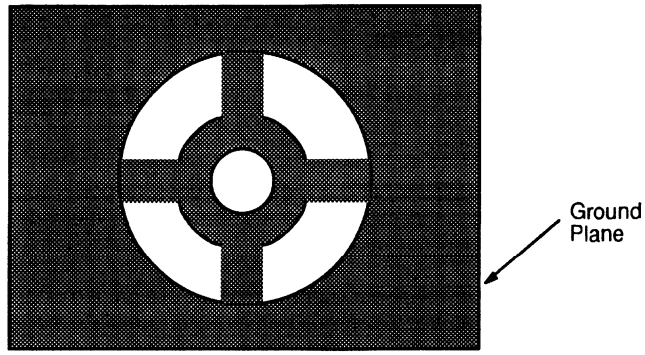
- Place a 0.1 µf capacitor as close as possible to *every* IC between V_{CC} and GND.
- Place a 1.0 µf capacitor between V_{CC} and GND for every four ICs on a power trace.



Rule of thumb number 2:

- Use power planes if you can.

This generally requires a multi-layer PC board that uses one or two of the internal layers to carry the power to each IC with very large traces. Don't forget to provide heat relief on the holes.



Typical Ground Plane
Heat Relief Pattern

- If power planes cannot be used for some reason, then do not snake the trace.

Use a comb pattern to distribute the power to the ICs. Run heavy buses down the side of the board with smaller traces taking the power between the ICs and smaller traces yet taking the power to the individual ICs.

Rule of thumb number 3:

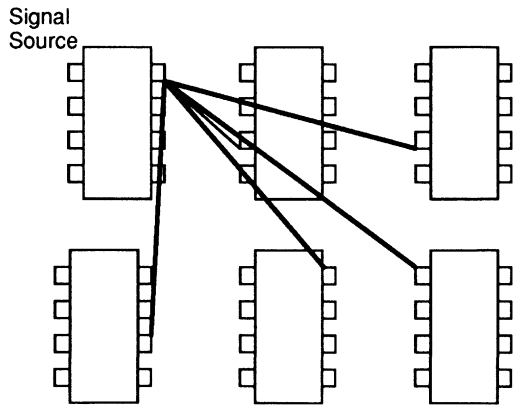
If you must wire wrap the prototype design place the bypass capacitors on the wire side of the board and solder them directly to the socket. Save yourself a lot of time and trouble and do this before you wire the board.

Rule of thumb number 4:

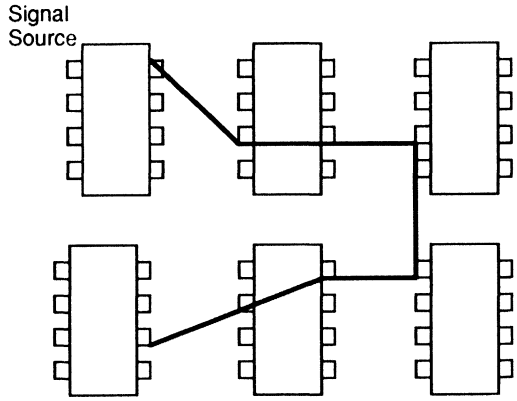
When wiring a prototype do not channel the wires. This looks nice but you will spend a lot of time looking for cross talk problems, where the signal is coupled from one wire to another. Use direct point-to-point wiring.

Rule of thumb number 5:

Use a crow foot wiring pattern and not a daisy chain pattern. Have the heel of the crow foot at the signal source to drive the entire foot.

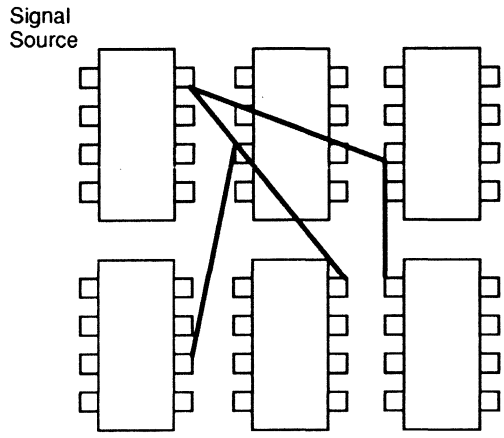


Example of a Crow Foot Pattern



Example of a Daisy Chain Pattern

If there are too many destinations for the signal to be supplied from a single pin, use a modified crow foot.



Example of a Modified Crow Foot Pattern

Am27C64

8,192 x 8-Bit CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time–55 ns**
- **Low power consumption: –100 µA maximum standby current**
- **Programming voltage: 12.75 V**
- **Single +5 -V power supply**
- **JEDEC–approved pinout**
- **±10% power supply tolerance**
- **Fast Flashrite™ programming**
- **Latch–up protected to 100 mA from –1 V to Vcc +1 V**

GENERAL DESCRIPTION

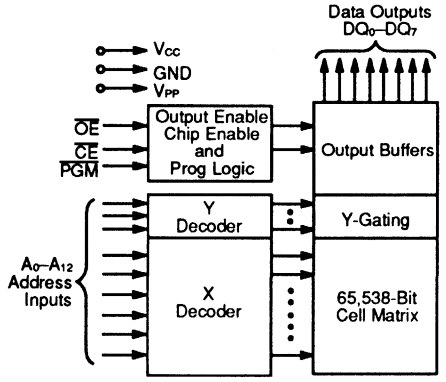
The Am27C64 is a 64K-bit, ultraviolet erasable programmable read-only memory. It is organized as 8,192 words by 8 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

Typically, any byte can be accessed in less than 55 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C64 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random.

BLOCK DIAGRAM



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PRODUCT SELECTOR GUIDE

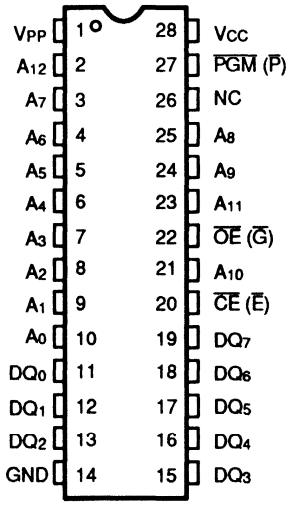
Family Part No.	Am27C64						
Ordering Part Number ±5% Vcc Tolerance	–55	–75					-255
±10% Vcc Tolerance	–	–70	–90	–120	–150	–200	–250
Max. Access Time (ns)	55	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	55	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	40	40	50	65	75	100

Publication# 11419 Rev. B Amendment/0
Issue Date: March 1991

CONNECTION DIAGRAMS

Top View

DIP



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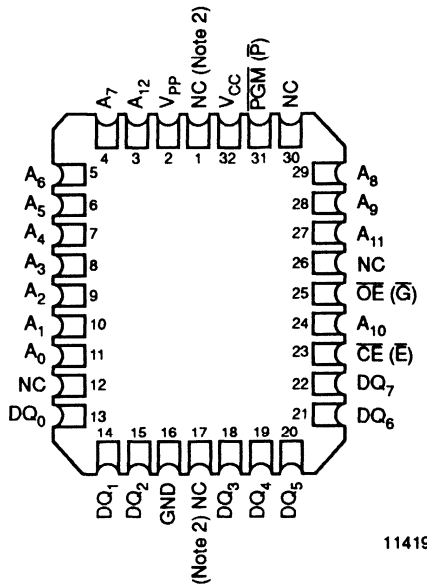
LCC*



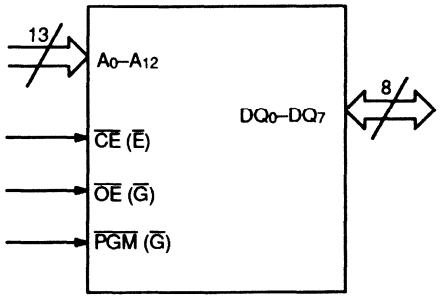
11419-003A

* Also Available in a 32-pin rectangular plastic leaded chip carrier

Notes:

1. JEDEC nomenclature is in parantheses.
2. Don't use (DU) for PLCC.

LOGIC SYMBOL



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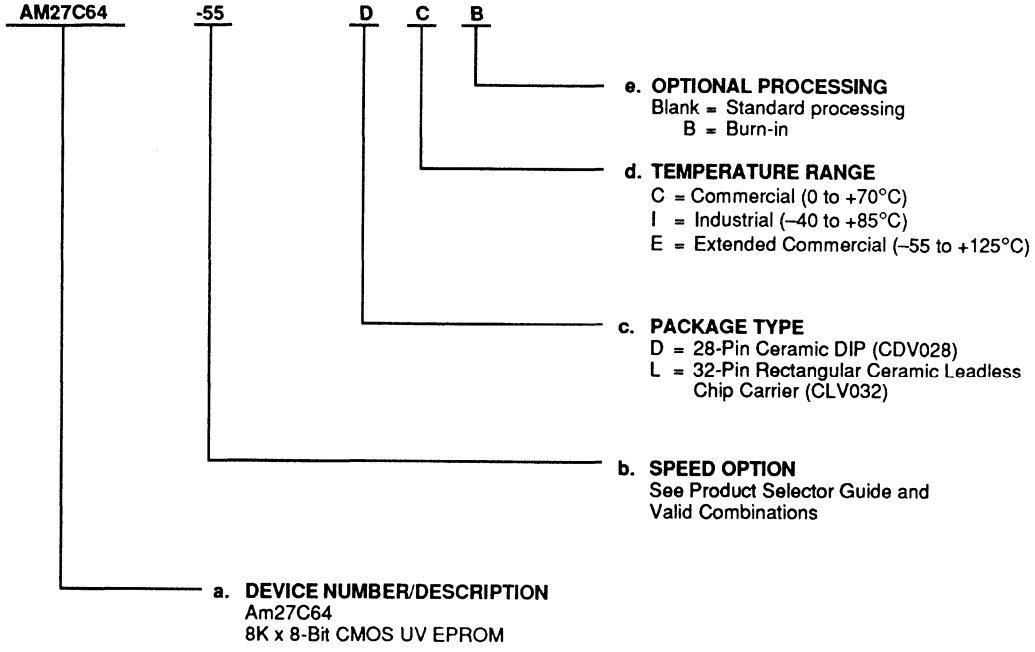
PIN DESCRIPTION

$A_0 - A_{12}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_7$	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27C64-55	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C64-70	
AM27C64-75	
AM27C64-90	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB,
AM27C64-120	
AM27C64-150	
AM27C64-200	
AM27C64-255	

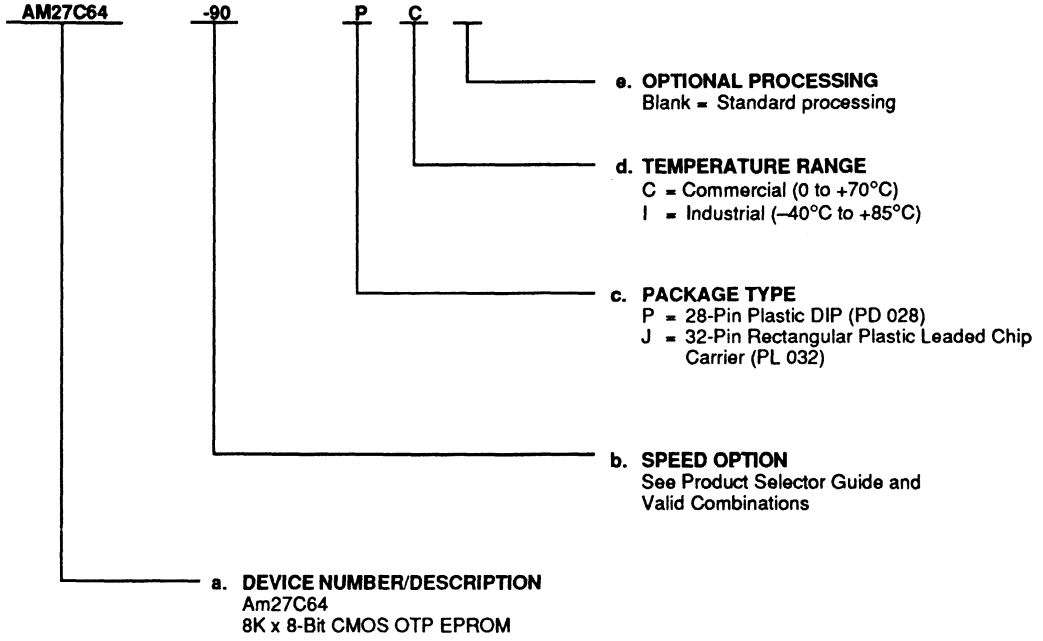
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27C64-90	JC, PC
AM27C64-120	JC, PC, JI, PI
AM27C64-150	
AM27C64-200	
AM27C64-255	

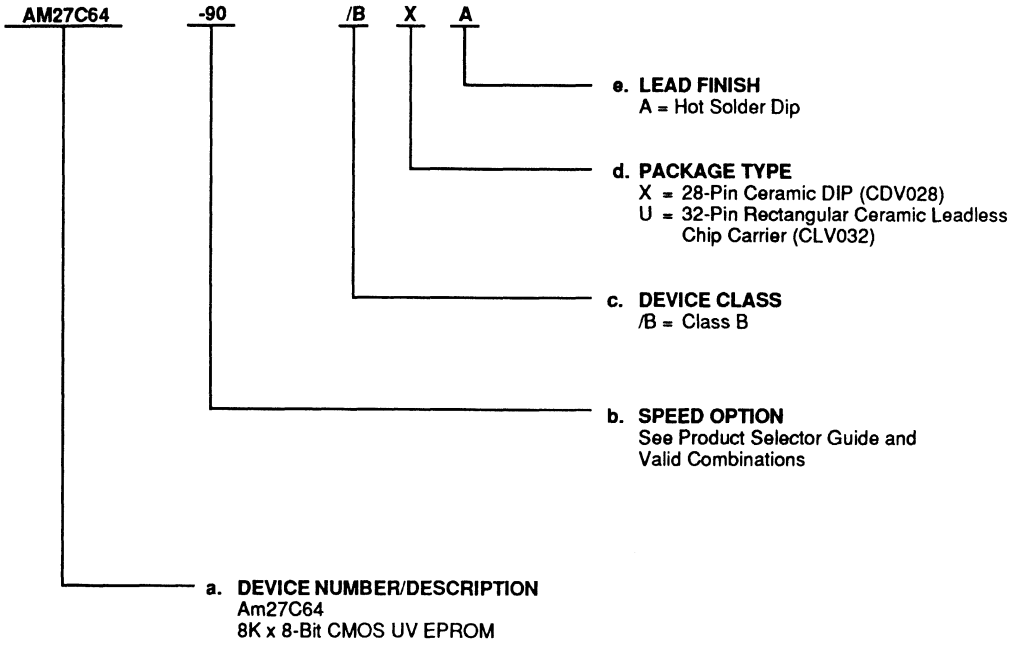
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Lead Finish



Valid Combinations	
AM27C64-90	/BXA, /BUA
AM27C64-120	
AM27C64-150	
AM27C64-200	
AM27C64-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C64

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C64 to an ultraviolet light source. A dosage of 15 W seconds/cm2 is required to completely erase an Am27C64. This dosage can be obtained by exposure to an ultraviolet lamp-wavelength of 2537 Angstroms (A)-with intensity of 12,000 µW/cm2 for 15 to 20 minutes. The Am27C64 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C64, and similar devices, will erase with light sources having wavelengths shorter than 4000 A. Although erasure times will be much longer than with UV sources at 2537 A, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C64 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C64

Upon delivery, or after each erasure, the Am27C64 has all 65,336 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C64 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ is at V_{IL}, and $\overline{PGM}$ is at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite programming algorithm (shown in Figure 1) reduces programming time by using initial 100 µs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.25 V.

Program Inhibit

Programming of multiple Am27C64s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C64 may be common. A TTL low-level program pulse applied to an Am27C64 $\overline{PGM}$ input with V_{PP} = 12.75 ± 0.25 and $\overline{CE}$ LOW will program that Am27C64. A high-level $\overline{CE}$ input inhibits the other Am27C64s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}. $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmeed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C64.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C64. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A_0 = V_{IL}) represents the manufacturer code, and byte 1 (A_0 = V_{IH}), the device identifier code. For the Am27C64, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C64 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}—t_{OE}.

Standby Mode

The Am27C64 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C64 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL–standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high–impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accomodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	V_{CC}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	V_{CC}	High Z
Standby (TTL)		V_{IH}	X	X	X	X	V_{CC}	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	V_{CC}	High Z
Program		V_{IL}	X	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	V_{CC}	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	V_{CC}	15H

Notes:

1. X can be either V_{IL} or V_{IH}
2. $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$
3. A_1–$A_8 = A_{10}$–$A_{12} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	–65 to + 125°C
All Other Products	–65 to + 150°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC} (Note 1)	–0.6 to V_{CC} + 0.6 V
A_9 and V_{PP} (Note 2)	–0.6 to 13.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. During transitions the inputs may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (Tc)	0 to +70°C
Industrial (I) Devices	
Case Temperature (Tc)	–40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (Tc)	–55 to +125°C
Military (M) Devices	
Case Temperature (Tc)	–55 to +125°C
Supply Read Voltages:	
V_{CC}/V_{PP} for Am27C64–XX5	+4.75 to +5.25 V
V_{CC}/V_{PP} for Am27C64–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		10	µA
			E/M Devices		10	
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = VIL, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		30	mA
			E/M Devices		30	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	C/I Devices		1.0	mA
			E/M Devices		1.0	
I_{PP1}	V_{PP} Supply Current (Read) (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

DC CHARACTERISTICS over operating range unless otherwise specified (Continued)

CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			V_{CC} – 0.3	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		10	µA
			E/M Devices		10	
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = VIL, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		25	mA
			E/M Devices		25	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	C/I Devices		100	µA
			E/M Devices		120	
I_{PP1}	V_{PP} Supply Current (Read) (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	9	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27C64 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. TA = 25°C, f = 1 MHz.
8. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns.
   Maximum DC voltage on input pins may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27C64							Unit
JEDEC	Standard				-55	-70, -75	-90	-120	-150	-200	-255 -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.								ns
				Max.	55	70	90	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.								ns
				Max.	55	70	90	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.								ns
				Max.	35	40	40	50	65	75	100	
t_{EHZQ}, t_{GHQZ}	t_{DF}	Output Enable HIGH to Output Float (Note 2)		Min.								ns
				Max.	25	25	25	30	30	30	30	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	0	0	ns
				Max.								

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27C64 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. For the -55, -70, and -75:

   Output Load: 1 TTL gate and C_L = 30 pF,

   Input Rise and Fall Times: 20 ns,

   Input Pulse Levels: 0 to 3 V,

   Timing Measurement Reference Level: 1.5 V for inputs and outputs.

For all other versions:

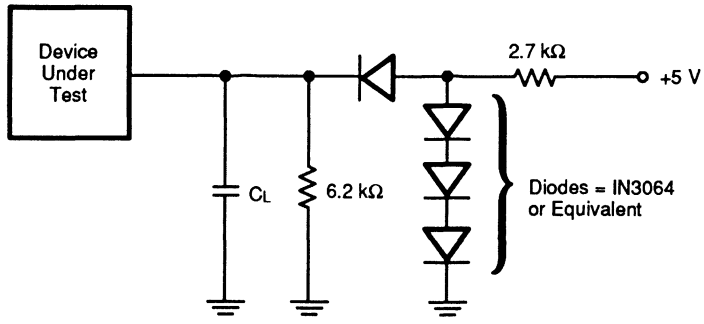
Output Load: 1 TTL gate and CL = 100 pF,

Input Rise and Fall Times: 20 ns,

Input Pulse Levels: 0.45 to 2.4 V,

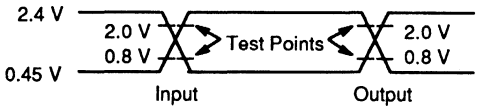
Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs.

SWITCHING TEST CIRCUIT

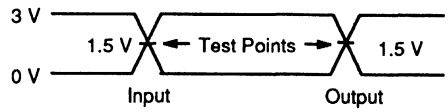


C_L = 100 pF including jig capacitance (30 pF for -55, -70, and -75)

SWITCHING TEST WAVEFORMS



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



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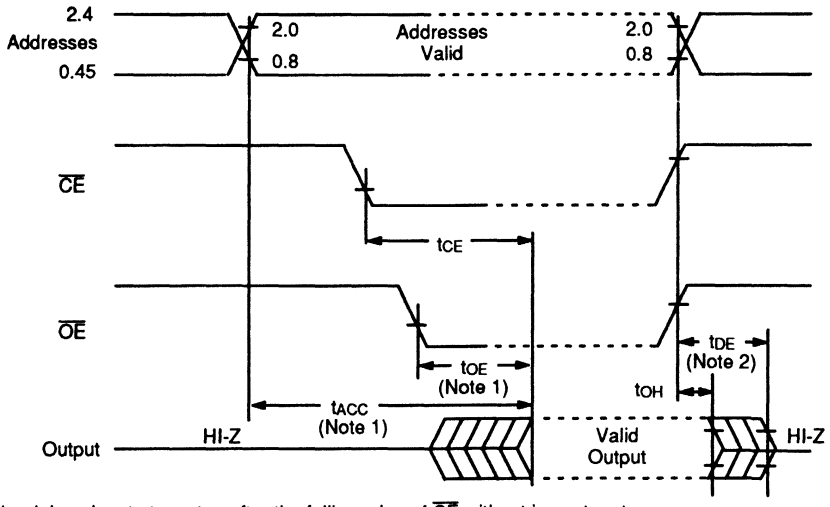
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for -55, -70, and -75 devices.

SWITCHING WAVEFORMS

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010



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Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING FLOW CHART

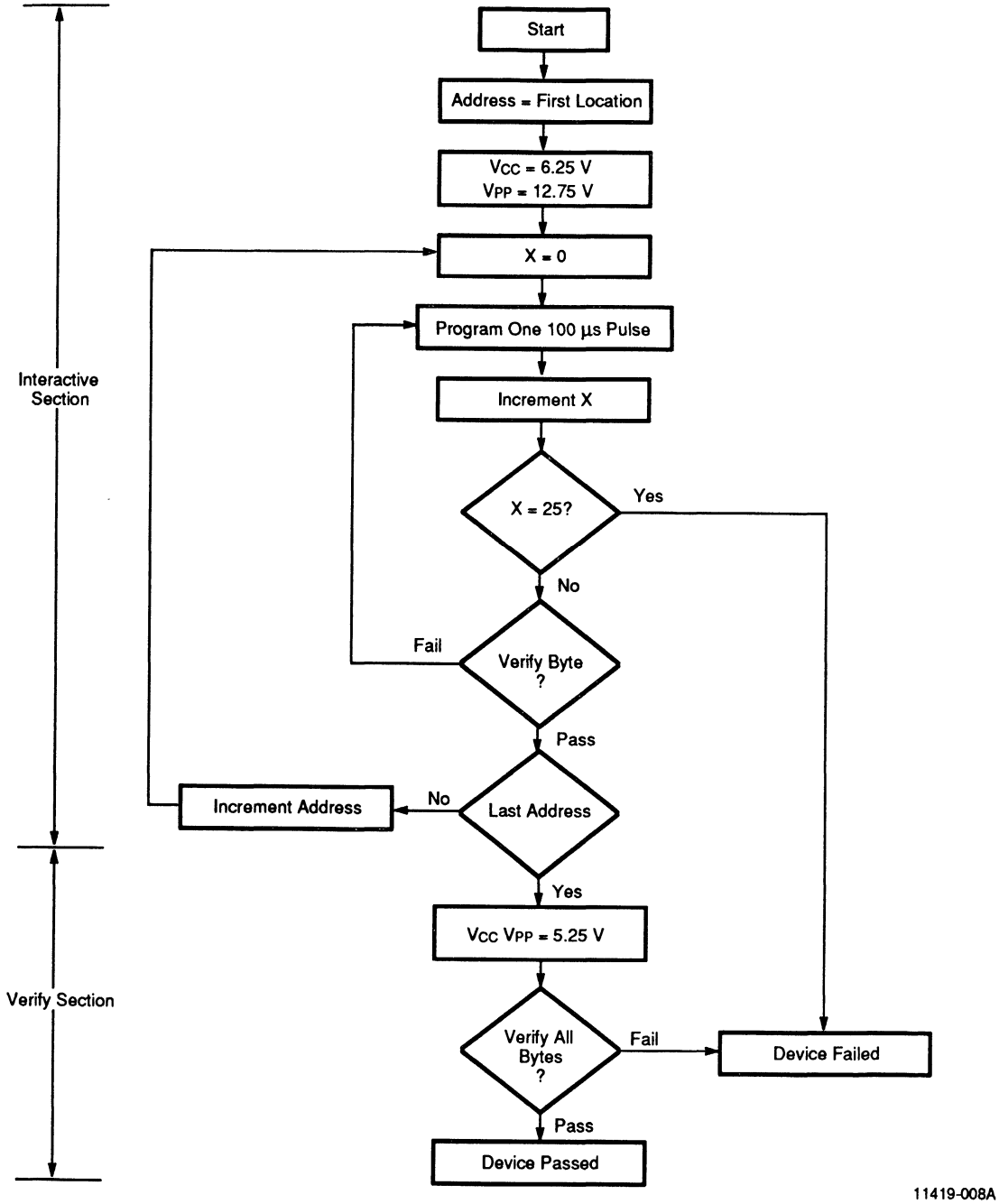


Figure 1. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.3	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC3}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

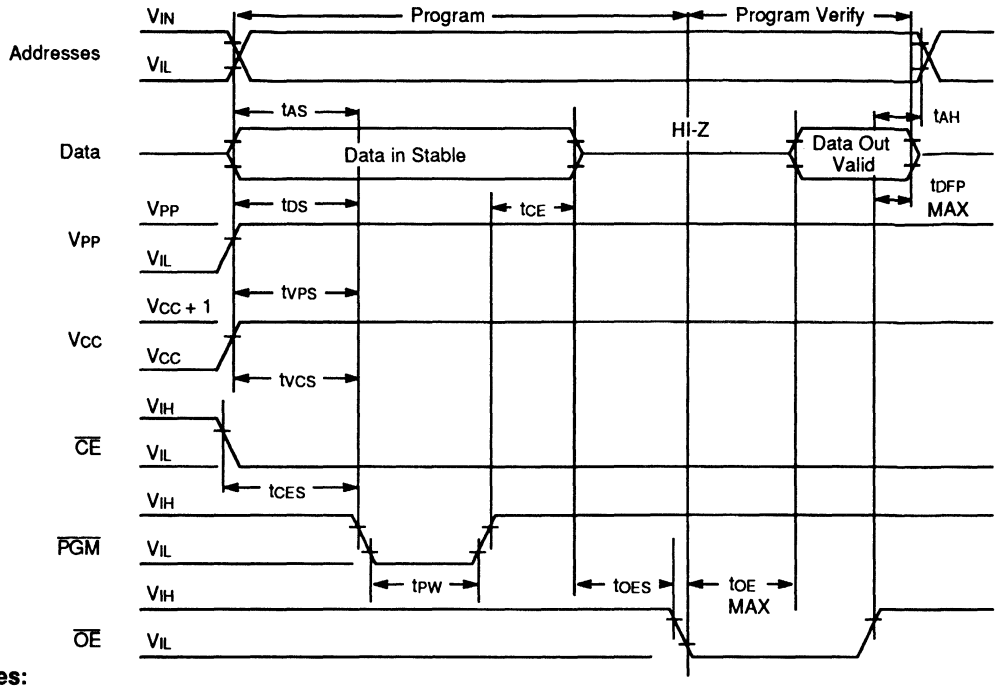
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	100	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		100	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C64, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

PROGRAMMING ALGORITHM WAVEFORMS (Notes 1 & 2)



Notes:

1. The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

Am27C128

16,384 x 8-Bit CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time–55 ns**
- **Low power consumption: –100 µA maximum standby current**
- **Programming voltage: 12.75 V**
- **Single +5 -V power supply**
- **JEDEC–approved pinout**
- **±10% power supply tolerance**
- **Fast Flashrite™ programming**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**

GENERAL DESCRIPTION

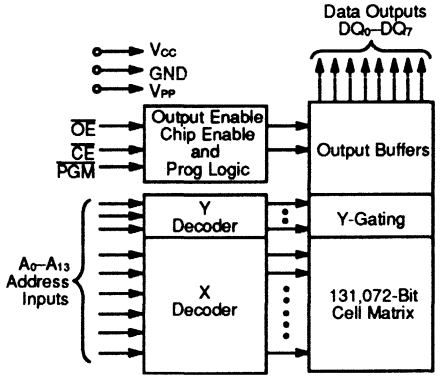
The Am27C128 is a 128K-bit, ultraviolet erasable programmable read-only memory. It is organized as 16,384 words by 8 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

Typically, any byte can be accessed in less than 55 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C128 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random.

BLOCK DIAGRAM



11420-001A

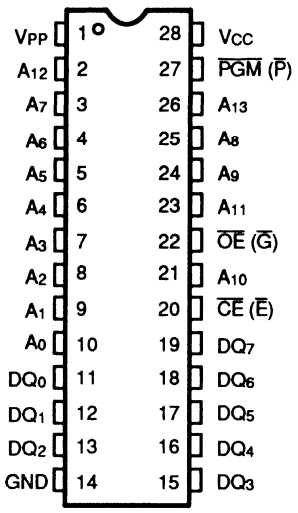
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C128						
Ordering Part Number ±5% Vcc Tolerance	-55	-75					-255
±10% Vcc Tolerance	–	-70	-90	-120	-150	-200	-250
Max. Access Time (ns)	55	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	55	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	40	40	50	65	75	100

CONNECTION DIAGRAMS

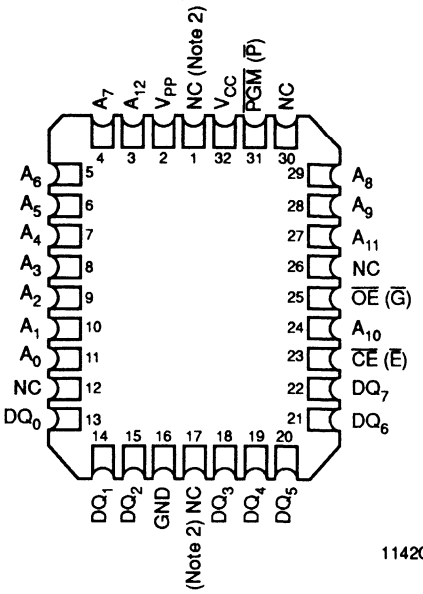
Top View

DIP



11420-002A

LCC*



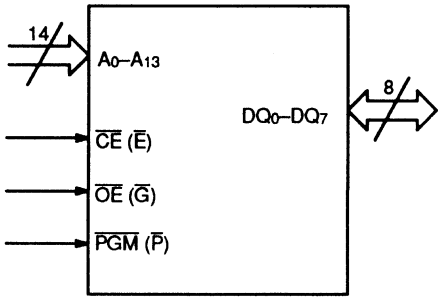
11420-003A

* Also Available in a 32-pin rectangular plastic leaded chip carrier

Notes:

1. JEDEC nomenclature is in parantheses.
2. Don't use (DU) for PLCC.

LOGIC SYMBOL



11420-004A

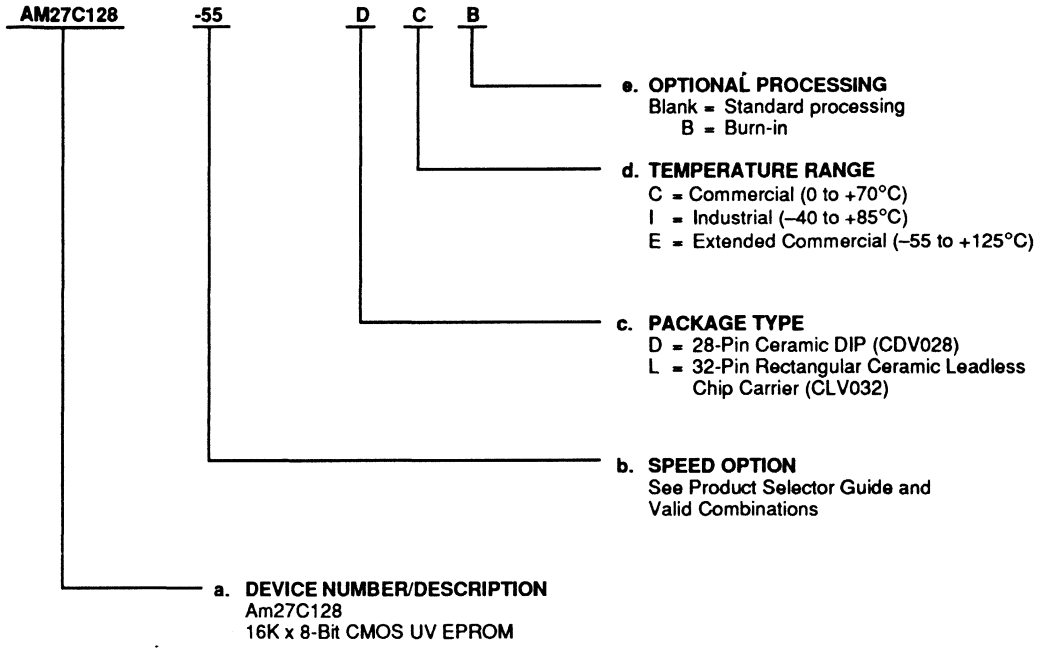
PIN DESCRIPTION

$A_0 - A_{13}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_7$	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27C128-55	DC, DCB, LC, LCB
AM27C128-70	
AM27C128-75	
AM27C128-90	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB,
AM27C128-120	
AM27C128-150	
AM27C128-200	
AM27C128-255	

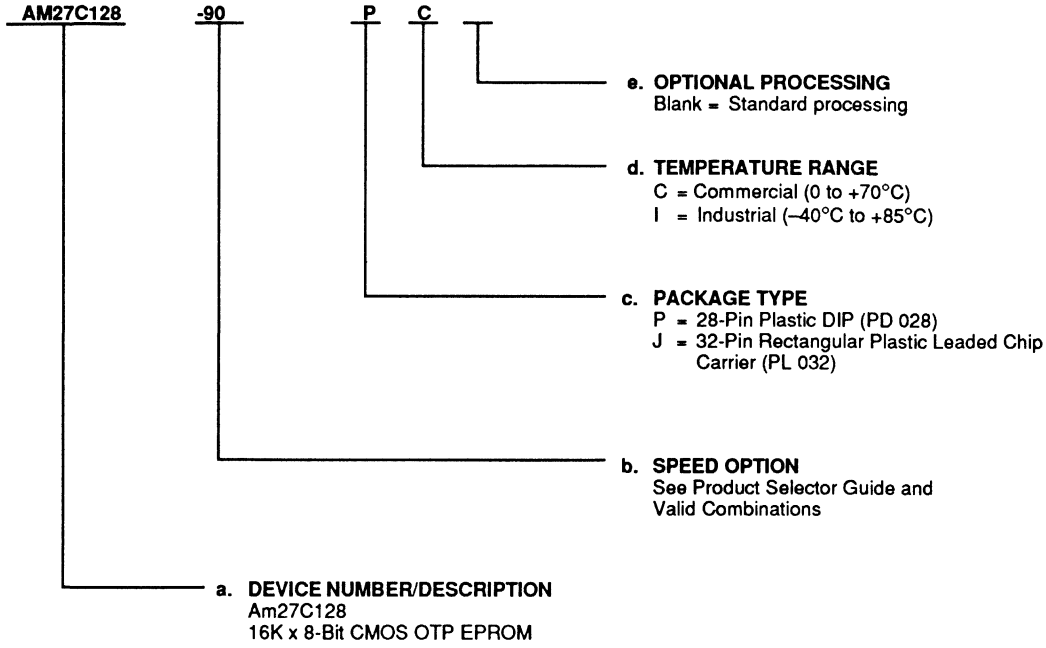
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27C128-90	JC, PC,
AM27C128-120	JC, PC, JI, PI
AM27C128-150	
AM27C128-200	
AM27C128-255	

Valid Combinations

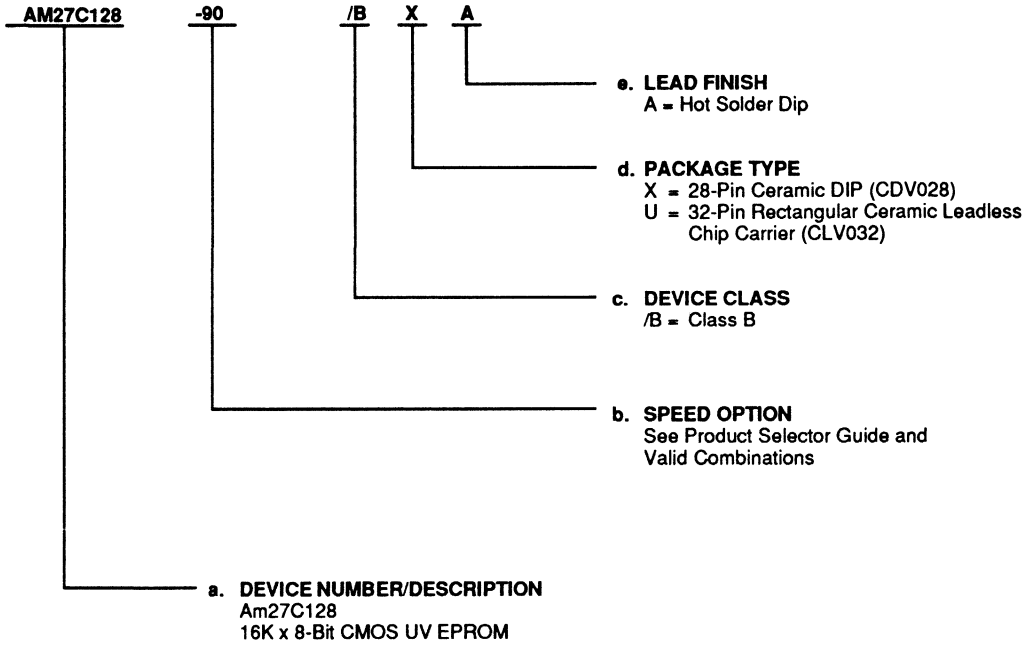
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Lead Finish



Valid Combinations	
AM27C128-90	/BXA, /BUA
AM27C128-120	
AM27C128-150	
AM27C128-200	
AM27C128-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C128

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C128 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C128. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Angstroms (Å)—with intensity of 12,000 µW/cm2 for 15 to 20 minutes. The Am27C128 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C128, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C128 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C128

Upon delivery, or after each erasure, the Am27C128 has all 131,072 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C128 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ is at V_{IL}, and $\overline{PGM}$ is at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite programming algorithm (shown in Figure 1) reduces programming time by using initial 100 µs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.25 V.

Program Inhibit

Programming of multiple Am27C128s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C128 may be common. A TTL low-level program pulse applied to an Am27C128 $\overline{PGM}$ input with V_{PP} = 12.75 ± 0.25 and $\overline{CE}$ LOW will program that Am27C128. A high-level $\overline{CE}$ input inhibits the other Am27C128s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}. $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmeed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C128.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C128. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A_0 = V_{IL}) represents the manufacturer code, and byte 1 (A_0 = V_{IH}), the device identifier code. For the Am27C128, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C128 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}—t_{OE}.

Standby Mode

The Am27C128 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C128 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL–standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high–impedance state, independent of the $\overline{OE}$ input.

Output OR–Tieing

To accomodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	V_{CC}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	V_{CC}	High Z
Standby (TTL)		V_{IH}	X	X	X	X	V_{CC}	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	V_{CC}	High Z
Program		V_{IL}	X	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto Select (Notes 3 & 4)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	V_{CC}	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	V_{CC}	16H

Notes:

1. X can be either V_{IL} or V_{IH}
2. $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$
3. A_1–$A_8 = A_{10}$–$A_{12} = V_{IL}$
4. $A_{13} = X$
4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	–65 to + 125°C
All Other Products	–65 to + 150°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC} (Note 1)	–0.6 to V_{CC} + 0.6 V
A_9 and V_{PP} (Note 2)	–0.6 to 13.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. During transitions the inputs may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0 to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	–40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (T_C)	–55 to +125°C
Military (M) Devices	
Case Temperature (T_C)	–55 to +125°C
Supply Read Voltages:	
V_{CC}/V_{PP} for Am27C128–XX5	+4.75 to +5.25 V
V_{CC}/V_{PP} for Am27C128–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		5	µA
			E/M Devices		10	
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		30	mA
			E/M Devices		30	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	C/I Devices		1.0	mA
			E/M Devices		1.0	
I_{PP1}	V_{PP} Supply Current (Read) (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

DC CHARACTERISTICS over operating range unless otherwise specified (Cont'd.)

CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			V_{CC} – 0.3	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		10	µA
			E/M Devices		10	
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = VIL, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		25	mA
			E/M Devices		25	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	C/I Devices		100	µA
			E/M Devices		120	
I_{PP1}	V_{PP} Supply Current (Read) (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	9	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27C128 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC voltage on output pins may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27C128							Unit
JEDEC	Standard				55	-70, -75	-90	-120	-150	-200	-255 -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.								ns
				Max.	55	70	90	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.								ns
				Max.	55	70	90	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.								ns
				Max.	35	40	40	50	65	75	100	
t_{EHQZ}, t_{GHQZ}	t_{DF}	Output Enable HIGH to Output Float (Note 2)		Min.								ns
				Max.	25	25	25	30	30	30	30	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	0	0	ns
				Max.								

Notes:

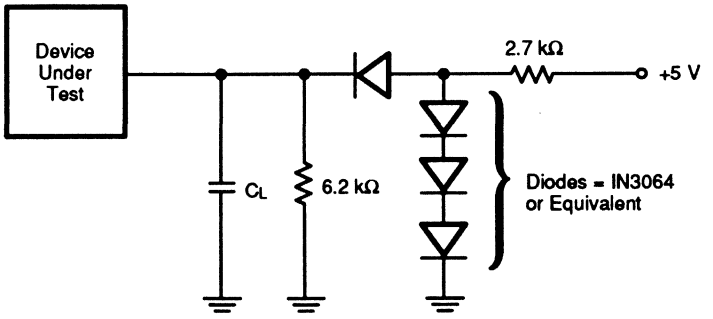
1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27C128 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. For the -55, -70, and -75:

   Output Load: 1 TTL gate and C_L = 30 pF,
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0 to 3 V,
   Timing Measurement Reference Level: 1.5 V for inputs and outputs.

For all other versions:

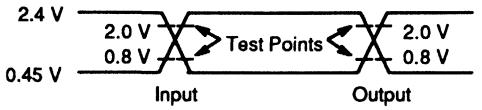
   Output Load: 1 TTL gate and CL = 100 pF,
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0.45 to 2.4 V,
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs.

SWITCHING TEST CIRCUIT

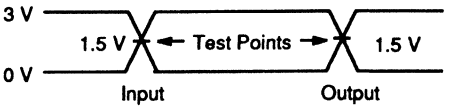


C_L = 100 pF including jig capacitance (30 pF for -55, -70, and -75)

SWITCHING TEST WAVEFORMS



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



11420-006A

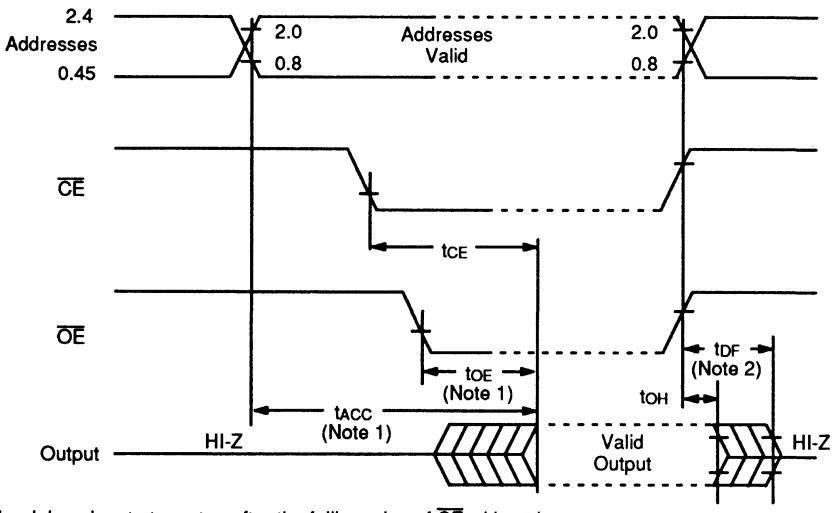
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for -55, -70, and –75 devices.

SWITCHING WAVEFORMS

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010



11419-007A

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

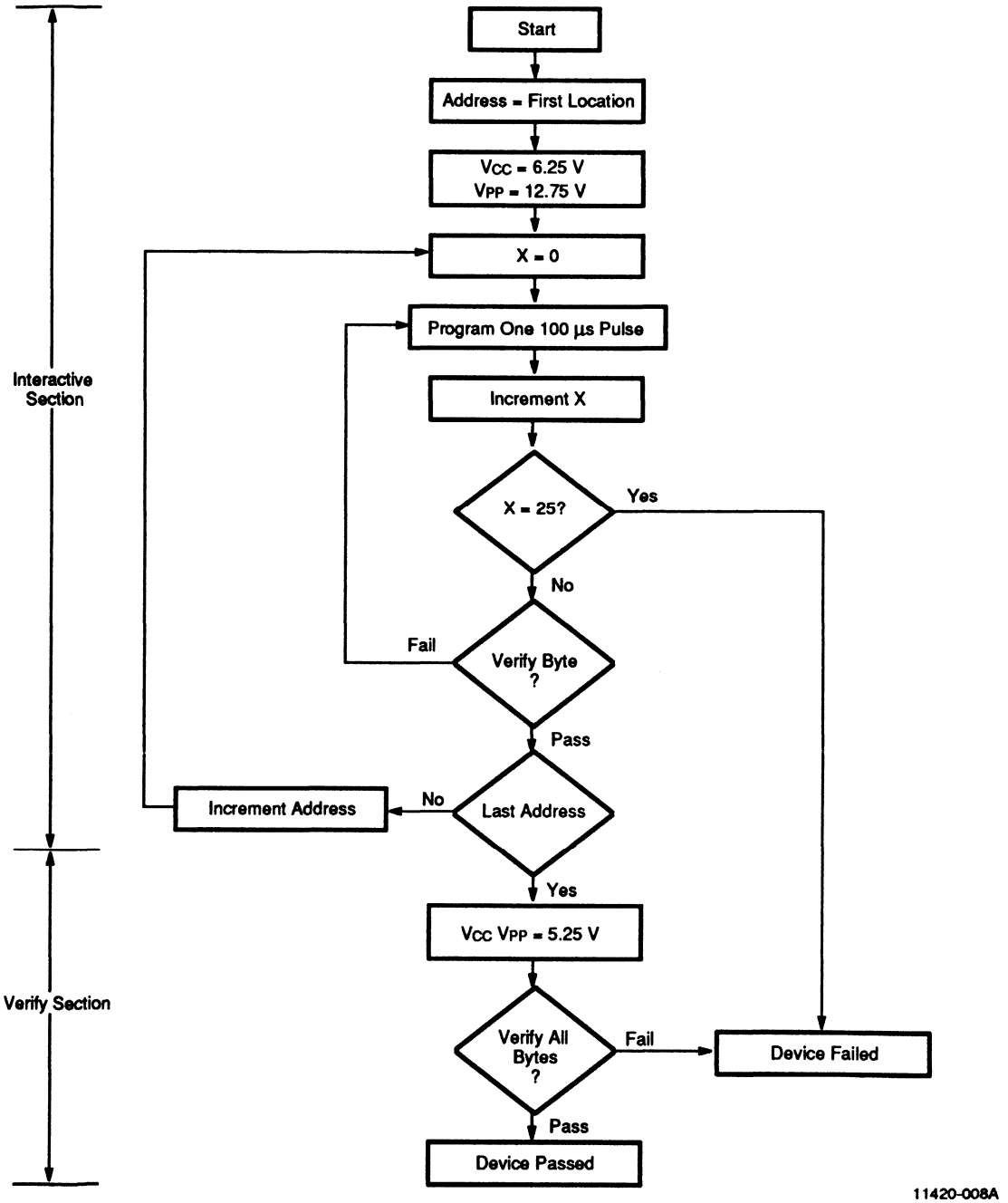


Figure 1. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.3	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

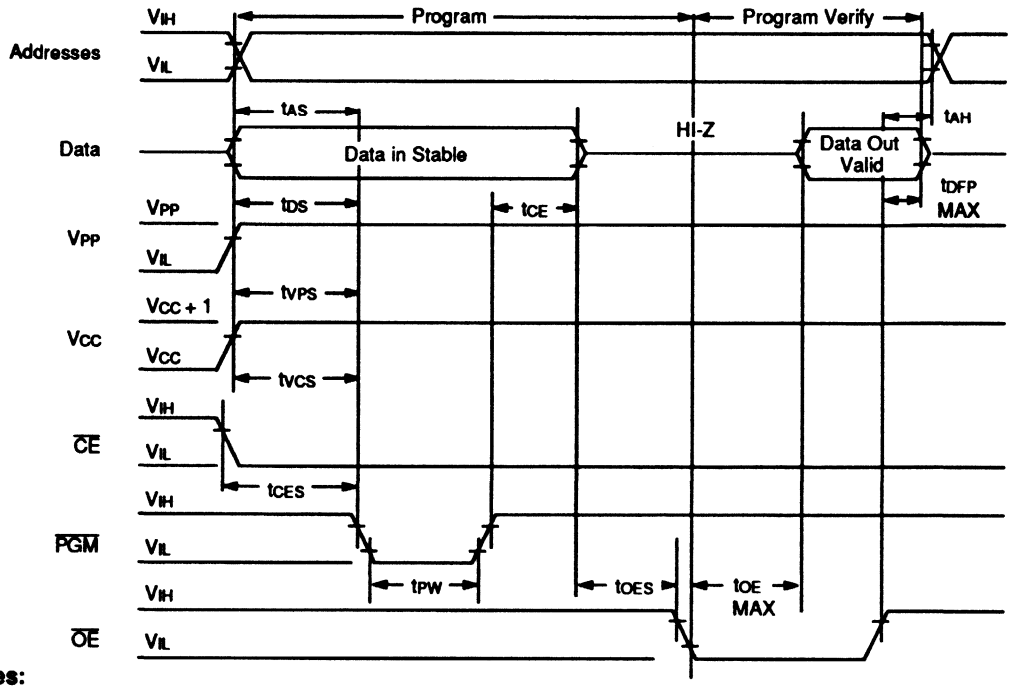
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbols		Parameter			
JEDEC	Standard	Description	Min.	Max.	Unit
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	100	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		100	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C128, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

PROGRAMMING ALGORITHM WAVEFORMS (NOTES 1 & 2)



Notes:

1. The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

11420-009A

Am27C256

32,768 x 8-Bit CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time–55 ns**
- **Low power consumption: –100 µA maximum standby current**
- **Programming voltage: 12.75 V**
- **Single +5 -V power supply**
- **JEDEC–approved pinout**
- **±10% power supply tolerance**
- **Fast Flashrite™ programming**
- **Latch–up protected to 100 mA from –1 V to Vcc +1 V**

GENERAL DESCRIPTION

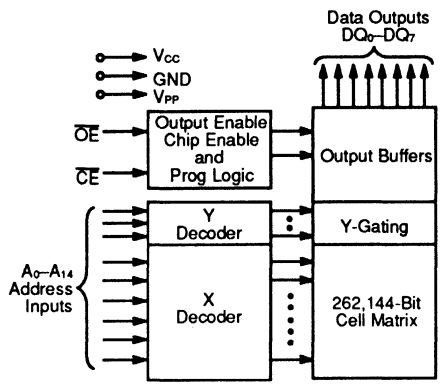
The Am27C256 is a 128K-bit, ultraviolet erasable programmable read-only memory. It is organized as 32,768 words by 8 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

Typically, any byte can be accessed in less than 55 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C256 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random.

BLOCK DIAGRAM



08007-001A

PRODUCT SELECTOR GUIDE

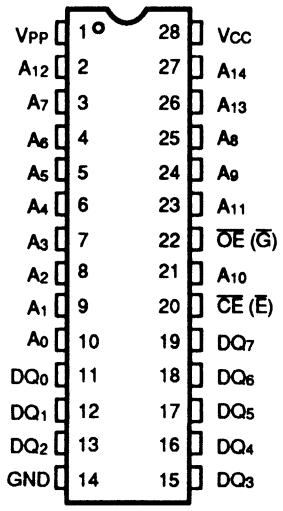
Family Part No.	Am27C256							
Ordering Part Number ±5% Vcc Tolerance	-55	-75						-255
±10% Vcc Tolerance	–	-70	-90	-100	-120	-150	-200	-250
Max. Access Time (ns)	55	70	90	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	55	70	90	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	40	40	40	50	65	75	100

Publication# 08007 Rev. F Amendment/0
Issue Date: March 1991

CONNECTION DIAGRAMS

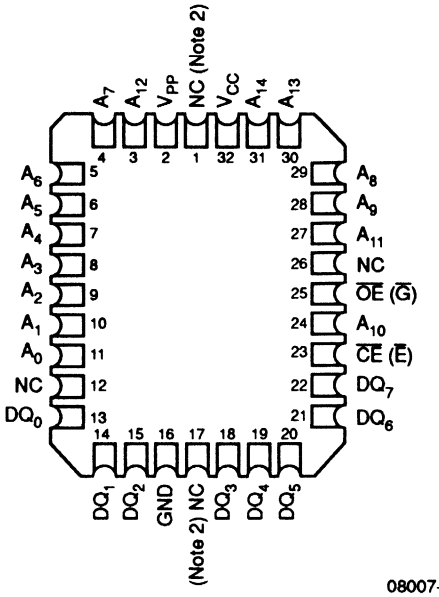
Top View

DIP



08007-002A

LCC*



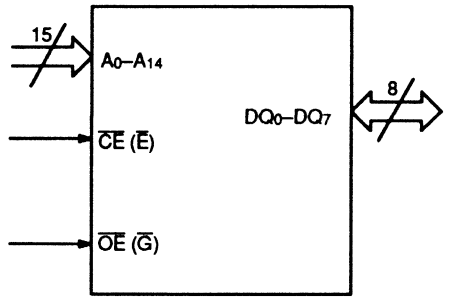
08007-003A

* Also Available in a 32-pin rectangular plastic leaded chip carrier

Notes:

1. JEDEC nomenclature is in parantheses.
2. Don't use (DU) for PLCC.

LOGIC SYMBOL



08007-004A

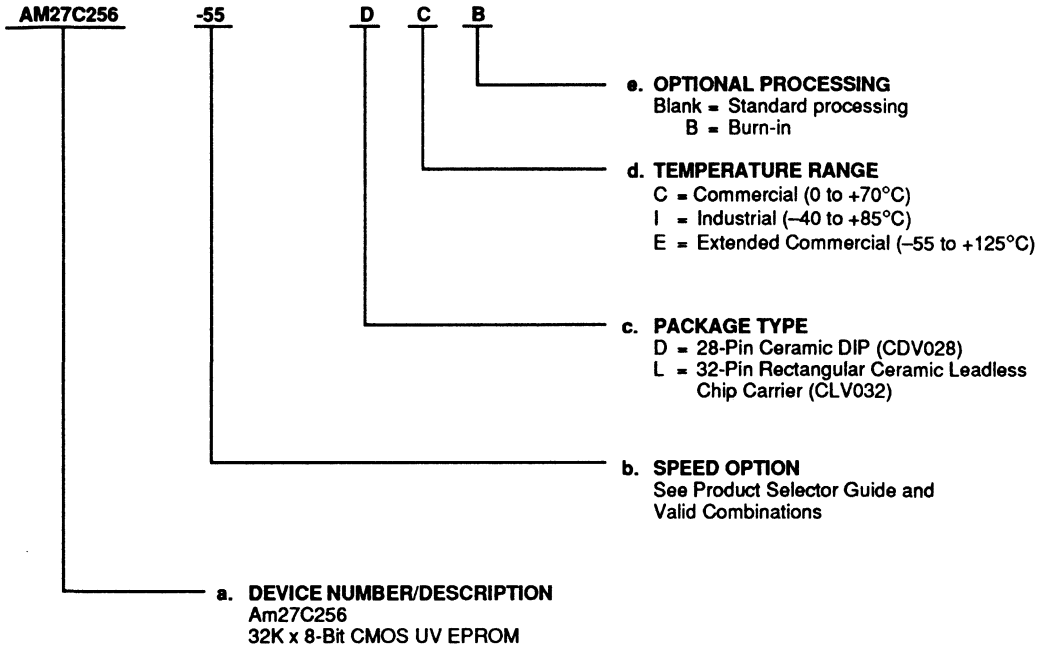
PIN DESCRIPTION

$A_0 - A_{14}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_7$	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27C256-55	DC, DCB, LC, LCB
AM27C256-70	
AM27C256-75	
AM27C256-90	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB,
AM27C256-100	
AM27C256-120	
AM27C256-150	
AM27C256-200	
AM27C256-255	

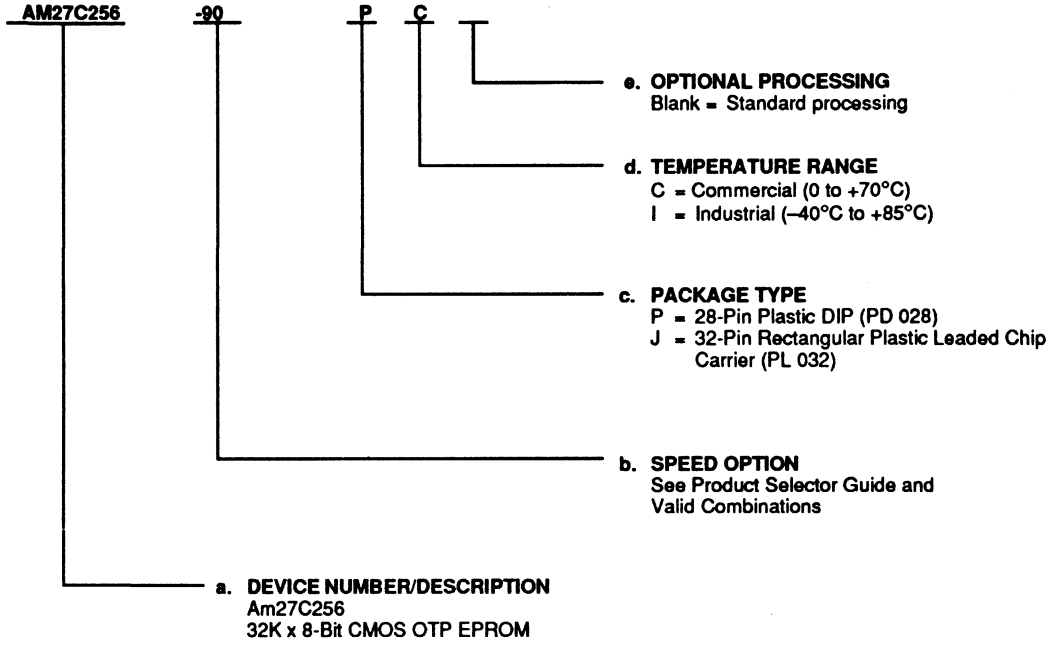
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C256-90	JC, PC
AM27C256-120	JC, PC, JI, PI
AM27C256-150	
AM27C256-200	
AM27C256-255	

Valid Combinations

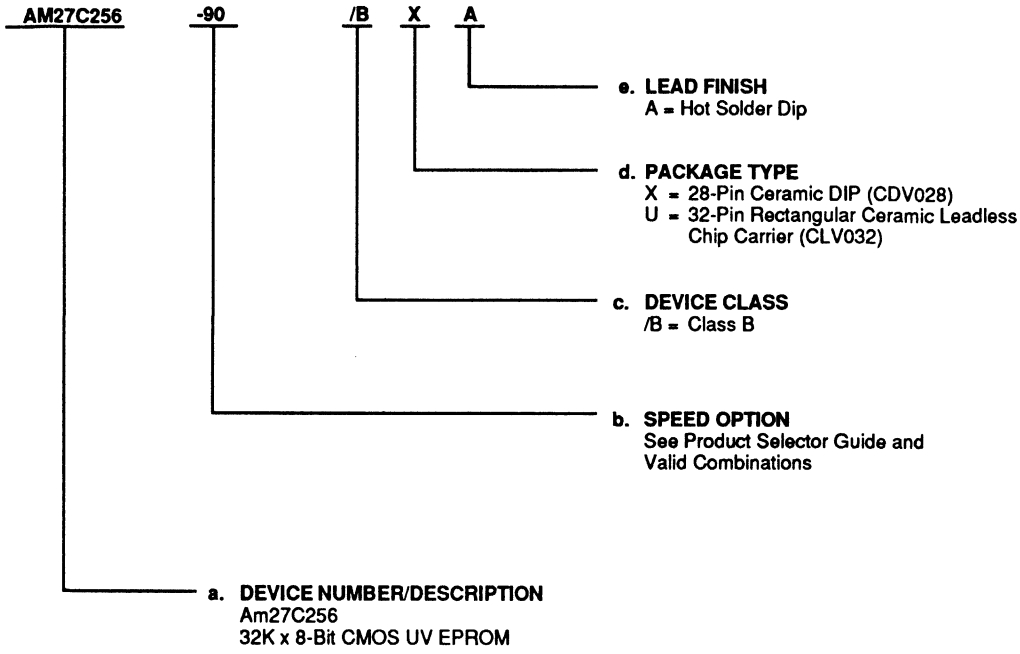
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Lead Finish



Valid Combinations	
AM27C256-90	/BXA, /BUA
AM27C256-100	
AM27C256-120	
AM27C256-150	
AM27C256-200	
AM27C256-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C256

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C256 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C256. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Angstroms (Å)—with intensity of 12,000 µW/cm_2 for 15 to 20 minutes. The Am27C256 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C256, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C256 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C256

Upon delivery, or after each erasure, the Am27C256 has all 262,144 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C256 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, $\overline{OE}$ is at V_{IH}, and $\overline{CE}$ is at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite programming algorithm (shown in Figure 2) reduces programming time by using initial 100 µs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the OTP EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.25 V.

Program Inhibit

Programming of multiple Am27C256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C256 may be common. A TTL low-level program pulse applied to an Am27C256 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 and $\overline{OE}$ HIGH will program that Am27C256. A high-level $\overline{CE}$ input inhibits the other Am27C256s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH}, and V_{PP} between 12.5 V to 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C256.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A_0 = V_{IL}) represents the manufacturer code, and byte 1 (A_0 = V_{IH}), the device identifier code. For the Am27C256, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}—t_{OE}.

Standby Mode

The Am27C256 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C256 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accomodate multiple memory connections, a two–line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	A_0	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	V_{CC}	High Z
Standby (TTL)		V_{IH}	X	X	X	V_{CC}	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	V_{CC}	High Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	High Z
Auto Select (Notes 3 & 4)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	V_{CC}	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	10H

Notes:

1. X can be either V_{IL} or V_{IH}
2. $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$
3. A_1–$A_8 = A_{10}$–$A_{12} = V_{IL}$
4. A_{13} and A_{14} = X
5. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	–65 to + 125°C
All Other Products	–65 to + 150°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC} (Note 1)	–0.6 to V_{CC} + 0.6 V
A_9 and V_{PP} (Note 2)	–0.6 to 13.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. During transitions the inputs may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (Tc)	0 to +70°C
Industrial (I) Devices	
Case Temperature (Tc)	–40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (Tc)	–55 to +125°C
Military (M) Devices	
Case Temperature (Tc)	–55 to +125°C
Supply Read Voltages:	
V_{CC}/V_{PP} for Am27C256–XX5	+4.75 to +5.25 V
V_{CC}/V_{PP} for Am27C256–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		10	µA
			E/M Devices		10	
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = VIL, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		30	mA
			E/M Devices		50	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	C/I Devices		1.0	mA
			E/M Devices		1.0	
I_{PP1}	V_{PP} Supply Current (Read) (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

DC CHARACTERISTICS over operating range unless otherwise specified (Continued)

CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			V_{CC} – 0.3	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		10	µA
			E/M Devices		10	
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = VIL, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		25	mA
			E/M Devices		25	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	C/I Devices		100	µA
			E/M Devices		120	
I_{PP1}	V_{PP} Supply Current (Read) (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	9	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27C256 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC voltage on output pins may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27C256							Unit
JEDEC	Standard				-55	-70, -75	-90	-120	-150	-200	-255, -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.								ns
				Max.	55	70	90	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.								ns
				Max.	55	70	90	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.								ns
				Max.	35	40	40	50	65	75	100	
t_{EHZQ}, t_{GHQZ}	t_{DF}	Output Enable HIGH to Output Float (Note 2)		Min.								ns
				Max.	25	25	25	30	30	30	30	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	0	0	ns
				Max.								

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27C256 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. For the -55, -70, and -75:

   Output Load: 1 TTL gate and C_L = 30 pF,

   Input Rise and Fall Times: 20 ns,

   Input Pulse Levels: 0 to 3 V,

   Timing Measurement Reference Level: 1.5 V for inputs and outputs.

For all other versions:

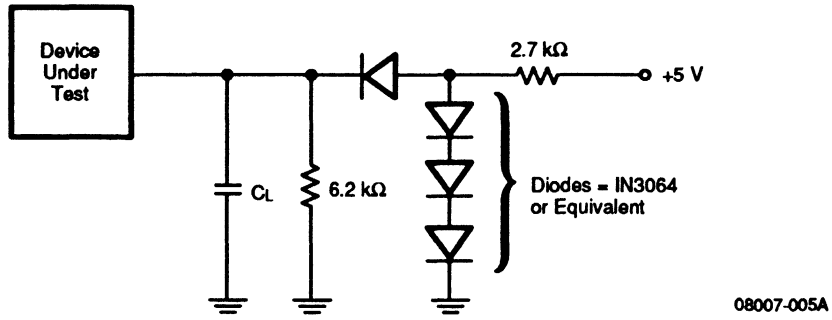
Output Load: 1 TTL gate and C_L = 100 pF,

Input Rise and Fall Times: 20 ns,

Input Pulse Levels: 0.45 to 2.4 V,

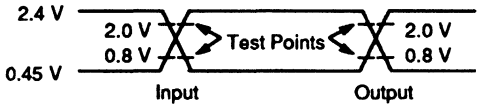
Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs.

SWITCHING TEST CIRCUIT

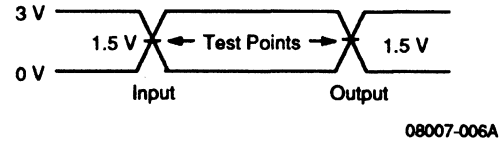


C_L = 100 pF including jig capacitance (30 pF for –55, –70, and –75)

SWITCHING TEST WAVEFORMS



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



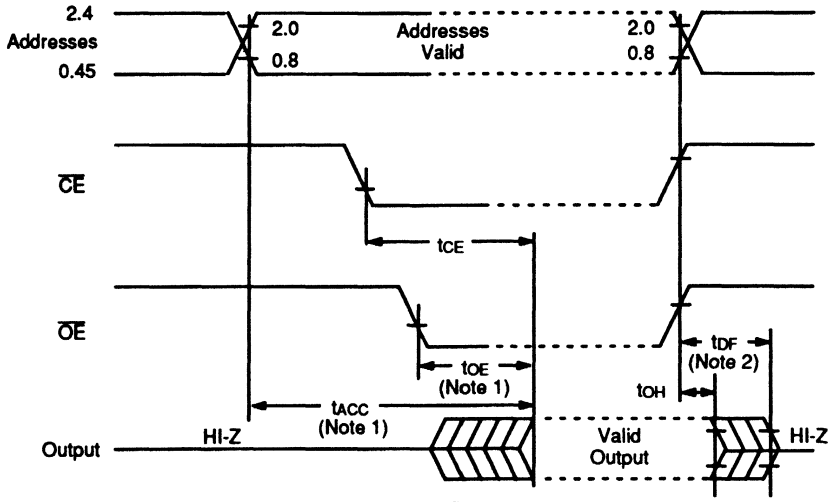
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for –55, –70, and –75 devices.

SWITCHING WAVEFORMS

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010



08007-007A

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

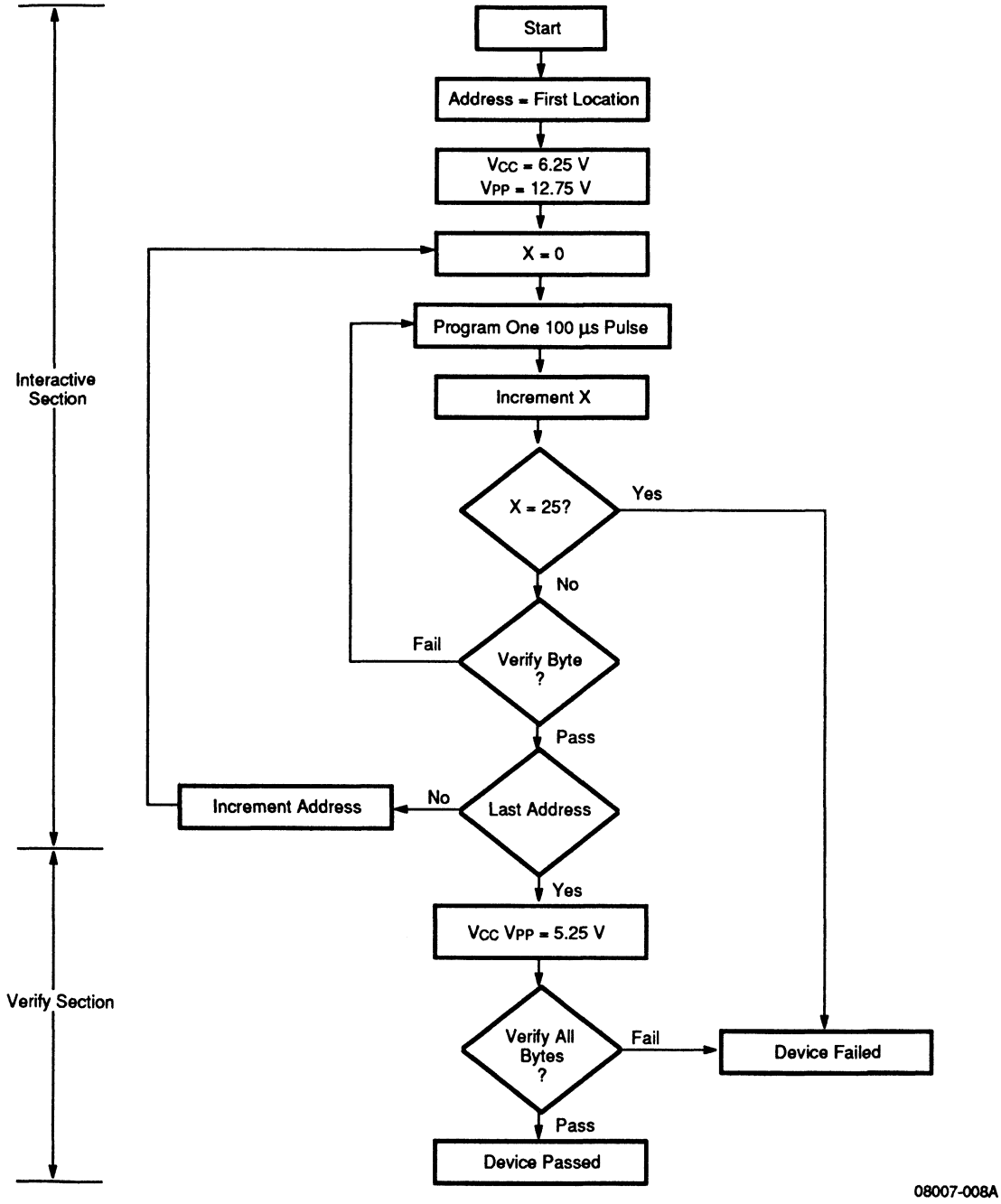


Figure 1. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.3	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

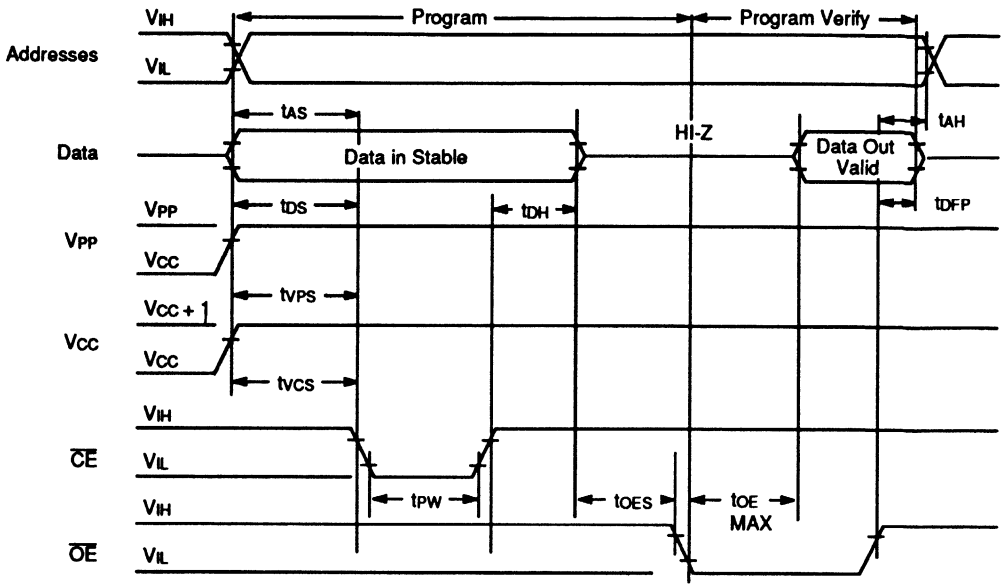
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	100	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH}	t_{PW}	$\overline{CE}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		100	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C256, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

PROGRAMMING ALGORITHM WAVEFORMS (Notes 1 & 2)



08007-009A

Notes:

1. The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

Am27H256

32,768 x 8-Bit High Speed CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Industry's fastest**
  - -35ns 256K-bit CMOS EPROM
- **Pin compatible with Am27C256**
- **High speed Flashrite™ programming**
  - -Typically less than 5 seconds
- **Versions available in industrial and military temperature ranges**
- **± 10% power supply tolerance available**

GENERAL DESCRIPTION

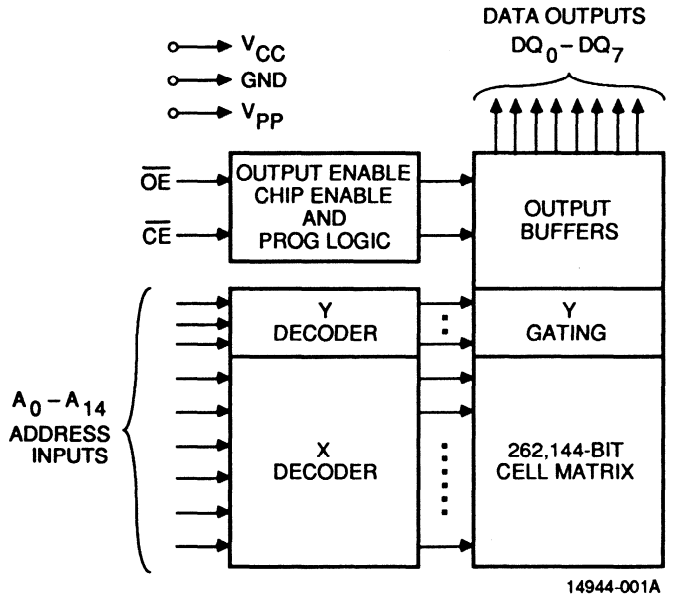
The Am27H256 is an ultra-high speed 256K-bit CMOS UV EPROM. It utilizes the standard JEDEC pinout making it functionally compatible with the Am27C256, but with significantly faster access capability. This superior random access capability results from a focused high-speed design implemented with AMD's advanced CMOS process technology. This offers users bipolar speeds with higher density, lower cost and proven reliability.

This device is ideal for use with the fastest processors. At 35ns, the Am27H256 completely eliminates performance-draining wait states without using bank-interleaving and caching techniques. Designers may take full advantage of high speed digital signal processors and microprocessors by allowing code to be executed at full speed directly out of EPROM. Typical applications include laser printers, switching networks, graphics, workstations and digital signal processing.

The Am27H256 supports AMD's Flashrite programming algorithm which allows the entire chip to be programmed in typically less than 5 seconds.

It is available in DIP as well as surface mount packages and is offered in commercial, industrial, and extended temperature ranges.

BLOCK DIAGRAM



14944-001A

Publication# 14944 Rev. B Amendment /0
Issue Date: March 1991

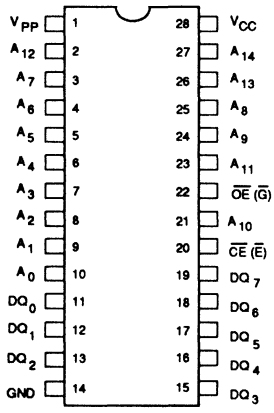
PRODUCT SELECTOR GUIDE

Family Part No.	Am27H256			
Ordering Part No:				
V_{CC} ± 5%	-35V05	–	–	–
V_{CC} ± 10%	-35	-45	-55	-70
Max. Access Time (ns)	35	45	55	70
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	35	45	55	70
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	20	20	25	35

CONNECTION DIAGRAMS

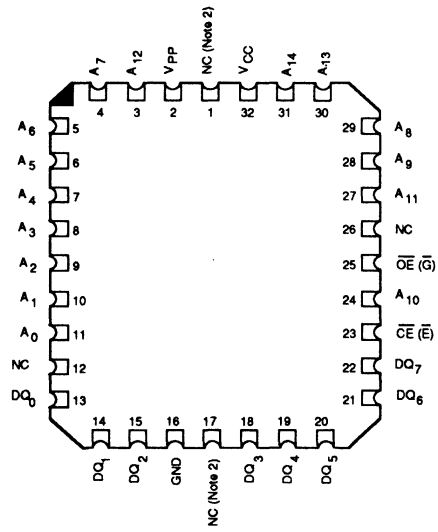
Top View

DIPs



14944-002A

LCC*



14944-003A

Notes:

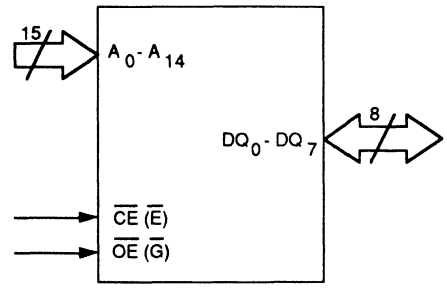
1. JEDEC nomenclature is in parentheses.
2. Don't Use (DU) for PLCC.

* Also available in 32-pin rectangular plastic leaded chip carrier

PIN DESCRIPTION

A_0– A_{14}	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ_0– DQ_7	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connection

LOGIC SYMBOL

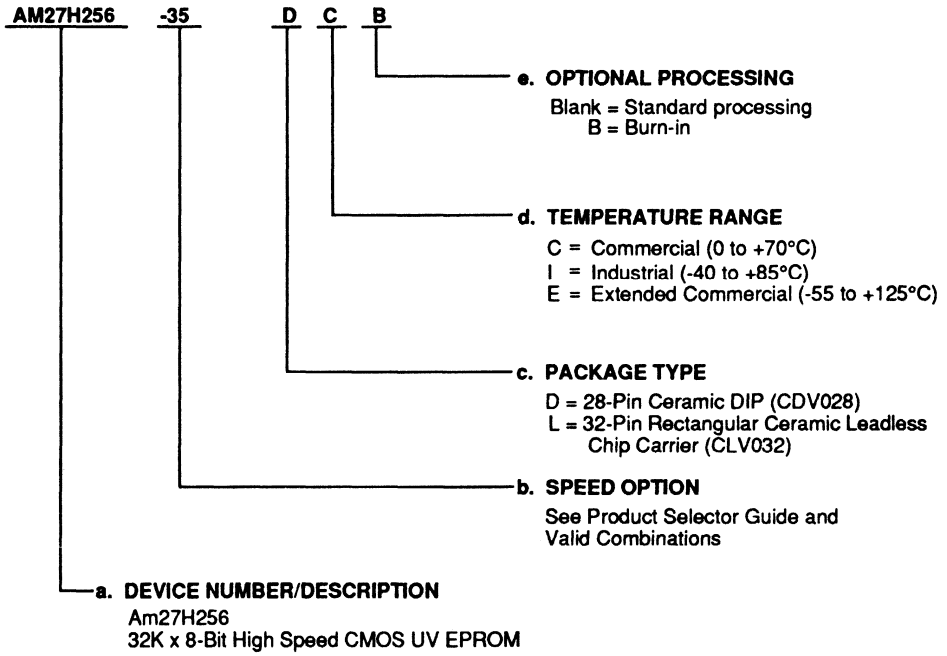


14944-004A

ORDERING INFORMATION
Standard Information

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27H256-35	DC, DCB, DI, DIB, LC, LI, LCB, LIB
AM27H256-35V05	
AM27H256-45	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27H256-55	
AM27H256-70	

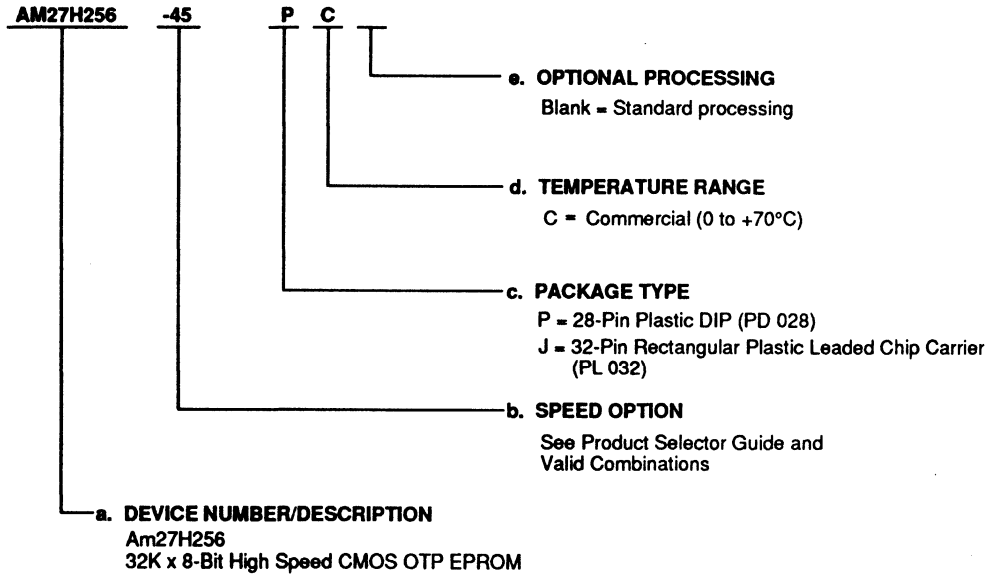
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations.

ORDERING INFORMATION (Cont'd.)
OTP Products (Preliminary)

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27H256-45	PC, JC
AM27H256-55	
AM27H256-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations.

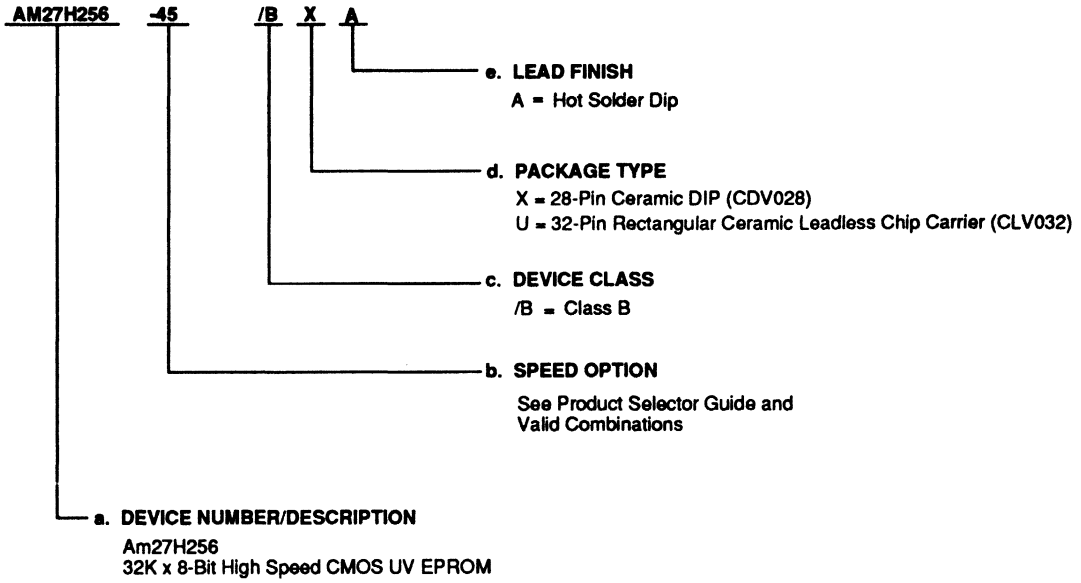
ORDERING INFORMATION (Cont'd.)

APL Products

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27H256-45	/BXA, /BUA
AM27H256-55	
AM27H256-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27H256

In order to clear all locations of their programmed contents, it is necessary to expose the Am27H256 to an ultraviolet light source. A dosage of 15 W seconds/cm² is required to completely erase an Am27H256. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Angstroms (Å)—with intensity of 12,000 μW/cm² for 15 to 20 minutes. The Am27H256 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27H256, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27H256 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27H256

Upon delivery, or after each erasure, the Am27H256 has all bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27H256 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ is at V_{IL}, and $\overline{OE}$ is at V_{IH}. For programming, the data to be programmed is applied 8 bits in parallel to the data input/output pins.

The Flashrite programming algorithm reduces programming time by using initial 100 μs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with $V_{CC} = V_{PP}$ = 5.25 V.

Program Inhibit

Programming of multiple Am27H256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27H256 may be common. A TTL low-level program pulse applied to an Am27H256 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V and $\overline{OE}$ HIGH will program that Am27H256. A high-level $\overline{CE}$ input inhibits the other Am27H256 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} between 12.5 V to 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27H256.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27H256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and byte 1($A_0 = V_{IH}$), the device identifier code. For the Am27H256, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27H256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27H256 has a standby mode which reduces the maximum V_{CC} current to 50% of the active current. It is placed in standby mode when $\overline{CE}$ is at V_{IH}. The amount of current drawn in standby mode depends on the frequency and the number of address pins switching. The Am27H256 is specified with 50% of the address lines toggling at 10 MHz. A reduction of the frequency or quantity of address lines toggling will significantly reduce the actual standby current.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in

their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	A_9	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	V_{CC}	Hi-Z
Standby		V_{IH}	X	X	X	V_{CC}	Hi-Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	Hi-Z
Auto Select	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	V_{CC}	01H
(Note 3 & 5)	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	10H

Notes:

1. V_H = 12.0 V ± 0.5 V
2. X = Either V_{IH} or V_{IL}
3. $A_1 - A_8 = A_{10} - A_{14} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.
5. The Am27H256 uses the same Flashrite algorithm during program as the Am27C256.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
OTP product	–65 to 125°C
All other products	–65 to 150°C
Ambient Temperature	
with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC}	–0.6 to V_{CC} +0.5 V
A_9 and V_{PP}	–0.6 to 13.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. Minimum DC voltage on input or I/O is –0.5 V. During transitions, the inputs may overshoot GND to –2.0V for periods of up to 10 ns. Maximum DC voltage on input and I/O is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.
2. For A_9 and V_{PP} the minimum DC input is –0.5 V. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 10 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0 to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	–40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (T_C)	–55 to +125°C
Military (M) Devices	
Case Temperature (T_C)	–55 to +125°C
Supply Read Voltages:	
V_{CC} for Am27H256-XXV05	+4.75 to + 5.25 V
V_{CC} for Am27H256-XX	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 4, 5, & 8) (for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -4 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA			0.45	V
V_{IH}	Input HIGH Voltage (Note 9)			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage (Note 9)			– 0.3	+ 0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to + V_{CC}			1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to + V_{CC}			10	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA (Open Outputs)	C Devices		50	mA
			I/E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}	C Devices		25	mA
			I/E/M Devices		35	
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Capacitance (Notes 2, 3, and 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV028		CLV032		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	6	10	6	9	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	10	12	7	9	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	10	10	7	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	6	9	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled, not 100% tested.
4. **Caution:** the Am27H256 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = +25°C, f = 1 MHz.
8. Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 10 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods less than10 ns.
9. Tested under static DC conditions.

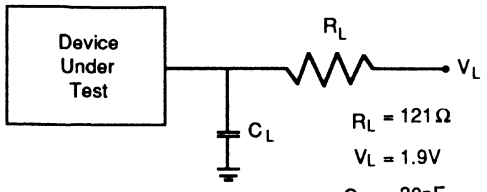
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3, & 4) (for APL Products, Group A, Subgroups 9, 10, and 11 are specified unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27H256				Unit
JEDEC	Standard				-35, -35V05	-45	-55	-70	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$, $C_L = C_{L1}$	Min.	–	–	–	–	ns
				Max.	35	45	55	70	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$, $C_L = C_{L1}$	Min.	–	–	–	–	ns
				Max.	35	45	55	70	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$, $C_L = C_{L1}$	Min.	–	–	–	–	ns
				Max.	20	20	25	35	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, Whichever Comes First, to Output Float	$C_L = C_{L2}$	Min.	0	0	0	0	ns
				Max.	20	20	25	35	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, Whichever Occured First		Min.	0	0	0	0	ns
				Max.	–	–	–	–	

Notes:

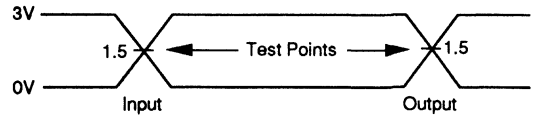
1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled, not 100% tested.
3. **Caution:** The Am27H256 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and C = C_L
   Input Rise and Fall Times: 5 ns
   Input Pulse Levels: 0 to 3 V
   Timing Measurement Reference Level – 1.5 V for inputs and outputs

SWITCHING TEST CIRCUIT



12750-004A

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤5 ns.

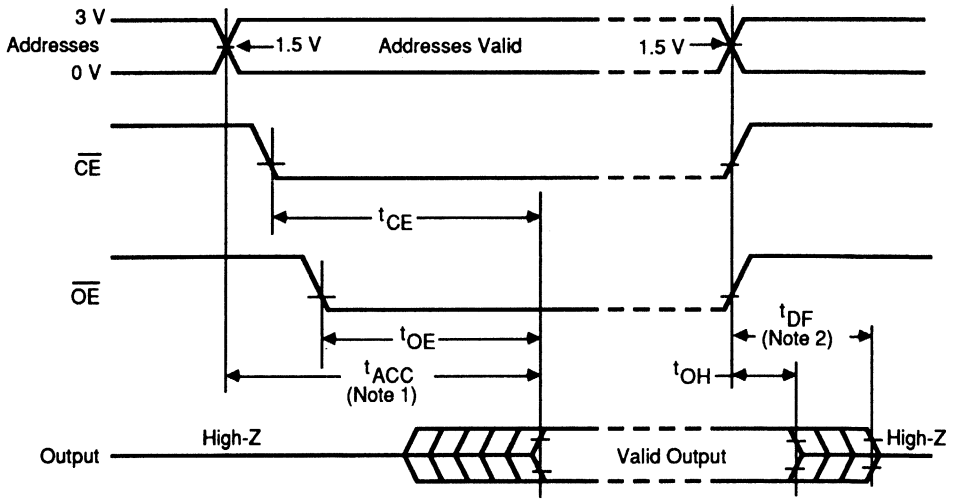
12750-005A

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



12750-006A

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Am27C512

65,536 x 8-Bit CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time—70ns**
- **Low power consumption: –100 µA maximum standby current**
- **Programming voltage: 12.75 V**
- **Single +5 -V power supply**
- **JEDEC–approved pinout**
- **±10% power supply tolerance**
- **Fast Flashrite™ programming**
- **Latch–up protected to 100 mA from –1 V to Vcc +1 V**

GENERAL DESCRIPTION

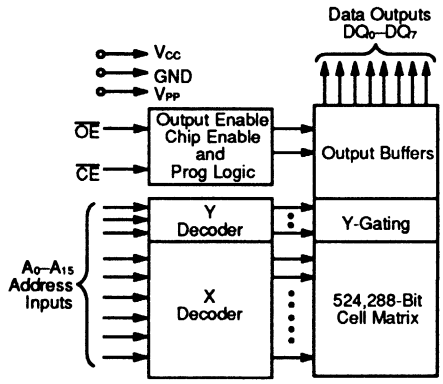
The Am27C512 is a 512K-bit, ultraviolet erasable programmable read-only memory. It is organized as 65,536 words by 8 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

Typically, any byte can be accessed in less than 70 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C512 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random.

BLOCK DIAGRAM



08140-001A

PRODUCT SELECTOR GUIDE

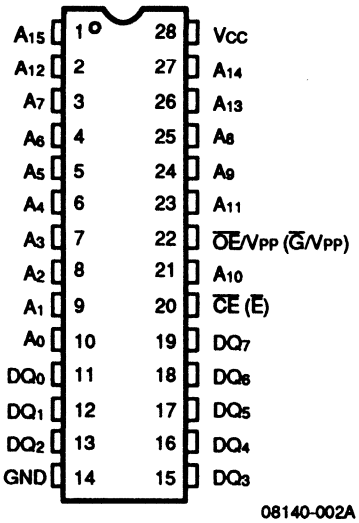
Family Part No.	Am27C512					
Ordering Part Number ±5% Vcc Tolerance	-75	-95	-125			-255
±10% Vcc Tolerance	–	-90	-120	-150	-200	-250
Max. Access Time (ns)	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	40	50	50	75	100

Publication# 08140 Rev. F Amendment/0
Issue Date: March 1991

CONNECTION DIAGRAMS

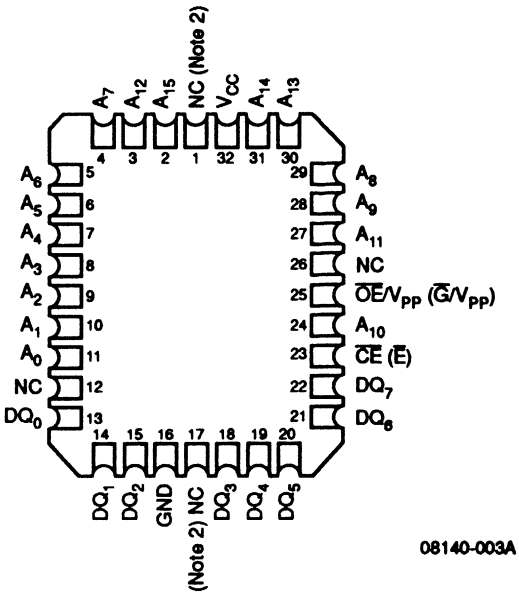
Top View

DIP



08140-002A

LCC*



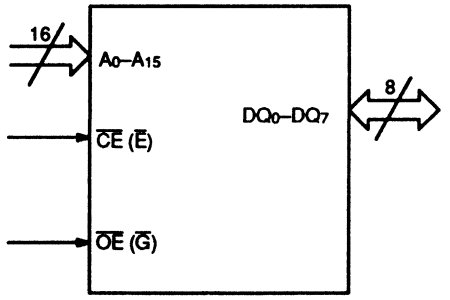
08140-003A

* Also Available in a 32-pin rectangular plastic leaded chip carrier

Notes:

1. JEDEC nomenclature is in parantheses.
2. Don't use (DU) for PLCC.

LOGIC SYMBOL



08140-004A

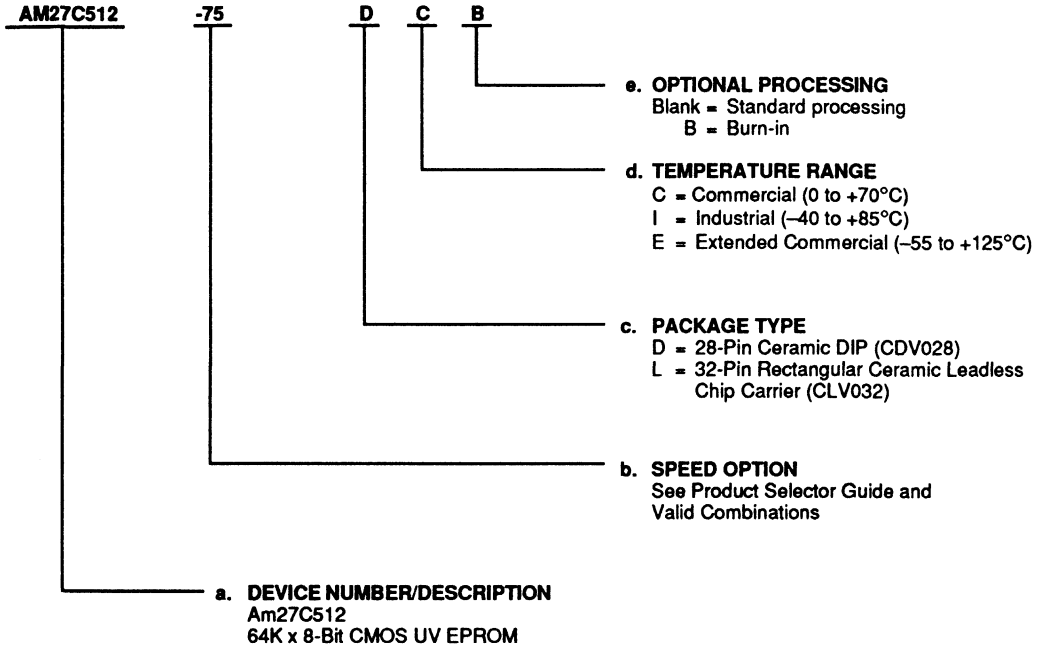
PIN DESCRIPTION

$A_0 - A_{15}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_7$	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27C512-75	DC, DCB, LC, LCB
AM27C512-95	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C512-125	
AM27C512-90	
AM27C512-120	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM27C512-150	
AM27C512-200	
AM27C512-255	

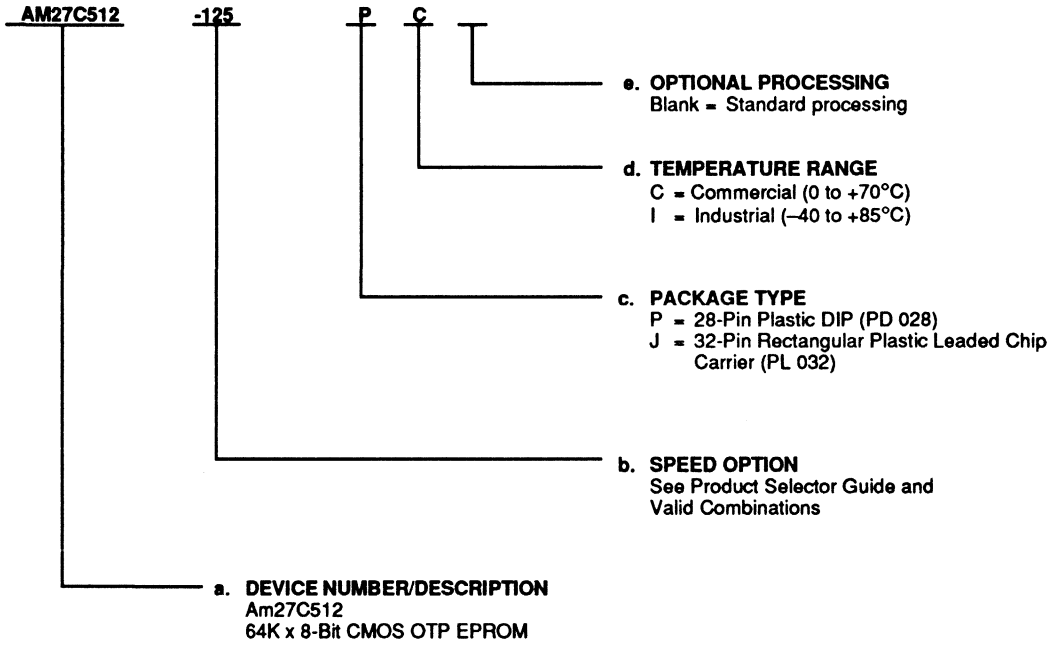
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C512-120	JC, PC, JI, PI
AM27C512-150	
AM27C512-200	
AM27C512-255	

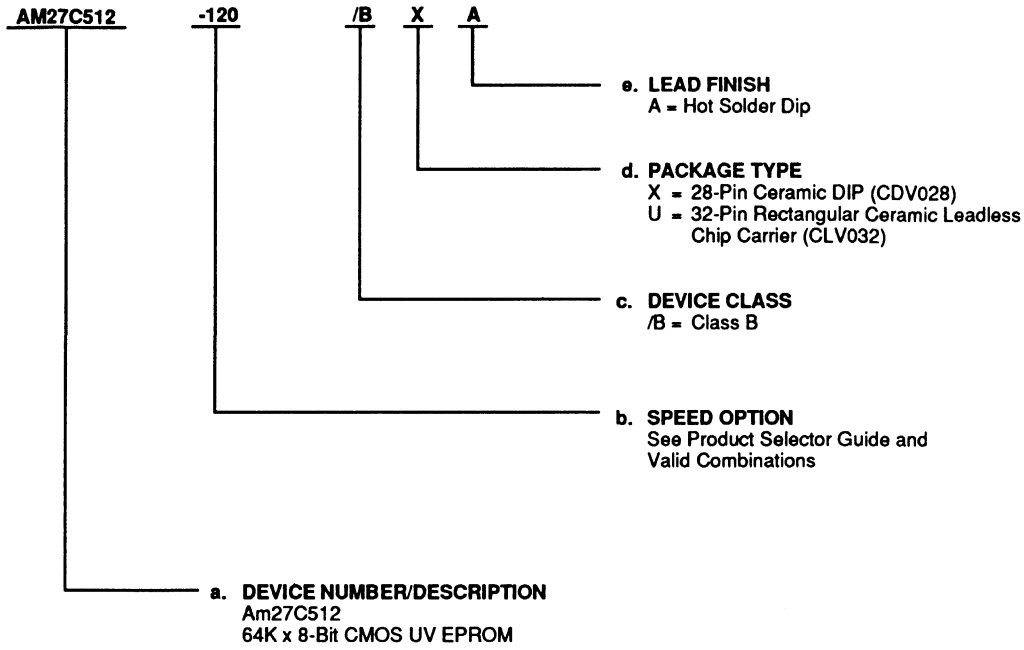
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Lead Finish



Valid Combinations	
AM27C512-120	/BXA, /BUA
AM27C512-150	
AM27C512-200	
AM27C512-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C512

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C512 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C512. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Angstroms (Å)—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C512 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C512, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C512 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C512

Upon delivery, or after each erasure, the Am27C512 has all 524,288 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C512 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the $\overline{OE}/V_{PP}$ pin, and $\overline{CE}$ is at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite programming algorithm (shown in Figure 1) reduces programming time by using initial 100 µs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with $V_{CC} = V_{PP}$ = 5.25 V.

Program Inhibit

Programming of multiple Am27C512s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C512 including $\overline{OE}/V_{PP}$ may be common. A TTL low-level program pulse applied to an Am27C512 $\overline{CE}$ input with $\overline{OE}/V_{PP}$ = 12.75 ± 0.25 V will program that Am27C512. A high-level $\overline{CE}$ input inhibits the other Am27C512s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmeed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C512.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and byte 1 ($A_0 = V_{IH}$), the device identifier code. For the Am27C512, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}—t_{OE}.

Standby Mode

The Am27C512 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C512 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL–standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high–impedance state, independent of the $\overline{OE}$ input.

Output OR–Tieing

To accomodate multiple memory connections, a two–line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins		$\overline{CE}$	$\overline{OE}/V_{PP}$	A_0	A_9	Outputs
Read		V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	High Z
Program		V_{IL}	V_{PP}	X	X	D_{IN}
Program Verify		V_{IL}	V_{IL}	X	X	D_{OUT}
Program Inhibit		V_{IH}	V_{PP}	X	X	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	91H

Notes:

1. X can be either V_{IL} or V_{IH}
2. $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$
3. $A_1–A_8 = A_{10}–A_{15} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:
- OTP Products: –65 to + 125°C
- All Other Products: –65 to + 150°C

Ambient Temperature with Power Applied: –55 to +125°C

Voltage with Respect to Ground:
- All pins except A_9, V_{PP}, and V_{CC} (Note 1): –0.6 to V_{CC} + 0.6 V
- A_9 and V_{PP} (Note 2): –0.6 to 13.5 V
- V_{CC}: –0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. During transitions the inputs may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices
- Case Temperature (T_C): 0 to +70°C

Industrial (I) Devices
- Case Temperature (T_C): –40 to +85°C

Extended Commercial (E) Devices
- Case Temperature (T_C): –55 to +125°C

Military (M) Devices
- Case Temperature (T_C): –55 to +125°C

Supply Read Voltages:
- V_{CC}/V_{PP} for Am27C512–XX5: +4.75 to +5.25 V
- V_{CC}/V_{PP} for Am27C512–XX0: +4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 7)

TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.3	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		5.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = VIL, f = 10 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		40	mA
			E/M Devices		50	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	C/I Devices		1.0	mA
			E/M Devices		1.0	

DC CHARACTERISTICS over operating range unless otherwise specified (Continued)

CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			V_{CC} – 0.3	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.3	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		5.0	µA
			E/M Devices		5.0	
I_{CC1}	Vcc Active Current (Note 5)	$\overline{CE}$ = VIL, f = 10 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		40	mA
			E/M Devices		50	
I_{CC2}	Vcc Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	C/I Devices		100	µA
			E/M Devices		100	

CAPACITANCE (Notes 2, 3, & 6)

Parameter Symbol	Parameter Description	Test Conditions	Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	10	pF
C_{IN2}	$\overline{OE}$/V_{PP} Input Capacitance	V_{IN} = 0 V	12	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	10	pF

Notes:

1. Vcc must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27C512 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. TA = 25°C, f = 1 MHz.
7. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns.
   Maximum DC voltage on input pins may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27C512						Unit
JEDEC	Standard				-75	-90, -95	-120, -125	-150	-200	-255, -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$	Min.							ns
				Max.	70	90	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}/V_{PP} = V_{IL}$	Min.							ns
				Max.	70	90	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.							ns
				Max.	40	40	50	50	75	100	
t_{EHQZ}, t_{GHQZ}	t_{DF}	Output Enable HIGH to Output Float (Note 2)		Min.							ns
				Max.	25	30	30	30	30	30	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	0	ns
				Max.							

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27C512 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. For the Am27C512-75:

   Output Load: 1 TTL gate and C_L = 30 pF,

   Input Rise and Fall Times: 20 ns,

   Input Pulse Levels: 0 to 3 V,

   Timing Measurement Reference Level: 1.5 V for inputs and outputs.

For all other versions:

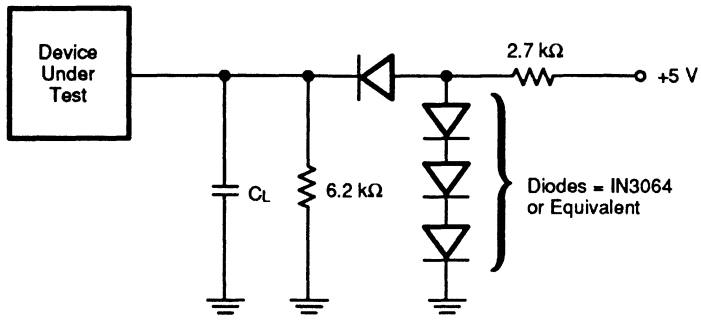
Output Load: 1 TTL gate and CL = 100 pF,

Input Rise and Fall Times: 20 ns,

Input Pulse Levels: 0.45 to 2.4 V,

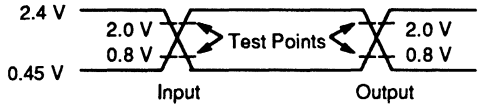
Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs.

SWITCHING TEST CIRCUIT

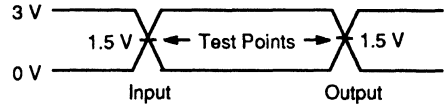


C_L = 100 pF including jig capacitance (30 pF for -75)

SWITCHING TEST WAVEFORMS



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



08140-006A

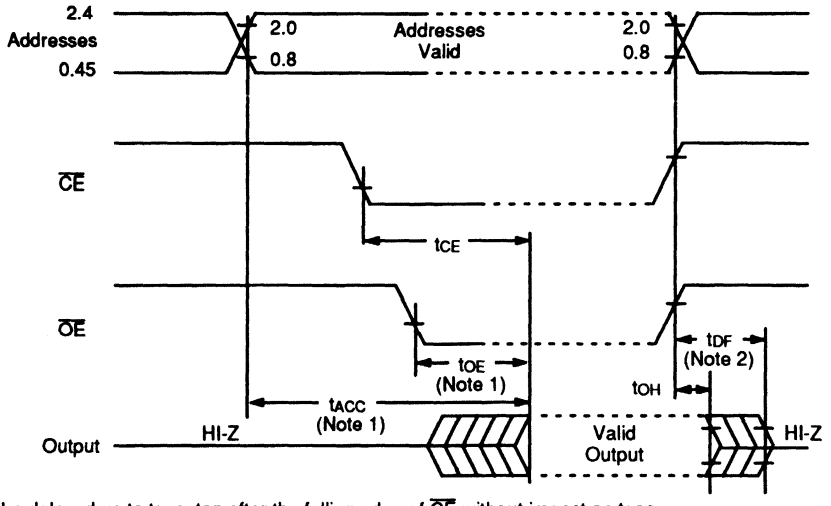
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for -75 devices.

SWITCHING WAVEFORMS

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010



08140-007A

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING FLOW CHART

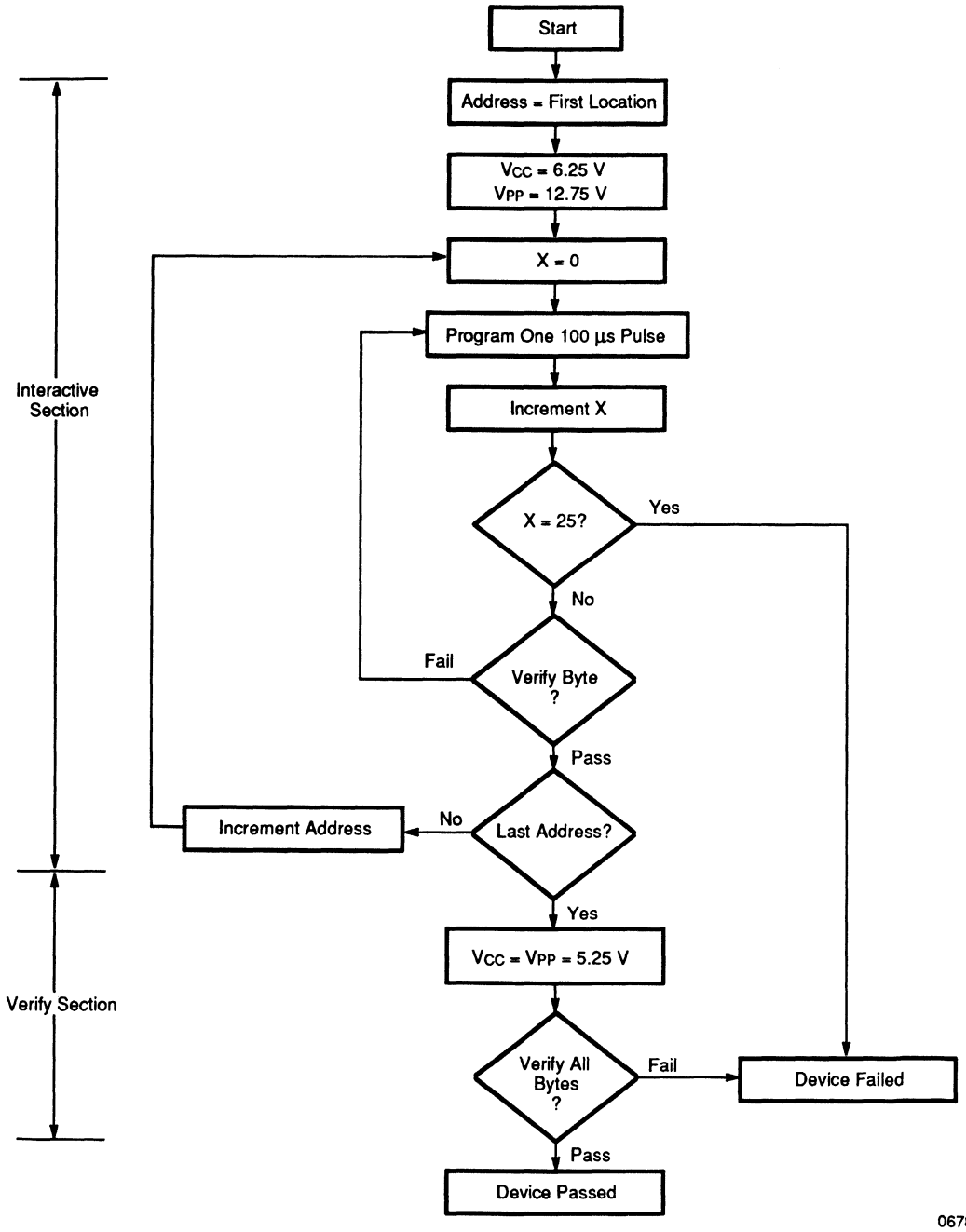


Figure 1. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ± 5°C) (Notes 1, 2, & 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.3	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$		30	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

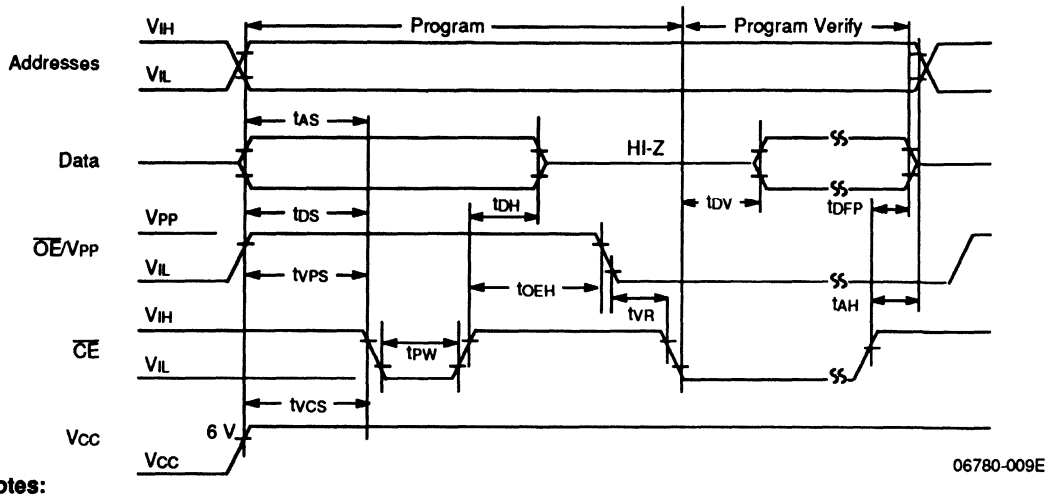
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ± 5°C) (Notes 1, 2, & 3)

Parameter Symbols		Parameter			
JEDEC	Standard	Description	Min.	Max.	Unit
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{EHQZ}	t_{DFP}	Chip Enable to Output Float Delay	0	60	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH}	t_{PW}	$\overline{CE}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELQV}	t_{DV}	Data Valid from $\overline{CE}$		250	ns
t_{EHGL}	t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2		µs
t_{GLEL}	t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	2		µs

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C512, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

PROGRAMMING ALGORITHM WAVEFORMS (Notes 1 & 2)



Notes:

1. The input timing reference level is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

Preliminary

Am27C512L

65,536 x 8-Bit Ultra-Low CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time—70ns**
- **Ultra-low power consumption:**
  - **5 mA maximum active current at 5 MHz**
  - **20 µA maximum standby current**
- **Programming voltage: 12.75 V**
- **Single +5 -V power supply**
- **JEDEC-approved pinout**
  - **Plug in replacement for Am27C512**
- **±10% power supply tolerance**
- **Fast Flashrite™ programming**
  - **Typical programming time of 15 seconds**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**

GENERAL DESCRIPTION

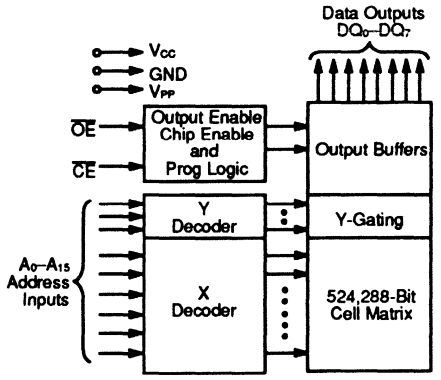
The Am27C512L is a 512K-bit, ultraviolet erasable programmable read-only memory. It is organized as 65,536 words by 8 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

Typically, any byte can be accessed in less than 70 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C512L offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 25 mW in active mode and 5 MHz operation, and 100 µW in standby mode and CMOS levels.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random.

BLOCK DIAGRAM



08140-001A

PRODUCT SELECTOR GUIDE

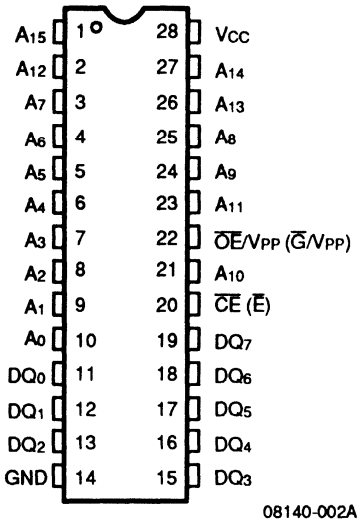
Family Part No.	Am27C512L					
Ordering Part Number ±5% Vcc Tolerance	-75	-95	-125			-255
±10% Vcc Tolerance	–	-90	-120	-150	-200	-250
Max. Access Time (ns)	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	40	50	50	75	100

Publication# 15616A Rev. A Amendment/0
Issue Date: March 1991

CONNECTION DIAGRAMS

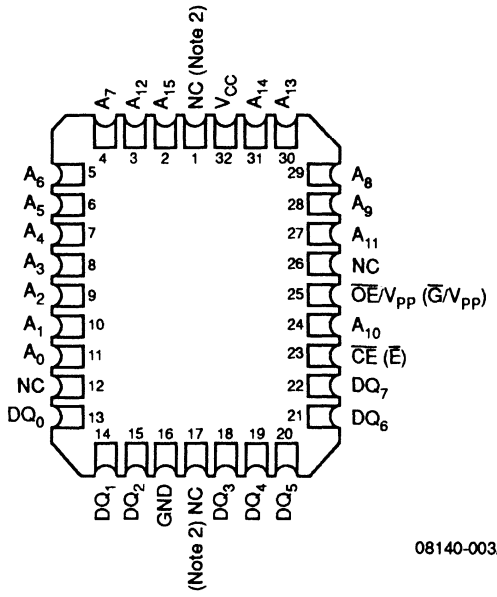
Top View

DIP



08140-002A

LCC*



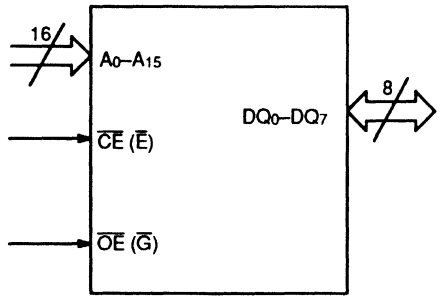
08140-003A

* Also Available in a 32-pin rectangular plastic leaded chip carrier

Notes:

1. JEDEC nomenclature is in parantheses.
2. Don't use (DU) for PLCC.

LOGIC SYMBOL



08140-004A

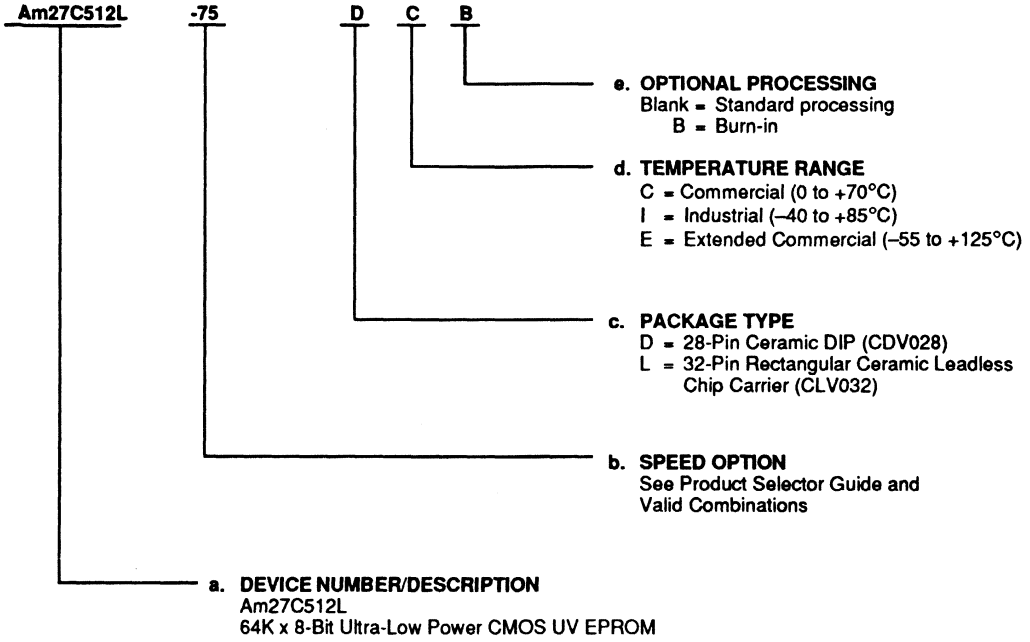
PIN DESCRIPTION

$A_0 - A_{15}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_7$	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
Am27C512L-75	DC, DCB, LC, LCB
Am27C512L-95	DC, DCB, DI, DIB, LC, LCB, LI, LIB
Am27C512L-125	
Am27C512L-90	
Am27C512L-120	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
Am27C512L-150	
Am27C512L-200	
Am27C512L-255	

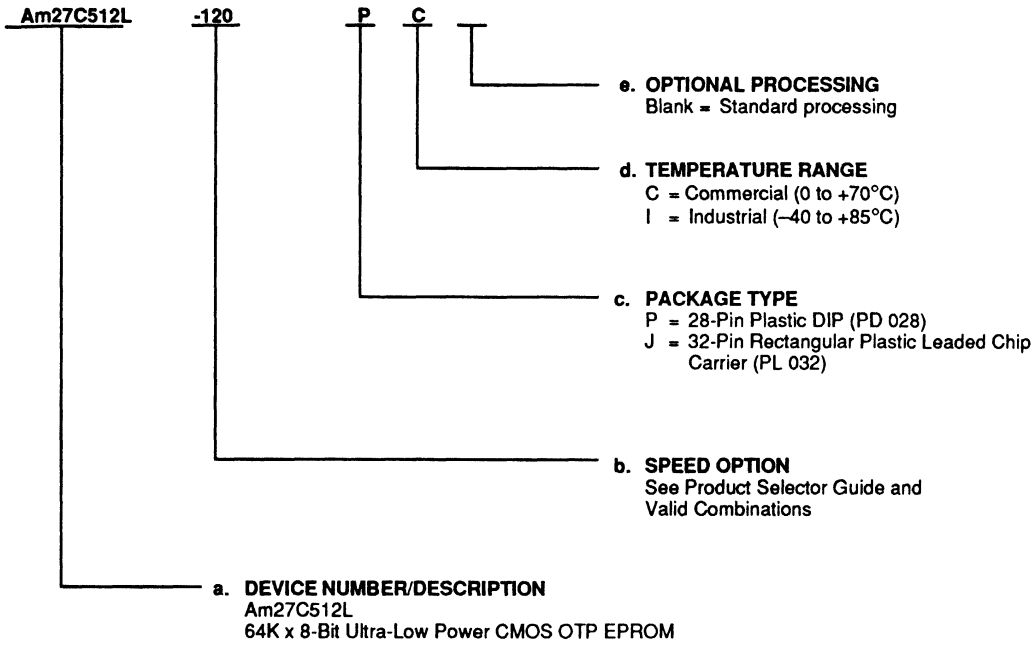
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
Am27C512L-120	JC, PC, JI, PI
Am27C512L-150	
Am27C512L-200	
Am27C512L-255	

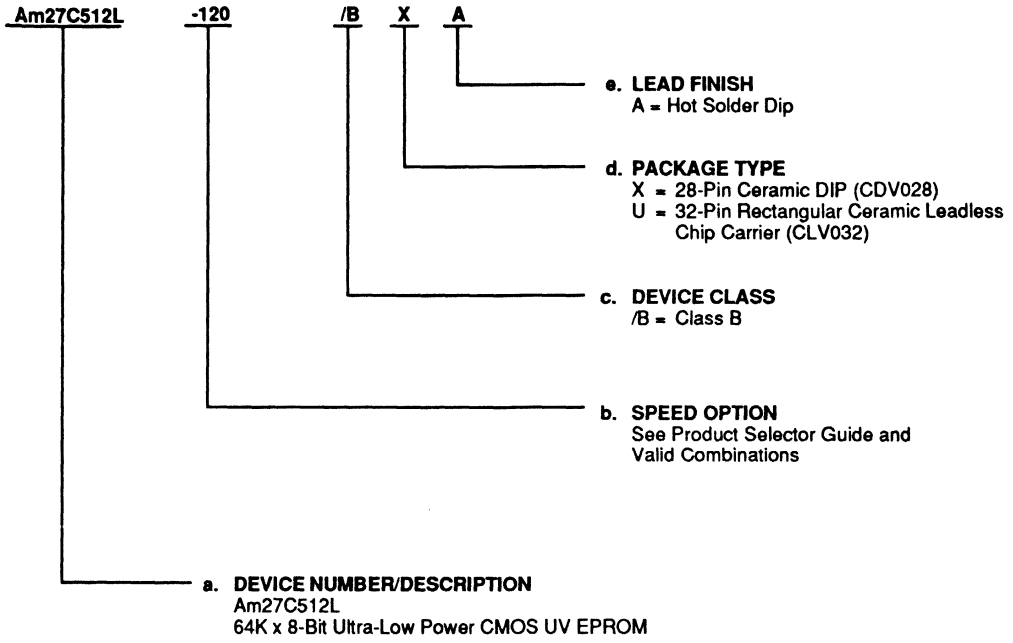
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Lead Finish



Valid Combinations	
Am27C512L-120	/BXA, /BUA
Am27C512L-150	
Am27C512L-200	
Am27C512L-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C512L

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C512L to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C512L. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Angstroms (Å)—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C512L should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C512L, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C512L and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C512L

Upon delivery, or after each erasure, the Am27C512L has all 524,288 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C512L through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the $\overline{OE}/V_{PP}$ pin, and $\overline{CE}$ is at V_{IL}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite programming algorithm (shown in Figure 1) reduces programming time by using initial 100 µs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with $V_{CC} = V_{PP}$ = 5.25 V.

Program Inhibit

Programming of multiple Am27C512Ls in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C512L including $\overline{OE}/V_{PP}$ may be common. A TTL low-level program pulse applied to an Am27C512L $\overline{CE}$ input with $\overline{OE}/V_{PP}$ = 12.75 ± 0.25 V will program that Am27C512L. A high-level $\overline{CE}$ input inhibits the other Am27C512Ls from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmeed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C512L.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C512L. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and byte 1 ($A_0 = V_{IH}$), the device identifier code. For the Am27C512L, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C512L has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least t_{ACC}—t_{OE}.

Standby Mode

The Am27C512L has a CMOS standby mode which reduces the maximum V_{CC} current to 20 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C512L also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL–standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high–impedance state, independent of the $\overline{OE}$ input.

Output OR–Tieing

To accomodate multiple memory connections, a two–line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins		$\overline{CE}$	$\overline{OE}/V_{PP}$	A_0	A_9	Outputs
Read		V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	High Z
Program		V_{IL}	V_{PP}	X	X	D_{IN}
Program Verify		V_{IL}	V_{IL}	X	X	D_{OUT}
Program Inhibit		V_{IH}	V_{PP}	X	X	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	91H

Notes:

1. X can be either V_{IL} or V_{IH}
2. $V_H = 12.0 \text{ V} \pm 0.5$ V
3. A_1–$A_8 = A_{10}$–$A_{15} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	–65 to + 125°C
All Other Products	–65 to + 150°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC} (Note 1)	–0.6 to V_{CC} + 0.6 V
A_9 and V_{PP} (Note 2)	–0.6 to 13.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. During transitions the inputs may undershoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.
2. During transitions, A_9 and V_{PP} may undershoot GND to –2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0 to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	–40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (T_C)	–55 to +125°C
Military (M) Devices	
Case Temperature (T_C)	–55 to +125°C
Supply Read Voltages:	
V_{CC}/V_{PP} for Am27C512L–XX5	+4.75 to +5.25 V
V_{CC}/V_{PP} for Am27C512L–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 7)

TTL and NMOS

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.3	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		2.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = VIL, f = 10 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		15	mA
			E/M Devices		25	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	C/I Devices		1.0	mA
			E/M Devices		1.0	

DC CHARACTERISTICS over operating range unless otherwise specified (Continued)

CMOS

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		V_{CC} – 0.8		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			0.7 V_{CC}	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		2.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Note 5 & 8)	$\overline{CE}$ = VIL, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		5.0	mA
			E/M Devices		10	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	C/I Devices		20	µA
			E/M Devices		40	

CAPACITANCE (Notes 2, 3, & 6)

Parameter Symbol	Parameter Description	Test Conditions	CDV028 Max.	CLV032 Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	12	9	pF
C_{IN2}	$\overline{OE}$/V_{PP} Input Capacitance	V_{IN} = 0 V	20	20	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	12	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	15	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27C512L must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. TA = 25°C, f = 1 MHz.
7. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC voltage on input pins may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.
8. I_{CC1} varies 1 mA per MHz for C/I devices. I_{CC1} varies 2 mA per MHz for E/M devices.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

Parameter Symbols		Parameter Description	Test Conditions		Am27C512L						Unit
JEDEC	Standard				-75	-90, -95	-120, -125	-150	-200	-255, -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}	Min.							ns
				Max.	70	90	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}/V_{PP}$ = V_{IL}	Min.							ns
				Max.	70	90	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.							ns
				Max.	40	40	50	50	75	100	
t_{EHQZ}, t_{GHQZ}	t_{DF}	Output Enable HIGH to Output Float (Note 2)		Min.							ns
				Max.	25	30	30	30	30	30	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	0	ns
				Max.							

Notes:

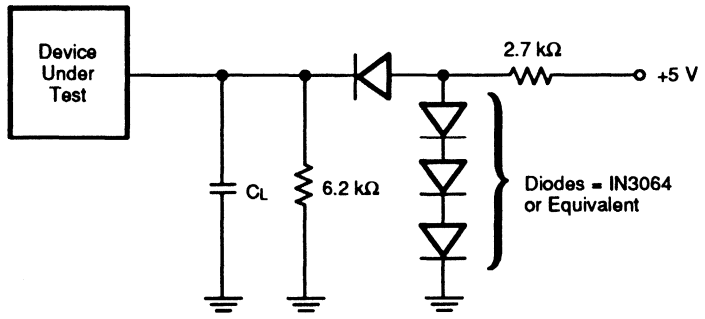
1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27C512L must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. For the Am27C512L-75:

   Output Load: 1 TTL gate and C_L = 30 pF,
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0 to 3 V,
   Timing Measurement Reference Level: 1.5 V for inputs and outputs.

   For all other versions:

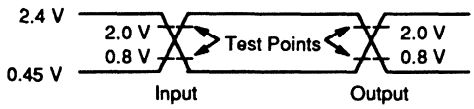
   Output Load: 1 TTL gate and CL = 100 pF,
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0.45 to 2.4 V,
   Timing Measurement Reference Level: 0.8 V and 2 V for inputs and outputs.

SWITCHING TEST CIRCUIT

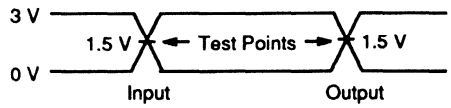


C_L = 100 pF including jig capacitance (30 pF for -75)

SWITCHING TEST WAVEFORMS



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



08140-006A

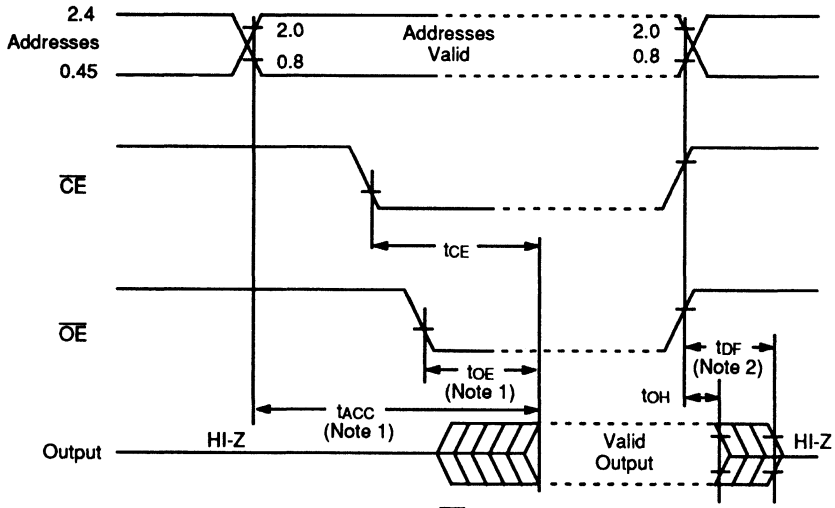
AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns for -75 devices.

SWITCHING WAVEFORMS

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010



08140-007A

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING FLOW CHART

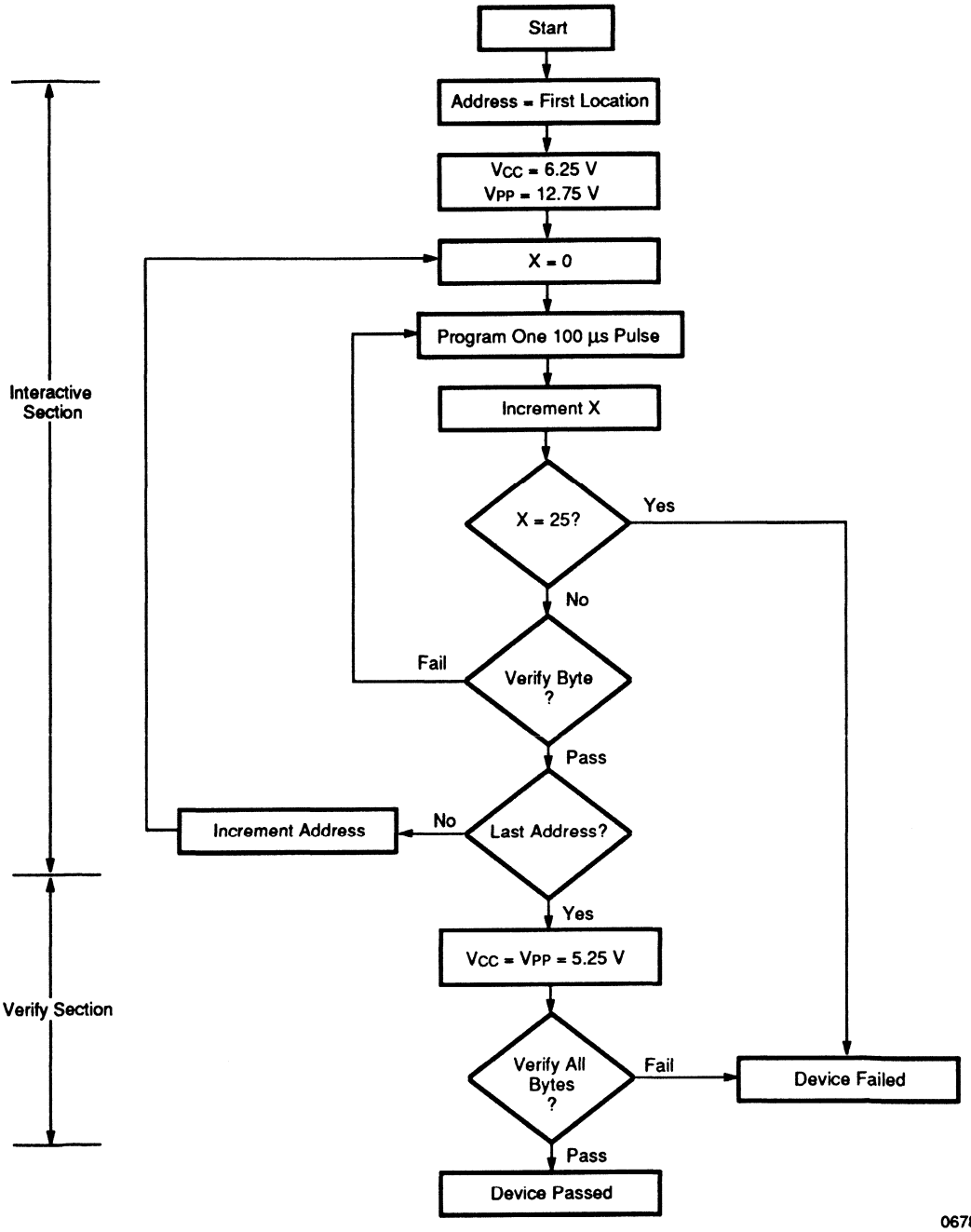


Figure 1. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ± 5°C) (Notes 1, 2, & 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.3	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$		30	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

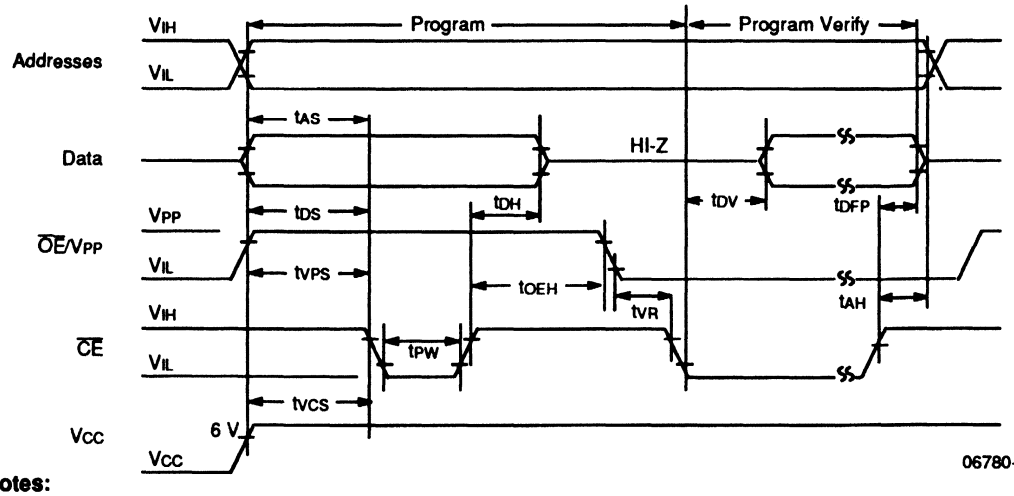
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ± 5°C) (Notes 1, 2, & 3)

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{EHQZ}	t_{DFP}	Chip Enable to Output Float Delay	0	60	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH}	t_{PW}	$\overline{CE}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELQV}	t_{DV}	Data Valid from $\overline{CE}$		250	ns
t_{EHGL}	t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	2		µs
t_{GLEL}	t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	2		µs

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C512L, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

PROGRAMMING ALGORITHM WAVEFORMS (Notes 1 & 2)



Notes:

1. The input timing reference level is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

Am27C010

1 Megabit (131,072 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Easy upgrade from 28-Pin JEDEC EPROMs**
- **Fast access time—100 ns**
- **Low power consumption:**
  - 100 µA maximum standby current
- **Programming voltage: 12.75 V**
- **Single +5 V power supply**
- **Compact 32-Pin DIP package requires no hardware change for upgrades to 8 megabits**
- **JEDEC-approved pinout**
- **±10% power supply tolerance standard on most speeds**
- **Fast Flashrite™ programming**
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**

GENERAL DESCRIPTION

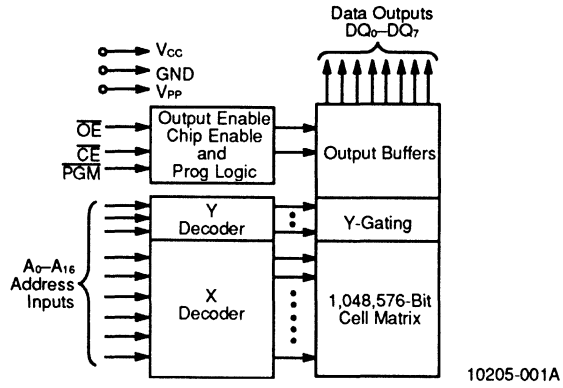
The Am27C010 is a 1 megabit, ultraviolet erasable programmable read-only memory. It is organized as 128K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C010 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random.

BLOCK DIAGRAM



10205-001A

PRODUCT SELECTOR GUIDE

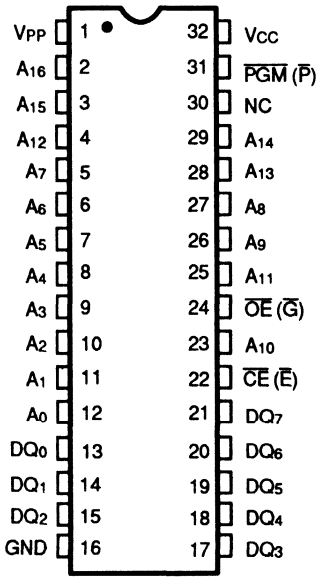
Family Part No.	Am27C010				
Ordering Part No: ±5% Vcc Tolerance	-105	-125			-255
±10% Vcc Tolerance		-120	-150	-200	-250
Max. Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	50	65	75	100

Publication# 10205 Rev. C Amendment/0
Issue Date: March 1991

CONNECTION DIAGRAMS

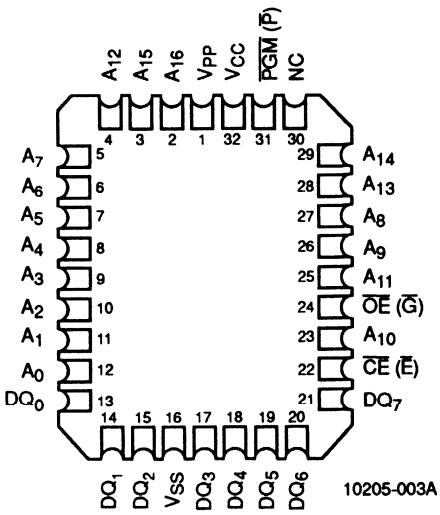
Top View

DIP



10205-002A

LCC*



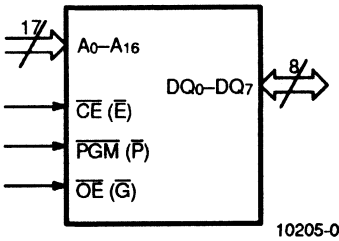
10205-003A

*Also available in a 32-pin rectangular Plastic Leaded Chip Carrier.

Notes:

1. JEDEC nomenclature is in parenthesis.
2. The 32-pin DIP to 32-pin LCC configuration varies from the JEDEC 28-pin DIP to 32-pin LCC configuration.

LOGIC SYMBOL



10205-004A

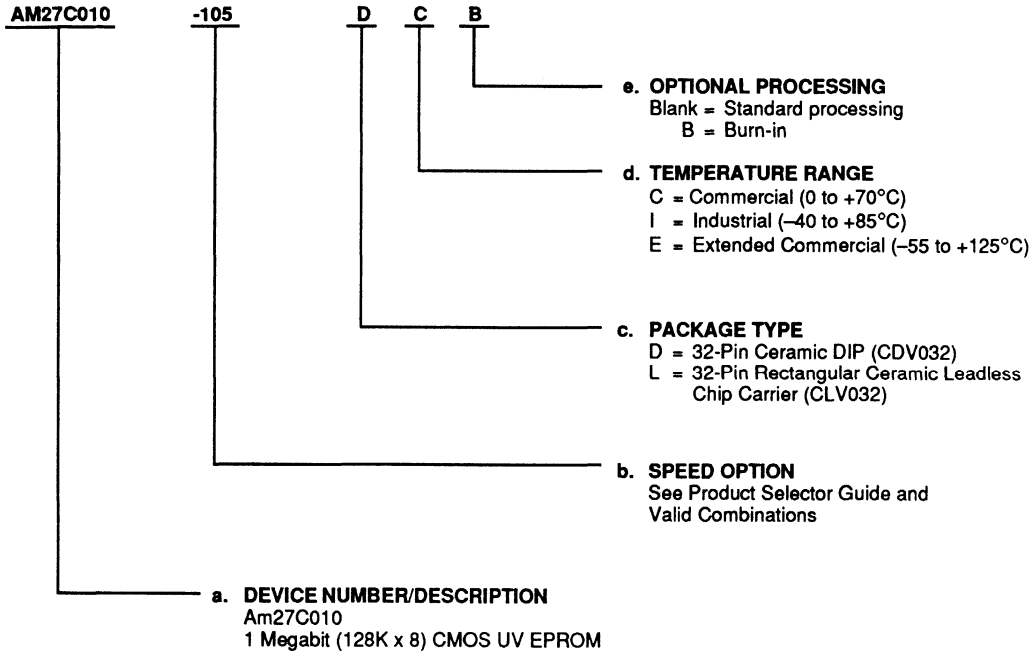
PIN DESCRIPTION

A0–A16	Address Inputs	**PGM (P)**	Program Enable Input
CE (E)	Chip Enable Input	**VCC**	VCC Supply Voltage
DQ0–DQ7	Data Input/Outputs	**VPP**	Program Supply Voltage
OE (G)	Output Enable Input	**GND**	Ground
		NC	No Internal Connect

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C010-105	DC, DCB
AM27C010-120	DC, DCB, DI, DIB, LC, LI
AM27C010-125	
AM27C010-150	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27C010-200	
AM27C010-255	

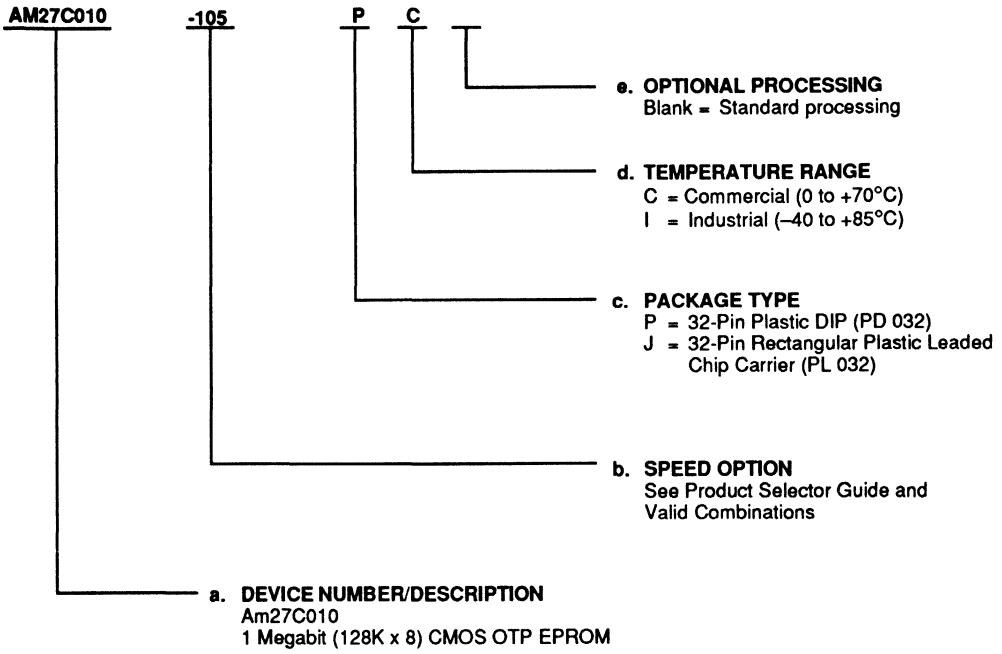
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C010-105	PC, JC, PI, JI
AM27C010-120	
AM27C010-125	
AM27C010-150	
AM27C010-200	
AM27C010-255	

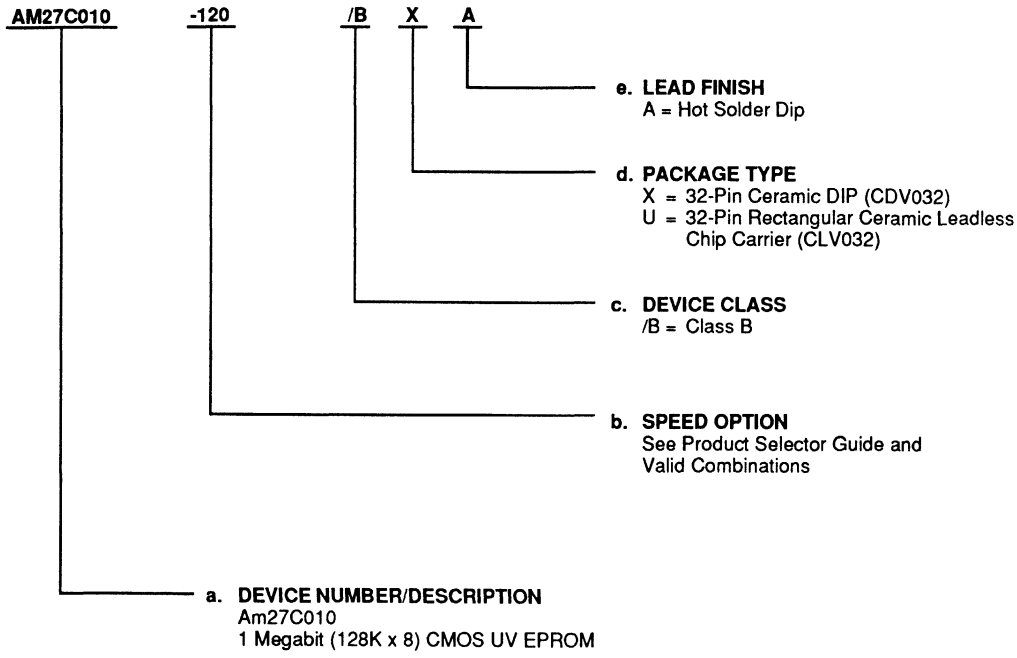
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27C010-120	/BXA, /BUA
AM27C010-150	
AM27C010-200	
AM27C010-250	

For other Surface Mount Package options, contact NVD Military Marketing.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C010

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C010 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C010. This dosage can be obtained by exposure to an ultraviolet lamp —wavelength of 2537 Angstroms (Å) —with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C010 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C010, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C010 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C010

Upon delivery, or after each erasure, the Am27C010 has all 1,048,576 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C010 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ and $\overline{PGM}$ are at V_{IL} and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite programming algorithm (shown in Figure 1) reduces programming time by using initial 100 µs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.25 V.

Program Inhibit

Programming of multiple Am27C010s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C010 may be common. A TTL low-level program pulse applied to an Am27C010 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V, $\overline{PGM}$ LOW, and $\overline{OE}$ HIGH will program that Am27C010. A high-level $\overline{CE}$ input inhibits the other Am27C010s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C010.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C010. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A_0 = V_{IL}) represents the manufacturer code, and Byte 1 (A_0 = V_{IH}), the device identifier code. For the Am27C010, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C010 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C010 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C010 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low-power standby mode and that the outut pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_0	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	X	X	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	X	High Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	OEH

Notes:

1. X can be either V_{IL} or V_{IH}
2. $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$
3. $A_1 - A_8 = A_{10} - A_{16} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	−65 to +125°C
All Other Products	−65 to +150°C
Ambient Temperature with Power Applied	−55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC} (Note 1)	−0.6 to V_{CC} +0.6 V
A_9 and V_{PP} (Note 2)	−0.6 to 13.5 V
V_{CC}	−0.6 to 7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. This is a stress rating only; functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Notes:

1. During transitions, the input may overshoot GND to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to −2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (Tc)	0 to +70°C
Industrial (I) Devices	
Case Temperature (Tc)	−40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (Tc)	−55 to +125°C
Military (M) Devices	
Case Temperature (Tc)	−55 to +125°C
Supply Read Voltages:	
V_{CC} for Am27C010-XX5	+4.75 to +5.25 V
V_{CC} for Am27C010-XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 4, 5 & 8) (for APL products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
TTL and NMOS Inputs						
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		10	µA
			E/M Devices		10	
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		30	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}	C/I Devices		1.0	mA
			E/M Devices		1.0	
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA
CMOS Inputs						
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			V_{CC} – 0.3	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		10	µA
			E/M Devices		10	
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		30	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	C/I Devices		100	µA
			E/M Devices		100	
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV032		CLV032		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution**: The Am27C010 must not be removed from, or inserted into, a socket or board when V_{CC} or V_{PP} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = +25°C, f = 1 MHz.
8. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns.
   Maximum DC voltage on output pins may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.

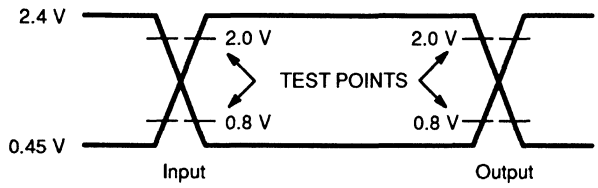
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4) (for APL products, Group A, Subgroups 9, 10, and 11 are tested unless otherwise noted)

JEDEC	Standard	Parameter Description	Test Conditions		Am27C010					Unit
					-105	-120, -125	-150	-200	-250, -255	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.						ns
				Max.	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.						ns
				Max.	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.	–	–	–	–	–	ns
				Max.	50	50	65	75	100	
t_{EHQZ}, t_{GHQZ}	t_{DF}	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float (Note 2)		Min.	0	0	0	0	0	ns
				Max.	35	35	35	40	40	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	ns
				Max.	–	–	–	–	–	

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled, not 100% tested.
3. **Caution**: The Am27C010 must not be removed from, or inserted into, a socket when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 n
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V.

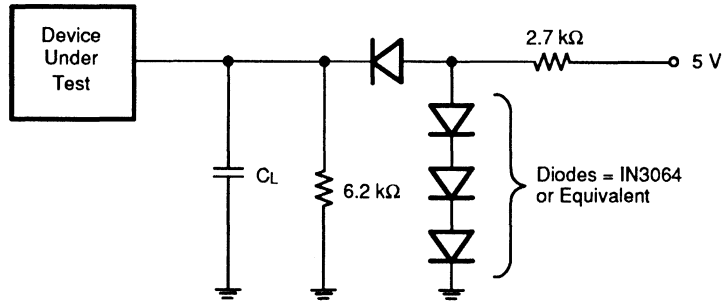
SWITCHING TEST WAVEFORM



10205-005A

AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

SWITCHING TEST CIRCUIT



10205-006A

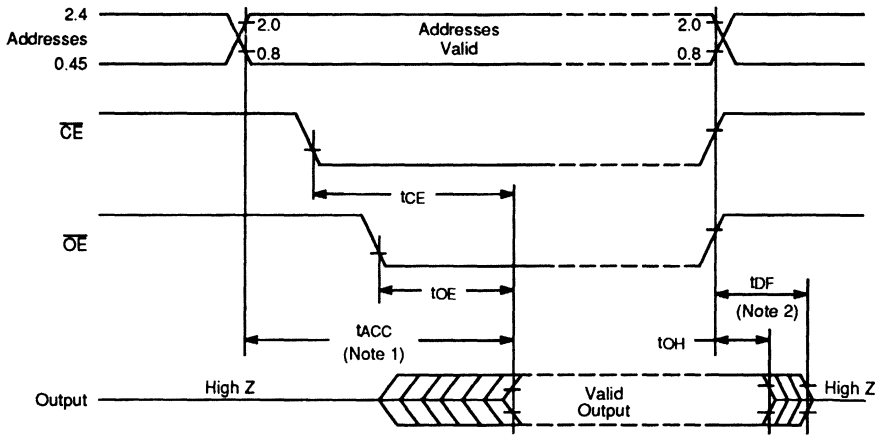
C_L = 100 pF including jig capacitance

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORM



10205-007B

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING FLOW CHART

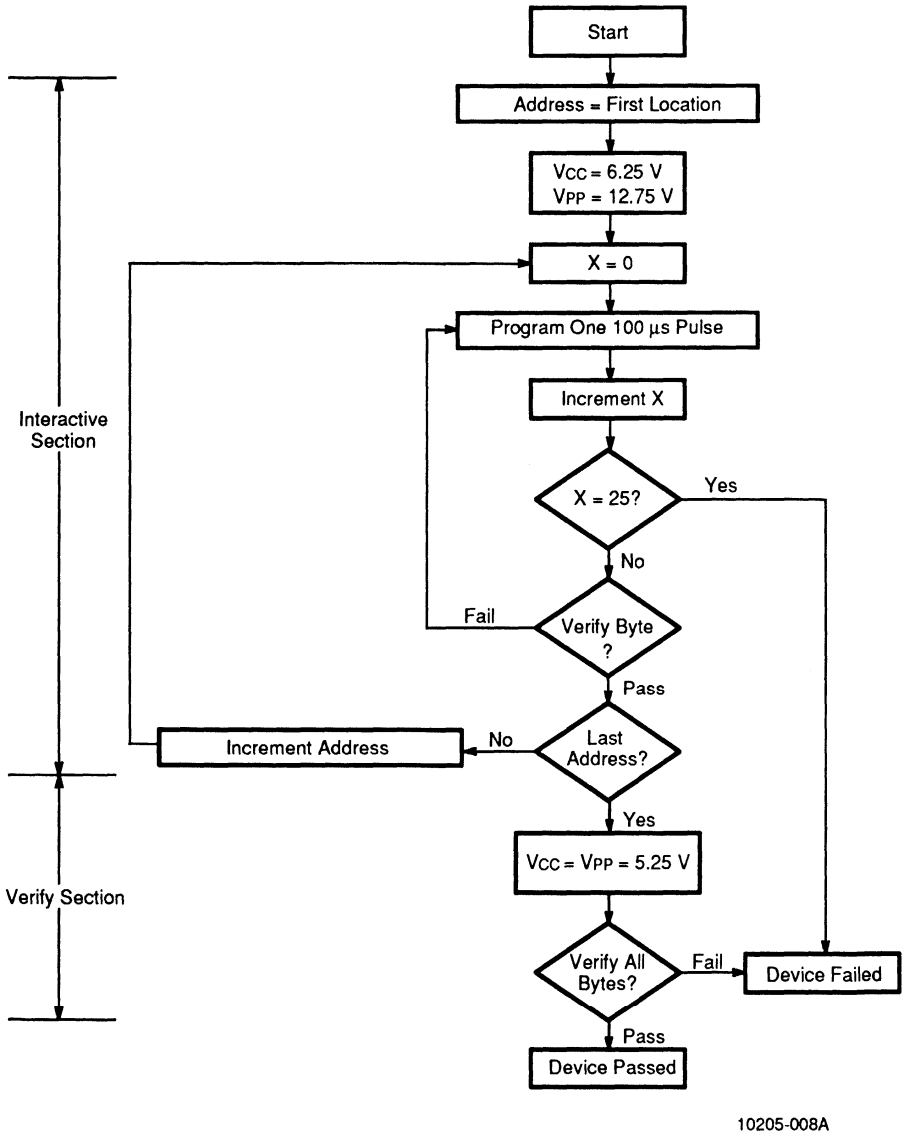


Figure 1. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.3	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

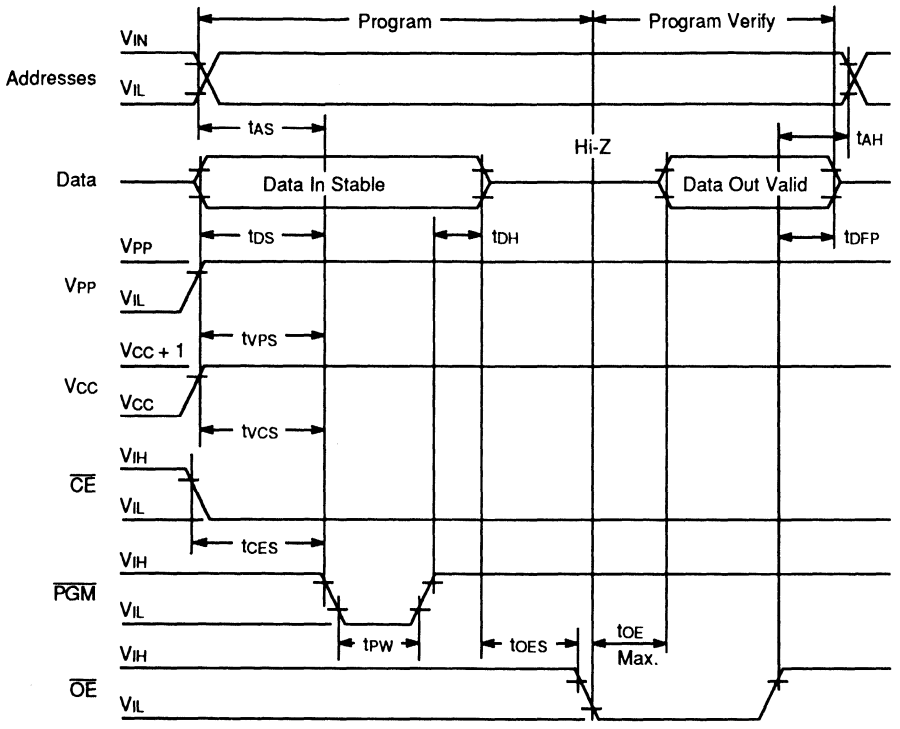
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min.	Max.	Unit
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C010, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

INTERACTIVE AND FLASHRITE PROGRAMMING ALGORITHM WAVEFORM (Notes 1 & 2)



10205-009A

Notes:

1. The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

Am27H010

1 Megabit (131,072 x 8-Bit) High Speed CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Industry's fastest**
  - -45ns 1 megabit CMOS EPROM
- **Pin compatible with Am27C010**
- **High speed Flashrite™ programming**
  - -Typically less than 30 seconds
- **Versions available in industrial and military temperature ranges**
- **± 10% power supply tolerance available**

GENERAL DESCRIPTION

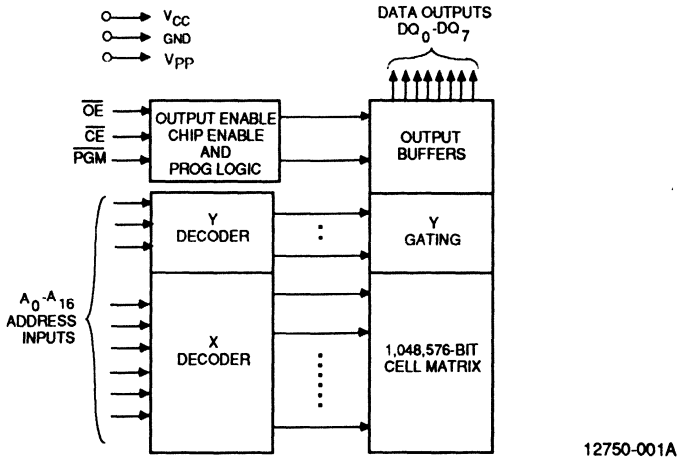
The Am27H010 is an ultra-high speed 1 megabit CMOS UV EPROM. It utilizes the standard JEDEC pinout making it functionally compatible with the Am27C010, but with significantly faster access capability. This superior random access capability results from a focused high-speed design implemented with AMD's advanced CMOS process technology. This offers users bipolar speeds with higher density, lower cost and proven reliability.

This device is ideal for use with the fastest processors. At 45ns, the Am27H010 completely eliminates performance-draining wait states without using bank-interleaving and caching techniques. Designers may take full advantage of high speed digital signal processors and microprocessors by allowing code to be executed at full speed directly out of EPROM. Typical applications include laser printers, switching networks, graphics, workstations and digital signal processing.

The Am27H010 supports AMD's Flashrite programming algorithm which allows the entire chip to be programmed in typically less than 30 seconds.

It is available in DIP as well as surface mount packages and is offered in commercial, industrial, and extended temperature ranges.

BLOCK DIAGRAM



12750-001A

PRODUCT SELECTOR GUIDE

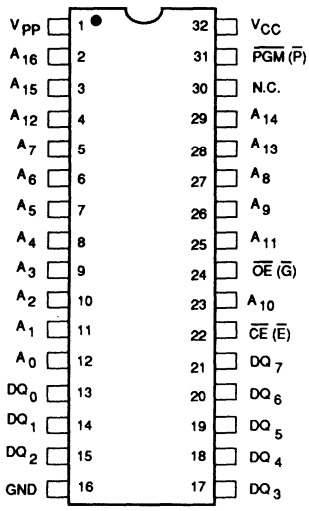
Family Part No.	Am27H010			
Ordering Part No:				
V_{CC} ± 5%	-45V05	–	–	-90V05
V_{CC} ± 10%	-45	-55	-70	-90
Max. Access Time (ns)	45	55	70	90
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	45	55	70	90
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	20	25	35	40

Publication# 12750 Rev. C Amendment /0
Issue Date: March 1991

CONNECTION DIAGRAMS

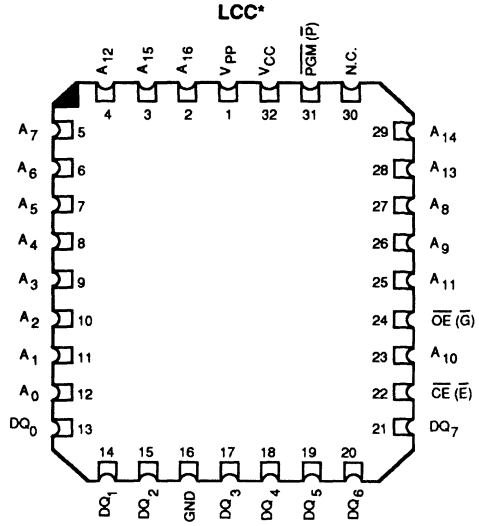
Top View

DIPs



12750-002A

LCC*



12750-003A

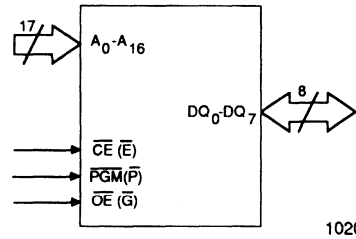
Note:
JEDEC nomenclature is in parentheses.

* Also available in 32-pin rectangular plastic leaded chip carrier

PIN DESCRIPTION

A_0–A_{16}	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ_0–DQ_7	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connection

LOGIC SYMBOL

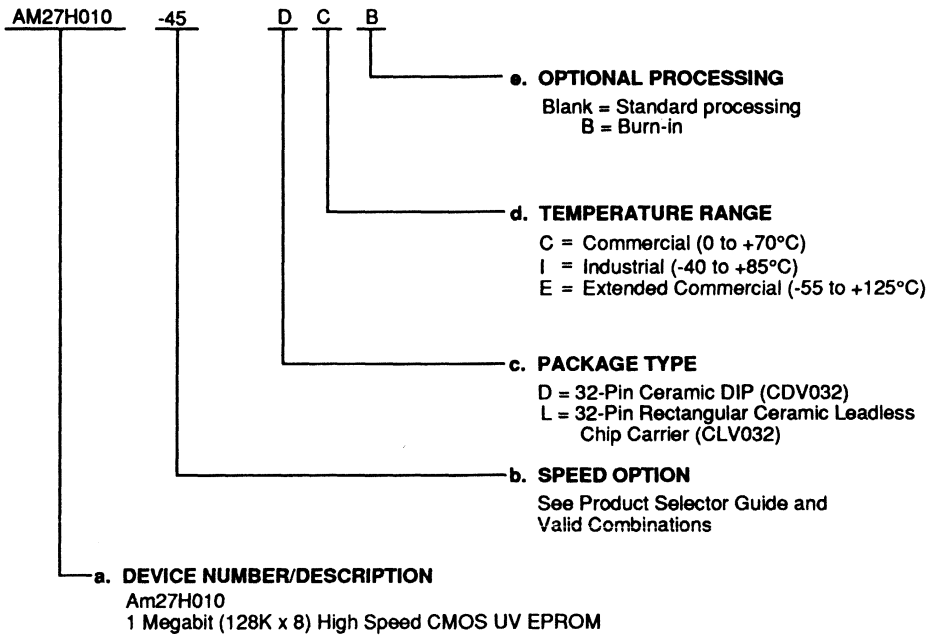


10205A-002A

ORDERING INFORMATION
Standard Information

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27H010-45	DC, DCB, DI, DIB, LC, LI, LCB, LIB
AM27H010-45V05	
AM27H010-90V05	
AM27H010-55	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27H010-70	
AM27H010-90	

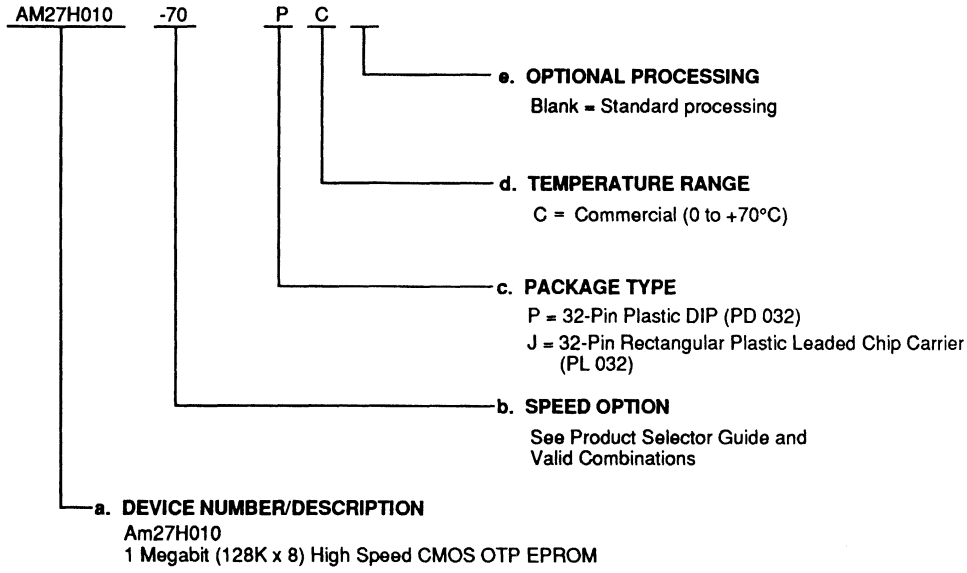
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations.

ORDERING INFORMATION
OTP Products (Preliminary)

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27H010-55	PC, JC
AM27H010-70	
AM27H010-90	
AM27H010-90V05	

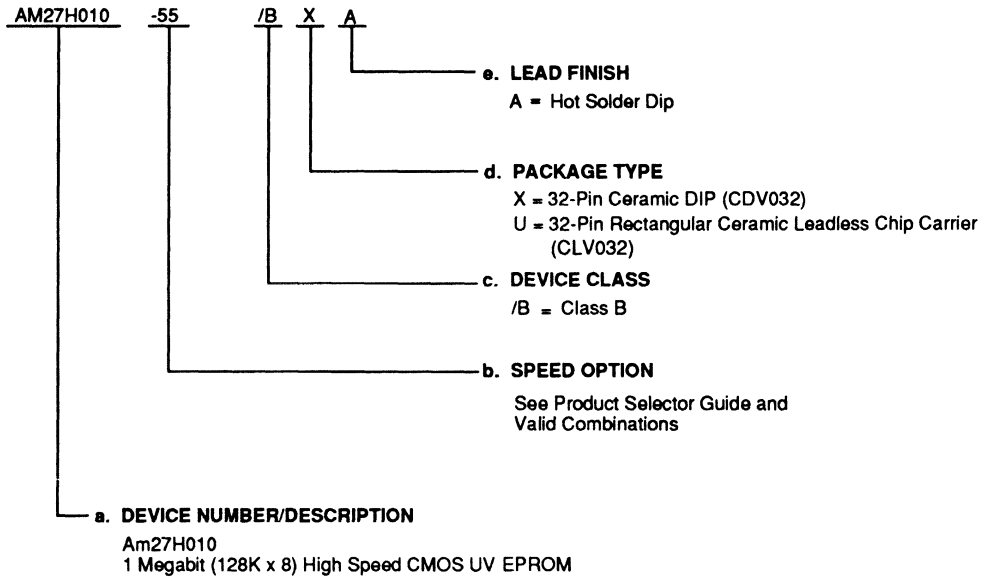
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27H010-55	/BXA, /BUA
AM27H010-70	
AM27H010-90	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27H010

In order to clear all locations of their programmed contents, it is necessary to expose the Am27H010 to an ultraviolet light source. A dosage of 30 W seconds/cm² is required to completely erase an Am27H010. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Angstroms (Å)—with intensity of 12,000 μW/cm² for 30 to 40 minutes. The Am27H010 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27H010, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27H010 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27H010

Upon delivery, or after each erasure, the Am27H010 has all 1,048,576 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27H010 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ and $\overline{PGM}$ is at V_{IL}, and $\overline{OE}$ is at V_{IH}. For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite programming algorithm reduces programming time by using initial 100 μs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with $V_{CC} = V_{PP}$ = 5.25 V.

Program Inhibit

Programming of multiple Am27H010s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27H010 may be common. A TTL low-level program pulse applied to an Am27H010 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V, $\overline{PGM}$ is LOW, and $\overline{OE}$ HIGH will program that Am27H010. A high-level $\overline{CE}$ input inhibits the other Am27H010 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V to 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27H010.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27H010. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and byte 1($A_0 = V_{IH}$), the device identifier code. For the Am27H010, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27H010 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27H010 has a standby mode which reduces the maximum V_{CC} current to 50% of the active current. It is placed in standby mode when $\overline{CE}$ is at V_{IH}. The amount of current drawn in standby mode depends on the frequency and the number of address pins switching. The Am27H010 is specified with 50% of the address lines toggling at 10 MHz. A reduction of the frequency or quantity of address lines toggling will significantly reduce the actual standby current.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in

their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_0	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	V_{IH}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	V_{IH}	Hi-Z
Standby		V_{IH}	X	X	X	X	V_{IH}	Hi-Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	Hi-Z
Auto Select	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	V_{CC}	O1H
(Note 3 & 5)	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	V_{CC}	OEH

Notes:

1. V_H = 12.0 V ± 0.5 V
2. X = Either V_{IH} or V_{IL}
3. $A_1 - A_8 = A_{10} - A_{16} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.
5. The Am27H010 uses the same Flashrite algorithm during program as the Am27C010.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
OTP product	–65 to 125°C
All other products	–65 to 150°C
Ambient Temperature	
with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC}	–0.6 to V_{CC} +0.5 V
A_9 and V_{PP}	–0.6 to 13.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. Minimum DC voltage on input or I/O is –0.5 V. During transitions, the inputs may overshoot GND to –2.0V for periods of up to 10 ns. Maximum DC voltage on input and I/O is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods up to 20 ns.
2. For A_9 and V_{PP} the minimum DC input is –0.5 V. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 10 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0 to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	–40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (T_C)	–55 to +125°C
Military (M) Devices	
Case Temperature (T_C)	–55 to +125°C
Supply Read Voltages:	
V_{CC} for Am27H010-XXV05	+4.75 to + 5.25 V
V_{CC} for Am27H010-XX	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 4, 5, & 8) (for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -4 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA			0.45	V
V_{IH}	Input HIGH Voltage (Note 9)			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage (Note 9)			– 0.3	+ 0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to + V_{CC}		1.0		µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to + V_{CC}			10	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA (Open Outputs)	C Devices		50	mA
			I/E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}	C Devices		25	mA
			I/E/M Devices		35	
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

DC CHARACTERISTICS (Cont.)

Capacitance (Notes 2, 3, and 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV032		CLV032		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	6	10	6	9	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	10	12	7	9	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	10	10	7	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	6	9	pF

Notes:

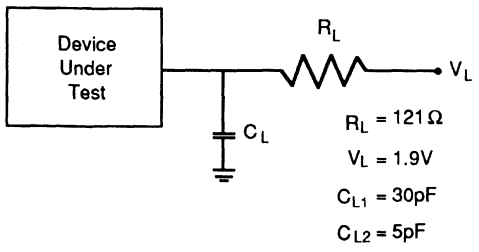
1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled, not 100% tested.
4. **Caution:** the Am27H010 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = +25°C, f = 1 MHz.
8. Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for periods less than 10 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V which may overshoot to V_{CC} +2.0 V for periods less than10 ns.
9. Tested under static DC conditions.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3, & 4) (for APL Products, Group A, Subgroups 9, 10, and 11 are specified unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27H010				Unit
JEDEC	Standard				-45V05, -45	-55	-70	-90V05, -90	
t_{AVOV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$, $C_L = C_{L1}$	Min.	–	–	–	–	ns
				Max.	45	55	70	90	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$, $C_L = C_{L1}$	Min.	–	–	–	–	ns
				Max.	45	55	70	90	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$, $C_L = C_{L1}$	Min.	–	–	–	–	ns
				Max.	20	25	35	40	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, Whichever Comes First, to Output Float	$C_L = C_{L2}$	Min.	0	0	0	0	ns
				Max.	20	25	35	40	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, Whichever Occured First		Min.	0	0	0	0	ns
				Max.	–	–	–	–	

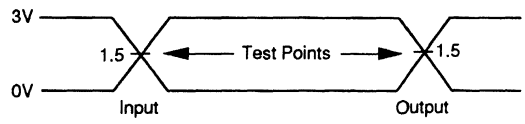
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled, not 100% tested.
3. **Caution:** The Am27H10 must not be removed from (or inserted into) a socket or board when V_{pp} or V_{cc} is applied.
4. Output Load: 1 TTL gate and C = C_L
   Input Rise and Fall Times: 5 ns
   Input Pulse Levels: 0 to 3 V
   Timing Measurement Reference Level – 1.5 V for inputs and outputs

SWITCHING TEST CIRCUIT



12750-004A

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤5 ns.

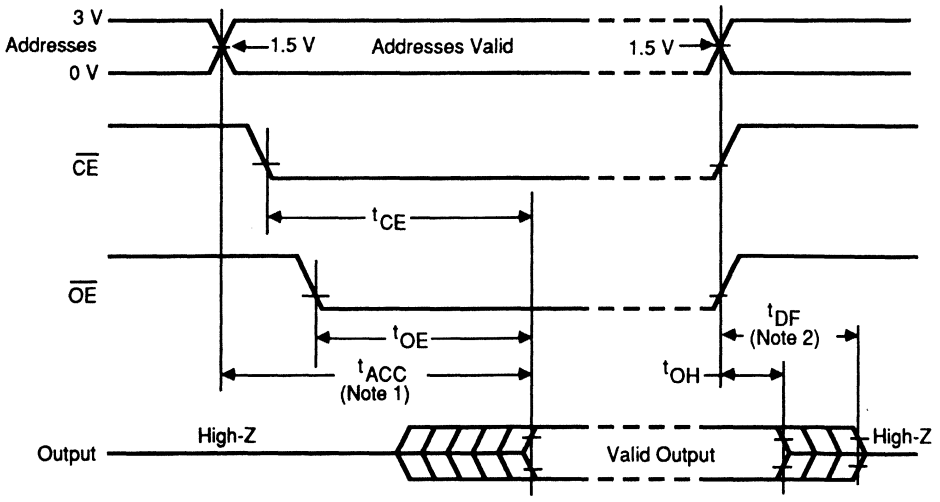
12750-005A

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



12750-006A

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Please refer to the Am27C010 data sheet for Programming Information.

Advance Information

Am27HB010

1 Megabit (131,072 x 8-Bit) Burst Mode CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High speed**
  - 50 ns random access
  - 15 ns burst access
- **No burst boundary**
- **No burst limit**
- **Pin compatible with Am27C010**
- **Supports all "Burst" microprocessors**
  - Am29000 compatible
- **Single + 5 V power supply**
- **± 10% power supply tolerance available**
- **High speed Flashrite™ programming**
  - Typically less than 30 seconds

GENERAL DESCRIPTION

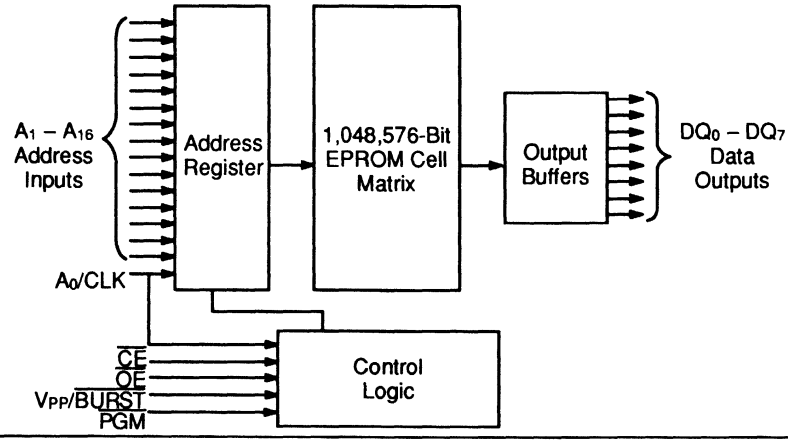
The Am27HB010 is a 1 megabit ultraviolet erasable programmable read-only memory. It is organized as 128K words by 8 bits per word. Two modes are available to access the data. Random access mode is selected by placing V_{IH} on the $V_{PP}/\overline{BURST}$ pin and this allows full random access to the data. Burst access is selected by placing V_{IL} on the $V_{PP}/\overline{BURST}$ pin which allows high speed access to sequential data. Burst mode may be entered without regard to page or word boundaries and may be sustained all the way up to the physical device boundary (128K bytes) if required.

The Am27HB010 is ideal for use with the fastest processors due to the high speed random access time. This device also achieves maximum performance with all of today's "burstable" processors due to the extremely fast burst mode access time. Designers may take full advantage of high speed digital signal processors and microprocessors by allowing code to be executed at full speed directly out of EPROM.

The Am27HB010 is programmed using AMD's Flashrite™ programming algorithm which allows the entire chip to be programmed typically in less than 30 seconds.

This device is available in 32-pin windowed DIP as well as surface mount packages and is offered in commercial, industrial and extended temperature ranges.

BLOCK DIAGRAM



14970-001B

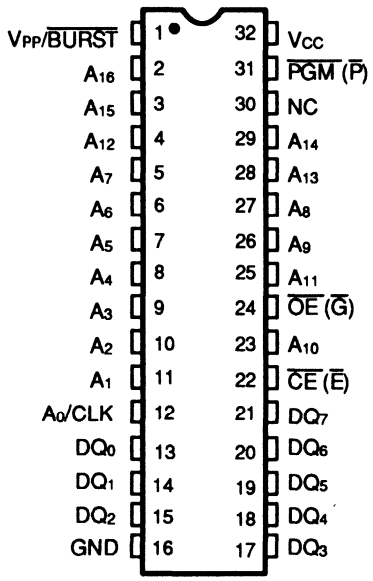
PRODUCT SELECTOR GUIDE

Family Part No.	Am27HB010		
Vcc ±5%	-50V05	-60V05	
Vcc ±10%	-50	-60	-90
Max Access Time (ns)	50	60	90
Burst Access (ns)	15	20	30
$\overline{CE}$ ($\overline{E}$) Access (ns)	50	60	90
$\overline{OE}$ ($\overline{G}$) Access (ns)	15	20	30

Publication # 14970 Rev. B Amendment /0
Issue Date: March 1991

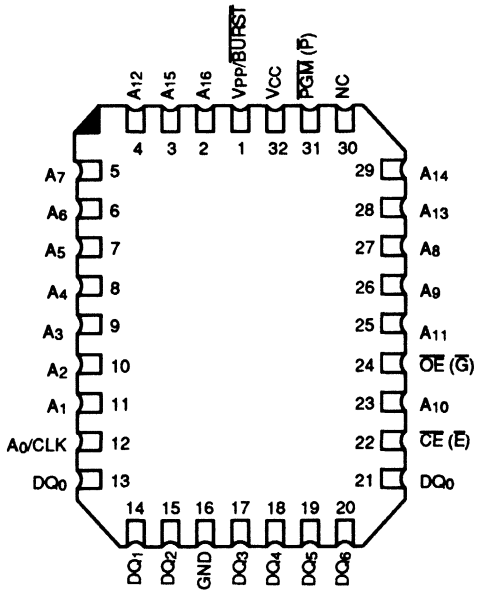
CONNECTION DIAGRAMS
Top View

DIP



14970-002B

LCC*



14970-003B

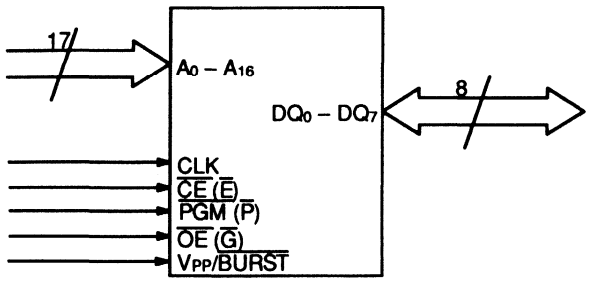
Note:
JEDEC nomenclature is in parenthesis

*Also available in a 32-pin PLCC.

PIN DESCRIPTION

A_0–A_{16}	Address Inputs	$\overline{PGM}$ ($\overline{P}$)	Program Enable Input
$\overline{CE}$ ($\overline{E}$)	Chip Enable Input	V_{CC}	V_{CC} Supply Voltage
DQ_0–DQ_7	Data Input/Outputs	$V_{PP}/\overline{BURST}$	Program Supply Voltage & Burst Enable
$\overline{OE}$ ($\overline{G}$)	Output Enable Input	GND	Ground
CLK	Clock	NC	No Internal Connection

LOGIC SYMBOL

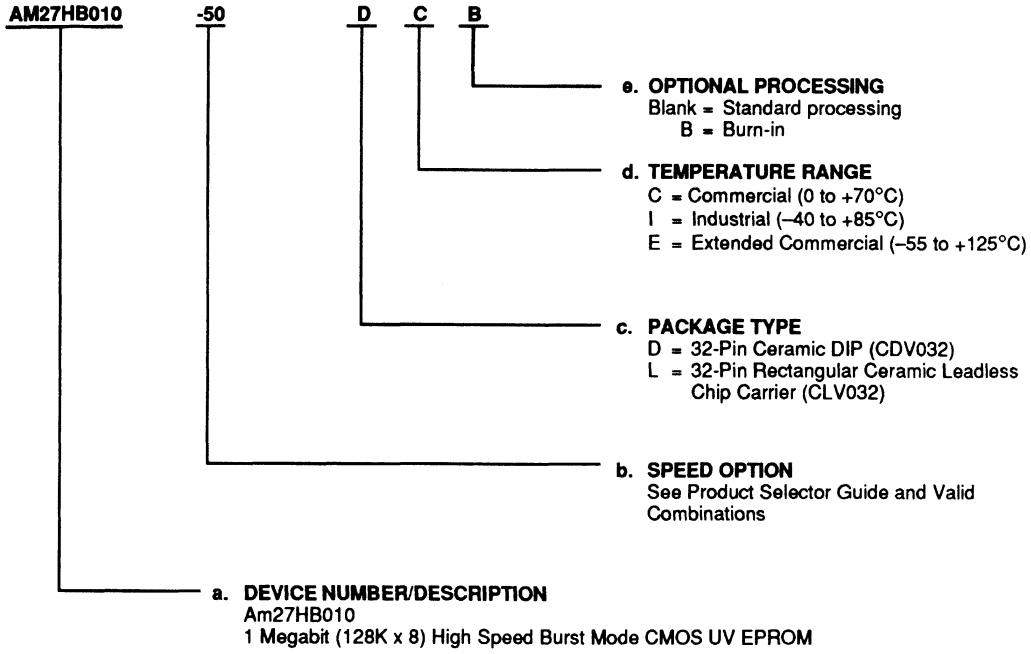


14970-004B

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27HB010-50	DC, DCB, DI, DIB, LC, LI, LCB, LIB
AM27HB010-50V05	
AM27HB010-60	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27HB010-90	

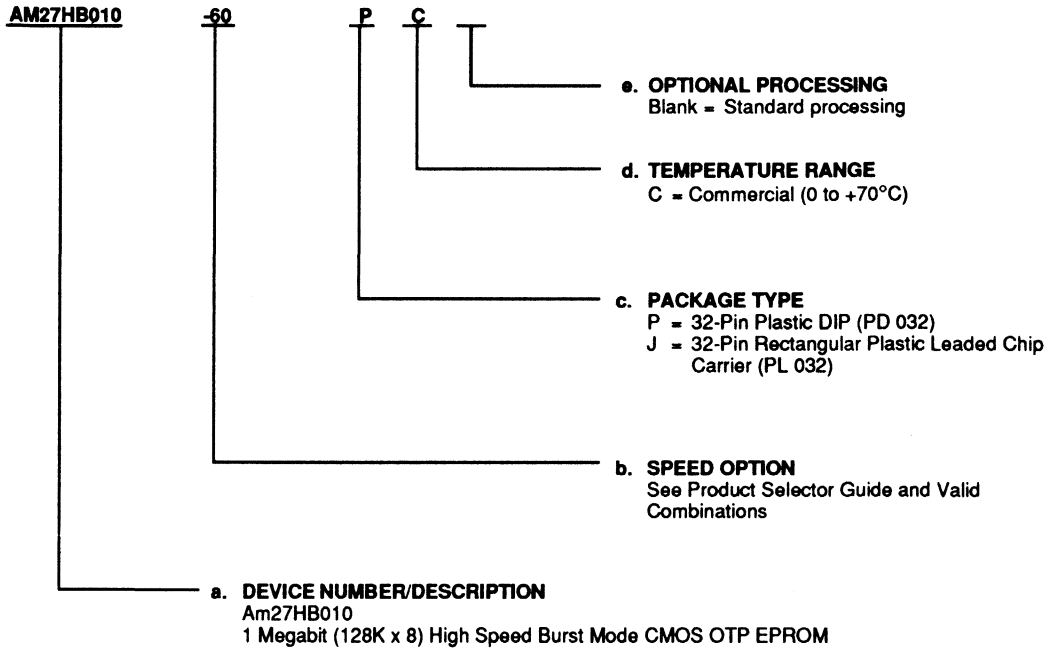
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
OTP Products (Preliminary)

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27HB010-60	PC, JC
AM27HB010-60V05	
AM27HB010-90	

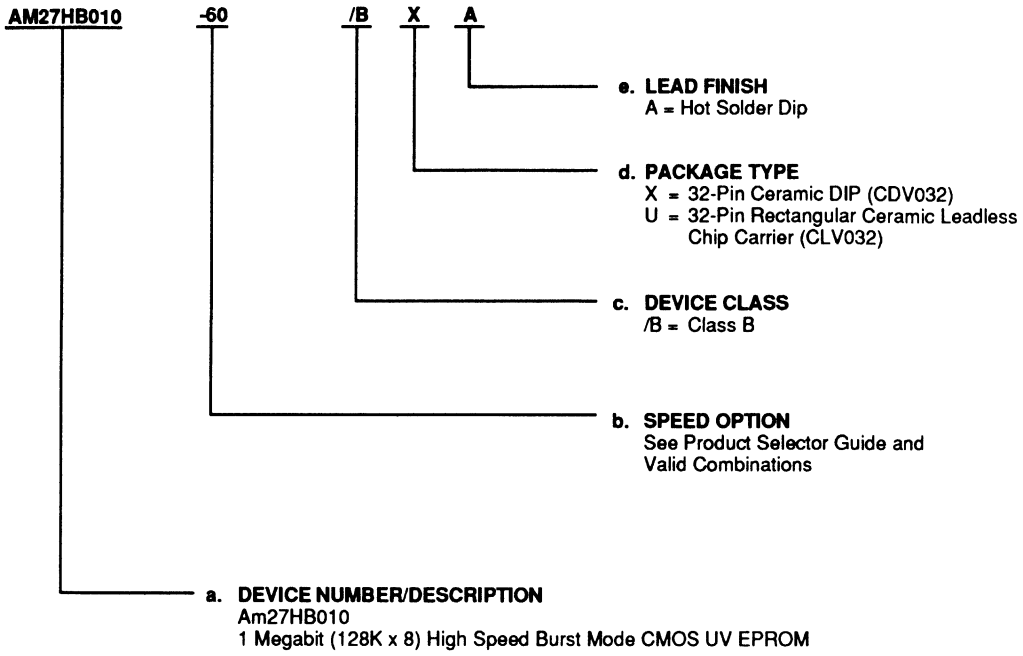
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27HB010-60	/BXA, /BUA
AM27HB010-90	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27HB010

In order to clear all locations of their programmed contents, it is necessary to expose the Am27HB010 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27HB010. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Angstroms (Å) — with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27HB010 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27HB010, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27HB010 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27HB010

Upon delivery, or after each erasure, the Am27HB010 has all 1,048,576 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27HB010 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, and $\overline{CE}$ and $\overline{PGM}$ are at V_{IL}, and $\overline{OE}$ is at V_{IH}. For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite programming algorithm reduces programming time by using initial 100 µs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.25 V.

Program Inhibit

Programming of multiple Am27HB010s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27HB010 may be common. A TTL low-level program pulse applied to an Am27HB010 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V, $\overline{PGM}$ is LOW, and $\overline{OE}$ HIGH will program that Am27HB010. A high-level $\overline{CE}$ input inhibits the other Am27HB010 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V to 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27HB010.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27HB010. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A_0 = V_{IL}) represents the manufacturer code, and byte 1 (A_0 = V_{IH}), the device identifier code. For the Am27HB010, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Random Read Mode

The Am27HB010 has three control functions that must be logically satisfied in order to obtain random access data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. $V_{PP}/\overline{BURST}$ must be at V_{IH}. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Initial Burst Access

The Am27HB010 will enter the burst-mode when both $V_{PP}/\overline{BURST}$ and $\overline{CE}$ are at logic '0'. The last pin to switch from V_{IH} to V_{IL} (either $V_{PP}/\overline{BURST}$ or $\overline{CE}$), will determine the exact entry into the burst-mode. At this time the addresses (A_0–A_{16}) are latched internally to the device for the remainder of the burst access. There are no boundary address conditions for entering the burst-mode. The access time for the initial access is measured from when the addresses ($A_1 - A_{16}$) are stable. The delay in A_0 will have no effect on access speed as long as the conditions listed in Switching Characteristics are met.

Burst Read Mode

After the initial access, sequential bytes of data may be accessed by toggling the A_0/CLK signal. Data will be available in the specified burst access time. There are no minimum or maximum amounts of data required for a burst. The device will perform a one byte burst or continue to the physical end of the device, 128K if required.

The device will also wrap around and go to the very beginning of the memory once the physical boundary of the device is reached. To exit burst mode, $V_{PP}/\overline{BURST}$ is toggled from V_{IL} to V_{IH}.

Burst Suspend Mode

Burst mode may be suspended by removing CE while V_{PP}/BURST is still at V_{IL}. To resume burst mode, V_{PP}/BURST remains at V_{IL} while CE is re-asserted. Data will then be available within the burst access time.

Standby Mode

The Am27HB010 has a TTL standby mode which reduces the maximum V_{CC} current to 20% of the active current. It is placed in standby mode when $\overline{CE}$ and $V_{PP}/\overline{BURST}$ is at V_{IH}. The amount of current drawn in standby mode depends on the frequency and the number of address pins switching. The Am27HB010 is specified with 50% of the address lines toggling at 10 MHz. A reduction of the frequency or quantity of address lines toggling will significantly reduce the actual standby current. The V_{CC} DC current can further be decreased to 1 mA by placing all inputs at steady CMOS logic levels.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_0/CLK	A_9	$V_{PP}/\overline{BURST}$	Outputs
Read		V_{IL}	V_{IL}	X	X	X	V_{IH}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	Hi-Z
Standby		V_{IH}	X	X	X	X	V_{IH}	Hi-Z
BURST Enable		V_{IL}	V_{IL}	X	X	X	V_{IL}	D_{OUT}
BURST Suspend (Note 7)		V_{IH}	V_{IH}	X	X	X	V_{IL}	Hi-Z
BURST Suspend (Note 7)		V_{IH}	V_{IL}	X	X	X	V_{IL}	D_{OUT}
BURST Read		V_{IL}	V_{IL}	X	L-H	X	V_{IL}	D_{OUT}
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	Hi-Z
Auto Select (Notes 3 & 5)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	V_{IH}	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	V_{IH}	0EH

Notes:

1. $V_H = 12.0\ V \pm 0.5\ V$
2. X = Either V_{IL} or V_{IH} (cannot exceed $V_{CC} + 0.5\ V$)
3. $A_1 - A_8 = A_{10} - A_{16} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.
5. The Am27HB010 uses the same Flashrite algorithm during program as the Am27C010.
6. $V_{IL} < 0.8\ V$; $V_{IH} > 2.0\ V$
7. BURST suspend is entered only when $\overline{CE}$ toggles from V_{IL} to V_{IH} during Burst Mode operation.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP product	–65 to +125°C
All other products	–65 to +150°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC} (Note 1)	–0.6 to V_{CC} +0.6 V
A_9 and V_{PP} (Note 2)	–0.6 to 13.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. This is a stress rating only; functional operation of the device at these limits or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum ratings for extended periods may affect device reliability.

Notes:

1. During transitions, the input may overshoot GND to –2.0 V for periods of up to 10 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods of up to 10 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 10 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (Tc)	0 to +70°C
Industrial (I) Devices	
Case Temperature (Tc)	–40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (Tc)	–55 to +125°C
Military (M) Devices	
Case Temperature (Tc)	–55 to +125°C
Supply Read Voltages:	
V_{CC} for Am27HB010-XXV05	+4.75 to +5.25 V
V_{CC} for Am27HB010-XX	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 4, 5 & 8) (for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA (C Devices) I_{OL} = 10 mA (I Devices) I_{OL} = 8 mA (E/M Devices)			0.45	V
V_{IH}	Input HIGH Voltage (Note 9)			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage (Note 9)			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC} + 0.5 V		1.0		µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to + V_{CC}			10	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		100	mA
			E/M Devices		120	
I_{CC2}	V_{CC} Standby Current (TTL)	$\overline{CE}$ = V_{IH}, $V_{PP}/\overline{BURST}$ = V_{IH}	C/I Devices		25	mA
			E/M Devices		35	
I_{CC3}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} – 0.3 V to V_{CC} + 0.5 V $V_{PP}/\overline{BURST}$ = V_{CC} – 0.3 V to V_{CC} + 0.5 V			1.0	mA
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV032		CLV032		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	6	12	6	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{IN} = 0 V	12	20	12	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	10	15	8	15	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled, not 100% tested.
4. **Caution**: The Am27HB010 must not be removed from (or inserted into) a socket when V_{PP} or V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP1}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the inputs may overshoot to –2.0 V for periods less than 10 ns.
   Maximum DC voltage on output pins may overshoot to V_{CC} + 2.0 V for periods less than 10 ns.
9. Tested under static DC conditions.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

Parameter Symbols		Parameter Description	Test Conditions	Am27HB010			Unit
JEDEC	Standard			-50 -50V05	-60 -60V05	-90	
t_{AVQV}	t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$, $C_L = C_{L1}$	50	60	90	ns
	t_{BACC}	Burst Access Time	$\overline{CE} = \overline{OE} = V_{PP}/\overline{BURST} = V_{IL}$, $C_L = C_{L1}$	15	20	30	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$, $C_L = C_{L1}$	50	60	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$, $C_L = C_{L1}$	15	20	30	ns
t_{GHQZ}	t_{DF} (Note 2)	Output Enable to Output Float	$\overline{CE} = V_{IL}$, $C_L = C_{L2}$	10	15	25	ns
	t_{SET}	Address Setup to BURST or $\overline{CE}$ Enable	$\overline{CE} = V_{IL}$, $C_L = C_{L1}$	10	15	25	ns
	t_{HOLD}	Address Hold to BURST or $\overline{CE}$ Enable	$\overline{CE} = V_{IL}$, $C_L = C_{L1}$	0	0	0	ns
	$t_{BCLKLOW}$	Minimum Low Time for for A_0 to Start BURST	$\overline{CE} = \overline{OE} = V_{PP}/\overline{BURST} = V_{IL}$, $C_L = C_{L1}$	10	15	20	ns
	t_{BSUSPS}	BURST Suspend Setup Time	$V_{PP}/\overline{BURST} = V_{IL}$, $C_L = C_{L1}$	10	15	25	ns
	t_{BSUSPH}	BURST Suspend Hold Time	$V_{PP}/\overline{BURST} = V_{IL}$ $C_L = C_{L1}$	10	15	25	ns
	t_{BRES}	BURST Resume Setup Time	$V_{PP}/\overline{BURST} = V_{IL}$, $C_L = C_{L1}$	10	15	25	ns
	$t_{BTERMCLK}$	BURST Terminate Setup to A_0/CLOCK Time	$V_{PP}/\overline{BURST} = V_{IH}$, $C_L = C_{L1}$	10	15	25	ns
	t_{BCLK}	Minimum CLOCK HIGH Time (Note 7)	$\overline{CE} = \overline{OE} = V_{PP}/\overline{BURST} = V_{IL}$, $C_L = C_{L1}$	6	8	13	ns
	t_{BCLKB}	Minimum CLOCK LOW Time (Note 7)	$\overline{CE} = \overline{OE} = V_{PP}/\overline{BURST} = V_{IL}$, $C_L = C_{L1}$	6	8	13	ns

Notes:

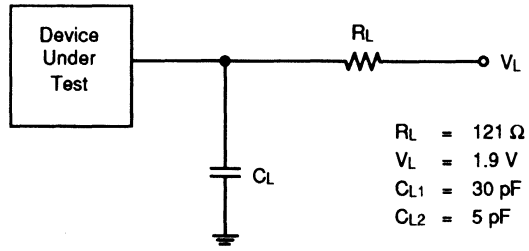
1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled, not 100% tested.
3. **Caution**: The Am27HB010 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and $C = C_L$
   Input Rise and Fall Times: 3 ns for -50; 5 ns for -60; 7 ns for -90
   Input Pulse Levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V for inputs and outputs
5. Transient Input Low Voltages to –2.0 V with 10 ns duration at the 50% amplitude point are permitted.
6. To guarantee Initial Burst Access, $t_{SET} + t_{BCLKLOW} + t_{HOLD} \geq t_{ACC}$.
7. Burst clocks should have 50% duty cycle. Clock skews are allowed as long as minimum t_{BCLK} and t_{BCLKB} specifications are met and $t_{BACC} = t_{BCLK} + t_{BCLKB}$.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

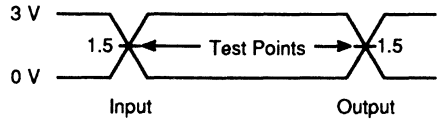
KS000010

SWITCHING TEST CIRCUIT



14970-005B

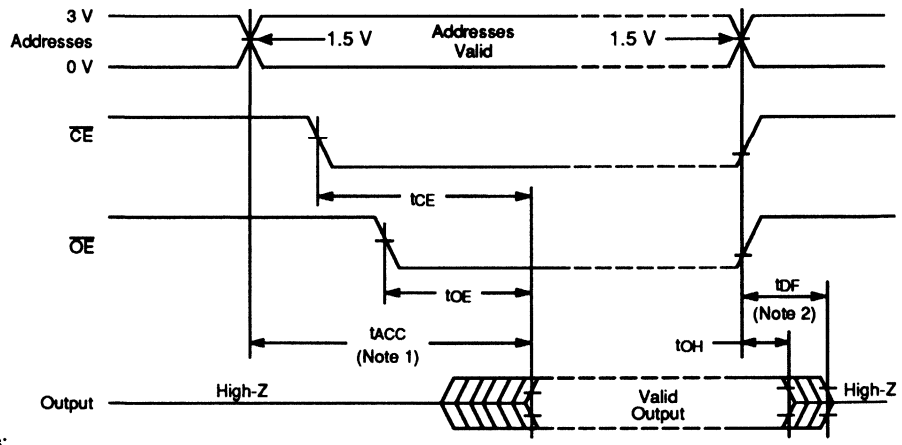
SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 for a logic "0". Input pulse rise and fall times are < 3 ns for –50; < 5 ns for –60; and < 7 for –90.

14970-006B

SWITCHING WAVEFORMS (Read Timings—Random Access Mode)

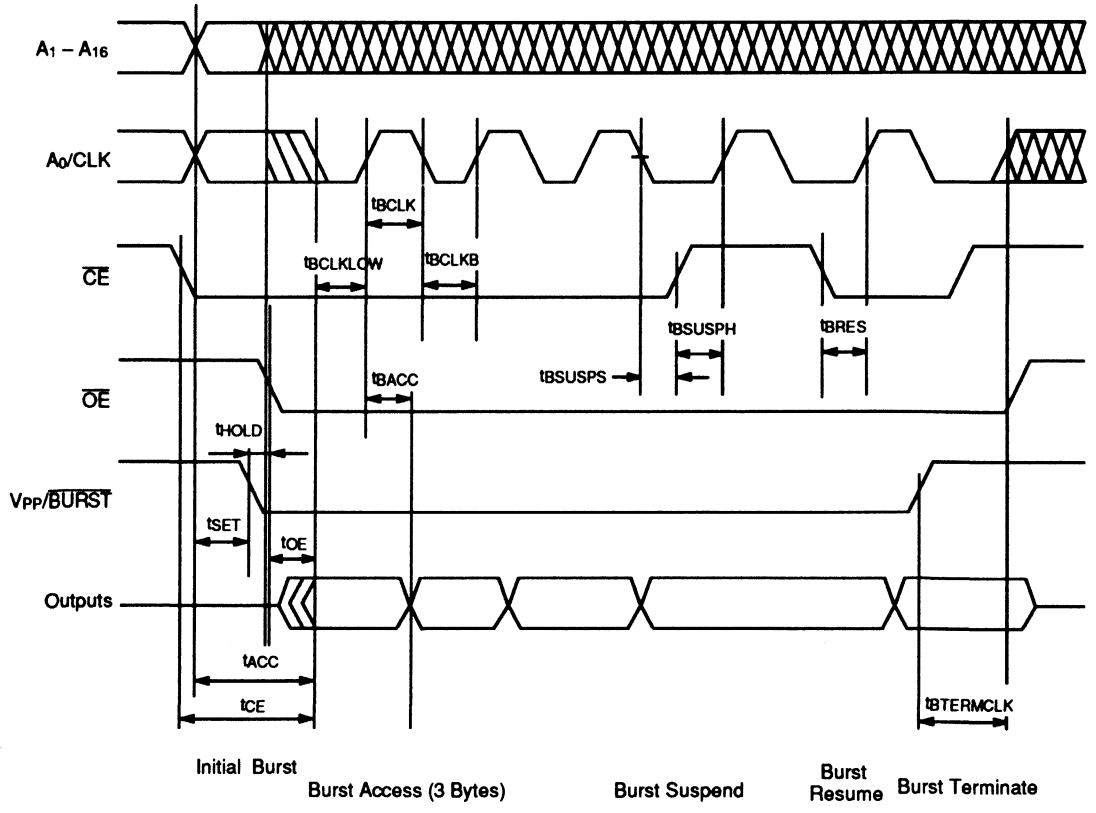


Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

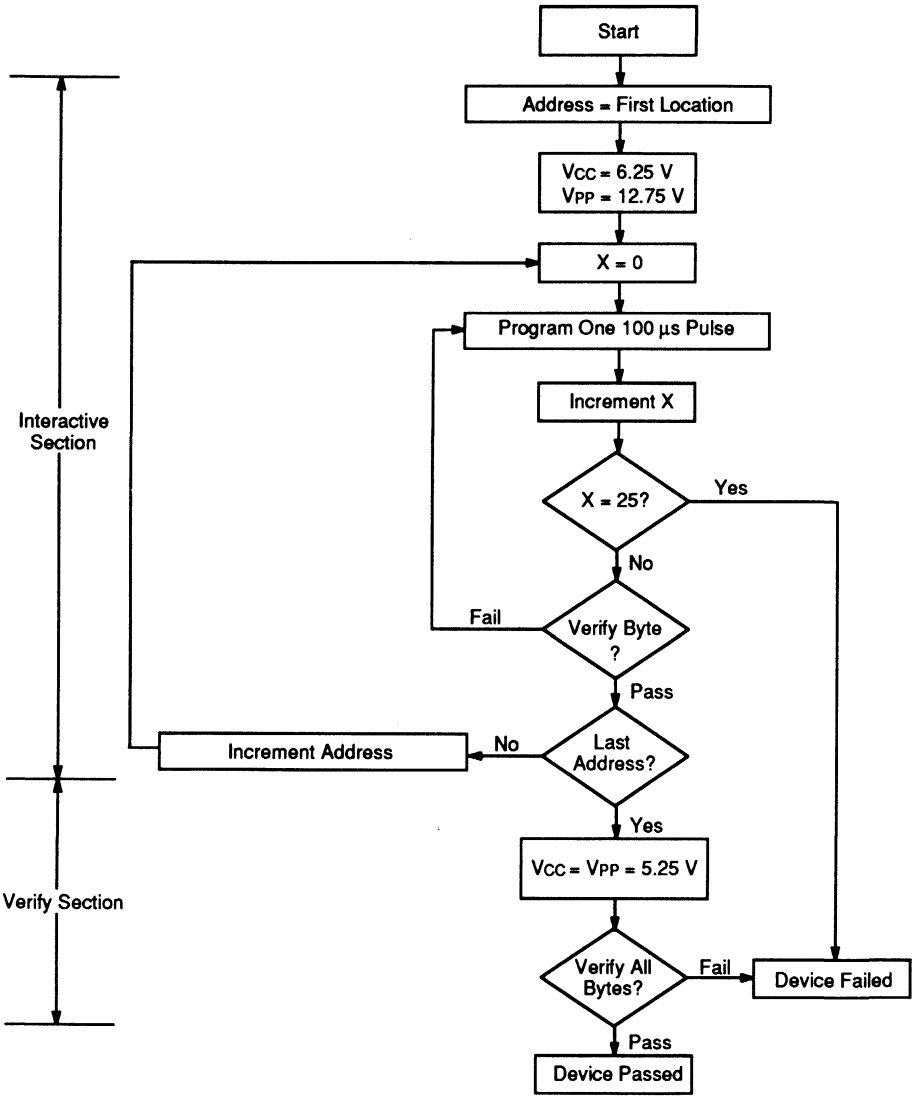
14970-007B

SWITCHING WAVEFORMS (Burst Mode)



14970-008B

PROGRAMMING FLOW CHART



14970-009B

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.3	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 12 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –4 mA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC3}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		50	mA
V_{CC1}	Supply Voltage		6.00	6.50	V
V_{PP}	Programming Voltage		12.5	13.0	V

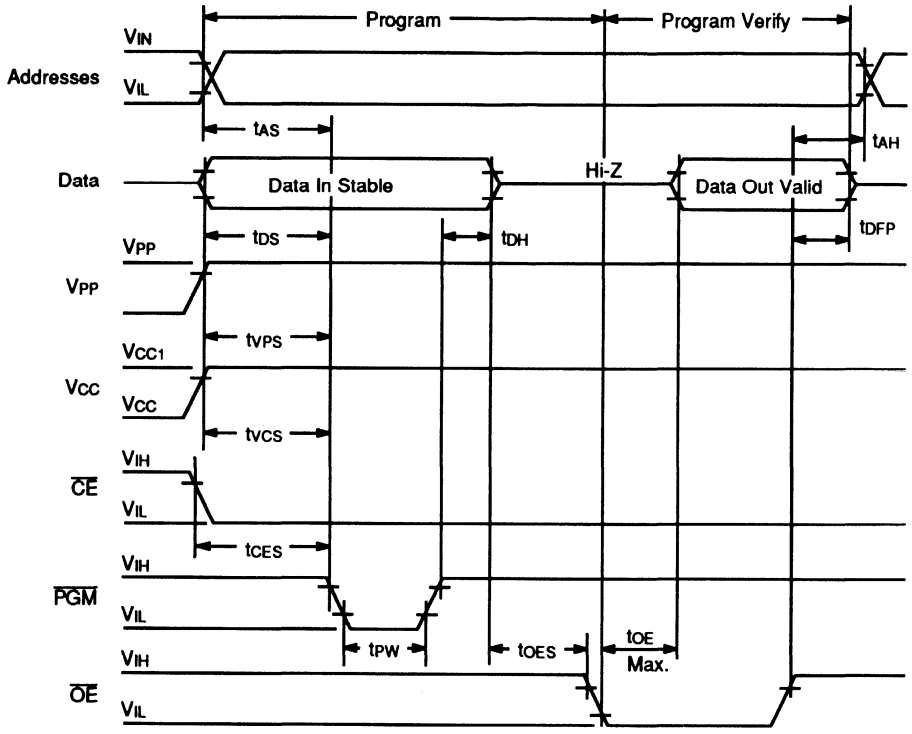
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		75	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27HB010, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

PROGRAMMING ALGORITHM WAVEFORM (Notes 1 & 2)



14970-010B

Notes:

1. The input timing reference level is 0.8 for a V_{IL} and 2 V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Am27C100

1Megabit (131,072 x 8-Bit) ROM Compatible CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **EIAJ 32-pin DIP package**
- **Pinout compatible with 28-pin ROM**
- **Fast access time**
  - 100 ns
- **Low power consumption**
  - 100 µA typical standby current
- **High speed Flashrite™ programming**
- **Single + 5 V power supply**
- **± 10% power supply tolerance available**
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**

GENERAL DESCRIPTION

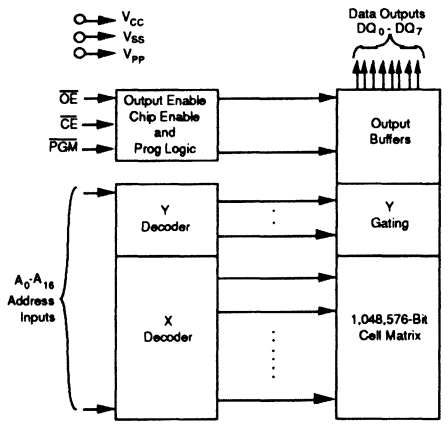
The Am27C100 is a 1 megabit ultraviolet erasable programmable read-only memory. The 32 pin EIAJ pinout is compatible with 28 pin megabit ROMs. The memory is organized as 128K words by 8 bits per word, operates from a single + 5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and plastic one time programmable (OTP) packages.

Any byte can be accessed in less than 120 ns, allowing operation with many high-performance microprocessors without any WAIT states. The Am27C100 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C100 supports AMD's Flashrite programming algorithm (0.1 ms pulses) resulting in typical programming times of less than 30 seconds.

BLOCK DIAGRAM



12566-001A

PRODUCT SELECTOR GUIDE

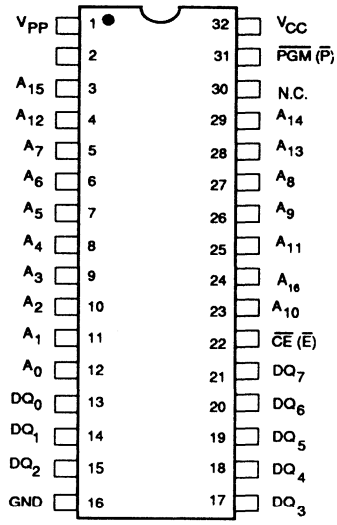
Family Part No.	Am27C100				
Ordering Part Number: V_{CC} ± 5%	-105	-125	-155		-255
V_{CC} ± 10%		-120	-150	-200	
Max. Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)		50	65	75	100

Publication# 12566 Rev. B Amendment /0
Issue Date: March 1991

CONNECTION DIAGRAM

Top View

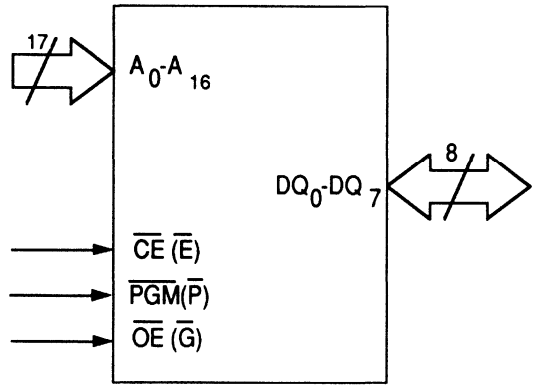
DIPs



12566-002A

Note:
1. JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



10205A-002A

PIN DESCRIPTION

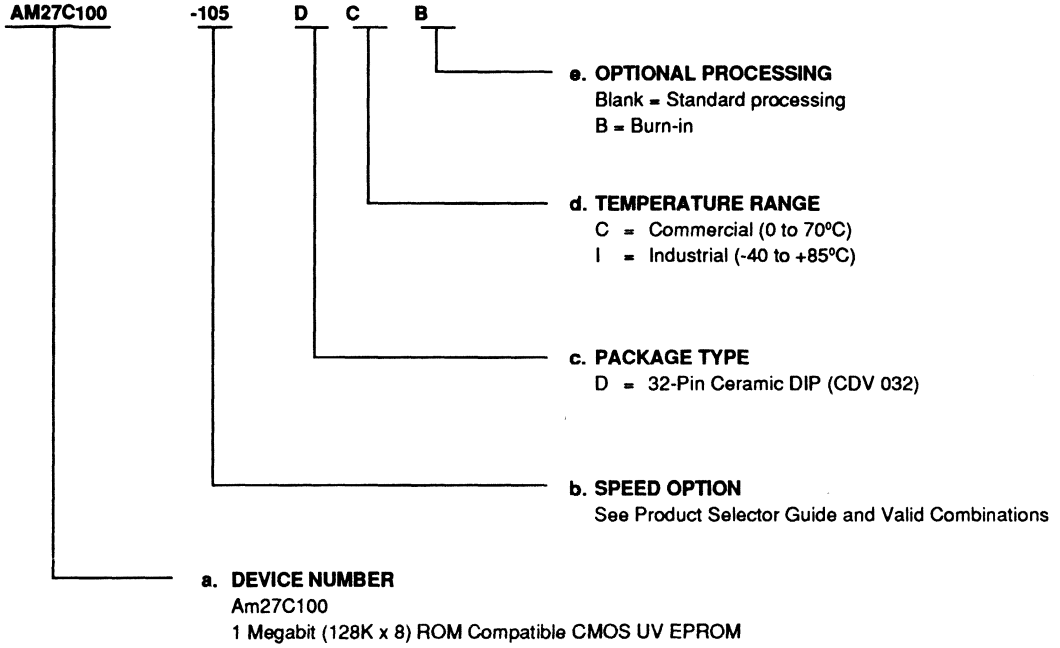
A_0–A_{16}	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ_0–DQ_7	=	Data Input/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connect

ORDERING INFORMATION

Standard Information

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27C100-105	DC, DCB
AM27C100-120	DC, DCB, DI, DIB
AM27C100-125	
AM27C100-150	
AM27C100-155	
AM27C100-200	
AM27C100-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing

AM27C100 -125 P C

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)

b. SPEED OPTION
See Product Selector Guide and Valid Combinations

a. DEVICE NUMBER
Am27C100
1 Megabit (128K x 8) CMOS ROM compatible OTP EPROM

Valid Combinations	
AM27C100-125	PC
AM27C100-155	
AM27C100-200	
AM27C100-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Erasing the Am27C100

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C100 to an ultraviolet light source. A dosage of 15 W seconds/cm² is required to completely erase an Am27C100. This dosage can be obtained by exposure to an ultraviolet Lamp-wavelength of 2537 Angstroms (Å)–with intensity of 12,000 µW/cm² for 15 to 20 minutes. The Am27C100 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C100, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C100 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C100

Upon delivery, or after each erasure, the Am27C100 has all 1,048,576 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C100 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ and $\overline{PGM}$ is at V_{IL}, and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite programming algorithm (shown in Figure 1) reduces programming time by using initial 100 µs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with $V_{CC} = V_{PP}$ = 5.25 V.

Program Inhibit

Programming of multiple Am27C100s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C100s may be common. A TTL low-level program pulse applied to an Am27C100 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V, $\overline{PGM}$ is LOW, and $\overline{OE}$ HIGH will program that Am27C100. A high-level $\overline{CE}$ input inhibits the other Am27C100s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C100.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C100. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and byte 1($A_0 = V_{IH}$), the device identifier code. For the Am27C100, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C100 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C100 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C100 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in stand-by mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	X	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	X	Hi-Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	Hi-Z
Auto Select	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	01H
(Note 3)	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	0DH

Notes:

1. $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$
2. X = Either V_{IH} or V_{IL}
3. $A_1 - A_8 = A_{10} - A_{16} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature

OTP products	–65 to 125°C
All other products	–65 to 150°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC} (Note 1)	–0.6 to V_{CC} +0.6 V
A_9 and V_{PP} (Note 2)	–0.6 to 13.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. During transitions, the inputs may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0 to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	–40 to +85°C
Supply Read Voltages:	
V_{CC} for Am27C100-XX5	+4.75 to + 5.25 V
V_{CC} for Am27C100-XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 4, 5, and 8)

TTL and NMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+ V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+ V_{CC}$		10	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE} = V_{IL}$, f =5 MHz $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CMOS Inputs

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+ V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+ V_{CC}$		10	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 2, 3, and 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV032		Unit
			Typ.	Max.	
C_{IN}	Address Input Capacitance	V_{IN} = 0 V	12	14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	14	17	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled, not 100% tested.
4. **Caution:** the Am27C100 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
5. I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = +25°C, f = 1 MHz.
8. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on input pins may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.

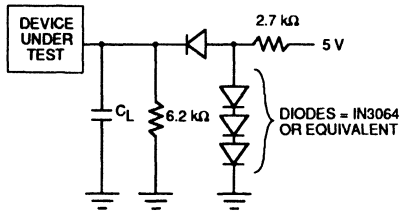
SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 3, and 4)

Parameter Symbols		Parameter Description	Test Condition		Am27C100					Unit
JEDEC	Standard				-105	-120, -125	-150, -155	-200	-255	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.		–	–	–	–	ns
				Max.	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.		–	–	–	–	ns
				Max.	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.		–	–	–	–	ns
				Max.	50	50	65	75	100	
t_{EHQZ}	t_{DF}	Chip Enable HIGH or Output Enable HIGH, Whichever Comes First, to Output Float		Min.		0	0	0	0	ns
t_{GHQZ}	(Note 2)			Max.	35	35	35	40	40	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, Whichever Occurred First		Min.	0	0	0	0	0	ns
				Max.		–	–	–	–	

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled, not 100% tested.
3. **Caution:** The Am27C100 must not be removed from (or inserted into) a socket or board when V_{pp} or V_{cc} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level - Inputs: 0.8 to 2.0 V
   Outputs: 0.8 to 2.0V

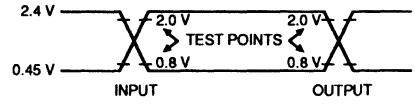
SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance.

10205A-004A

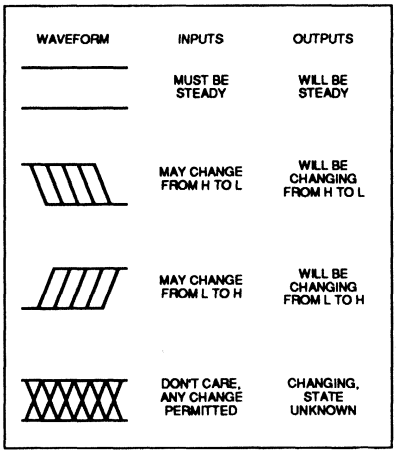
SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 20 ns.

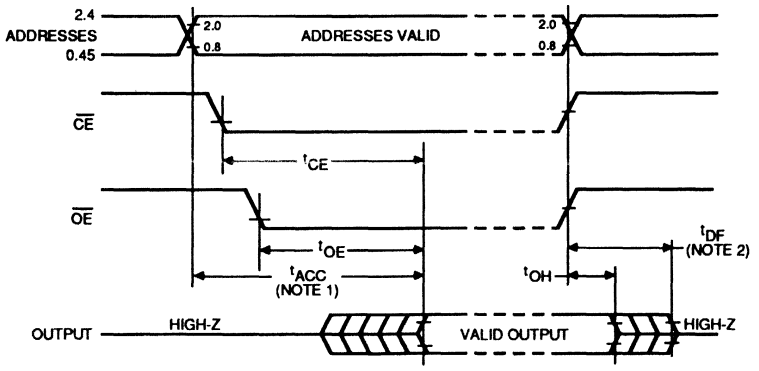
10205B-009A

KEY TO SWITCHING WAVEFORMS



KS000010

SWITCHING WAVEFORMS



10205A-005A

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

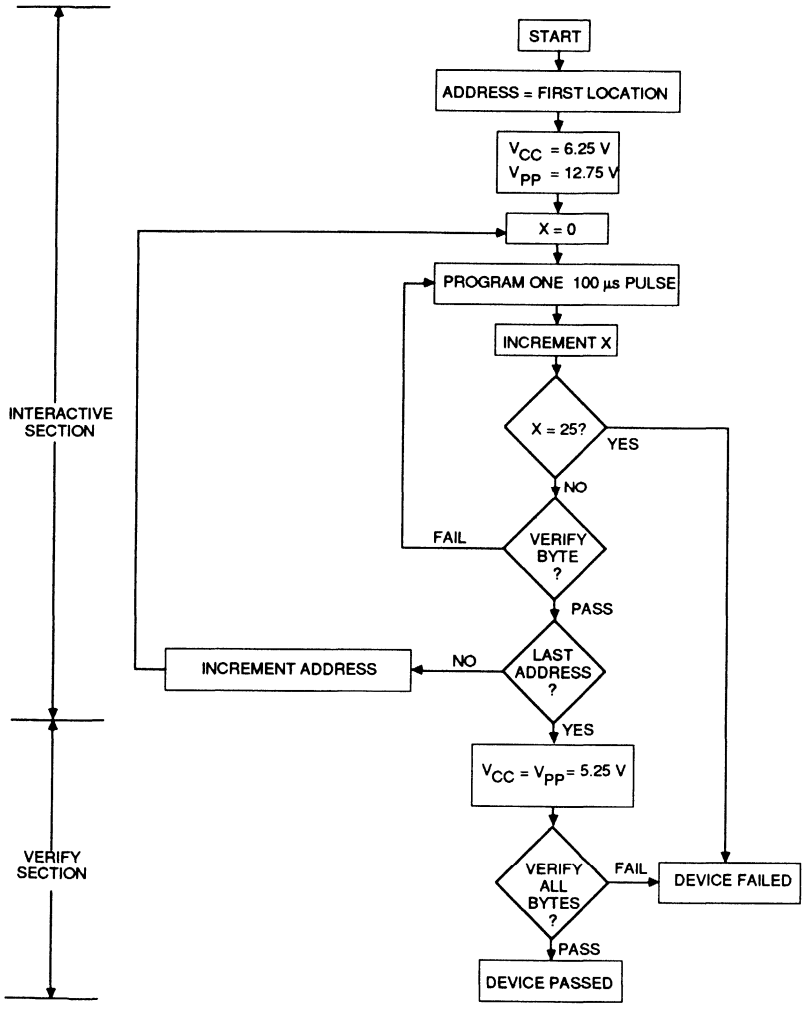


Figure 1. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ± 5°C) (Notes 1, 2, and 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	µA
V_{IL}	Input LOW Level (All Inputs)		– 0.3	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = – 400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	CE = V_{IL}, $\overline{OE}$ = V_{IH}		30	mA
V_{CC}	Supply Voltage		6.00	6.50	V
V_{PP}	Programming Voltage		12.5	13.0	V

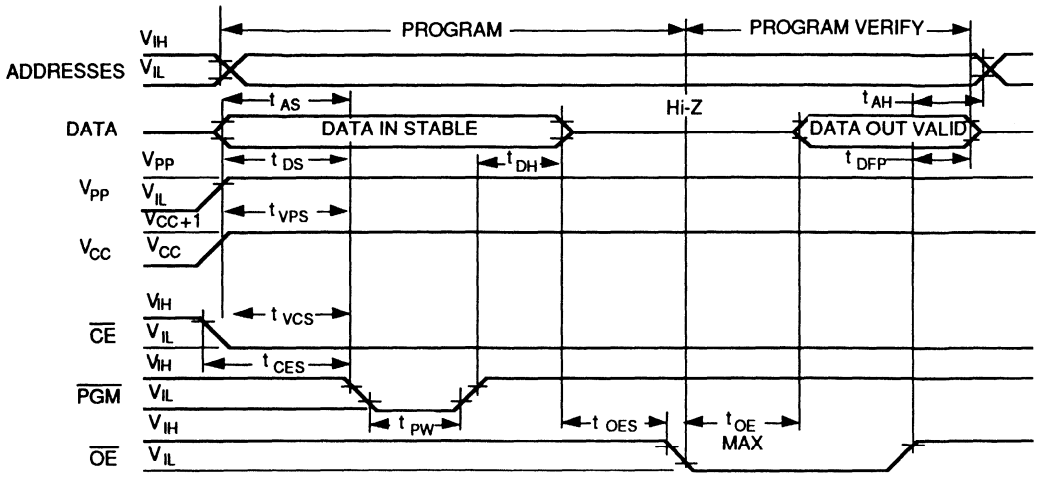
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ± 5°C) (Notes 1, 2, and 3)

Parameter Symbol		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C100, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

Flashrite PROGRAMMING ALGORITHM WAVEFORM (Notes 1 and 2)



Notes:

1. The input timing reference level is 0.8 V for V_{IL} ans 2.0 V for a V_{IH}.
2. t_{OE} and t_{DFB} are characteristics of the device but must be accommodated by the programmer.

Am27C1024

1 Megabit (65,536 x 16-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High Speed Flashrite™ programming**
- **Fast access time — 100 ns**
- **Low power consumption:**
  - 100 µA maximum standby current
- **Programming voltage: 12.75 V**
- **Single +5-V power supply**
- **JEDEC-approved 40-pin DIP and 44 pad LCC pinouts**
- **±10% power supply tolerance available**
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**

GENERAL DESCRIPTION

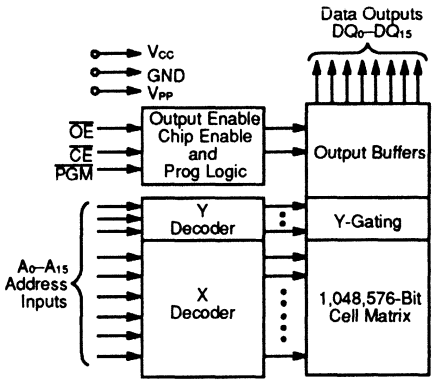
The Am27C1024 is a 1 megabit, ultraviolet erasable programmable read-only memory. It is organized as 64K words by 16 bits per word, operates from a single +5-V supply, has a static standby mode, and features fast single address location programming. The x16 organization makes the Am27C1024 ideal for use in 16-bit microprocessor systems. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

Any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors with reduced WAIT states. The Am27C1024 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 350 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C1024 supports AMD's Flashrite programming algorithm (100 µs pulses) resulting in typical programming times of less than 20 seconds.

BLOCK DIAGRAM



06780-001E

PRODUCT SELECTOR GUIDE

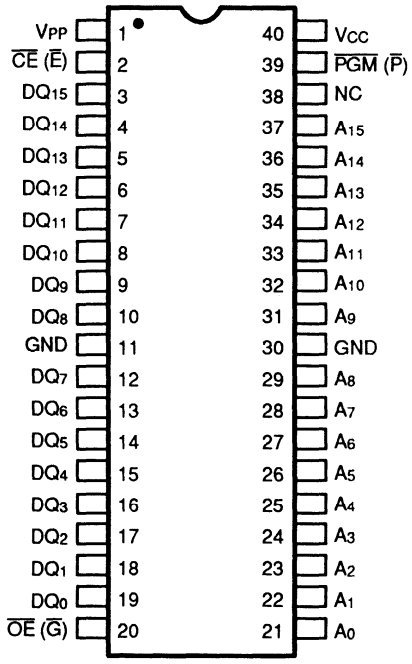
Family Part No.	Am27C1024				
Ordering Part No:					
±5% Vcc Tolerance	-105	-125			-255
±10% Vcc Tolerance		-120	-150	-200	-250
Max. Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	50	65	75	100

Publication# 06780 Rev. F Amendment/0
Issue Date: March 1991

CONNECTION DIAGRAMS

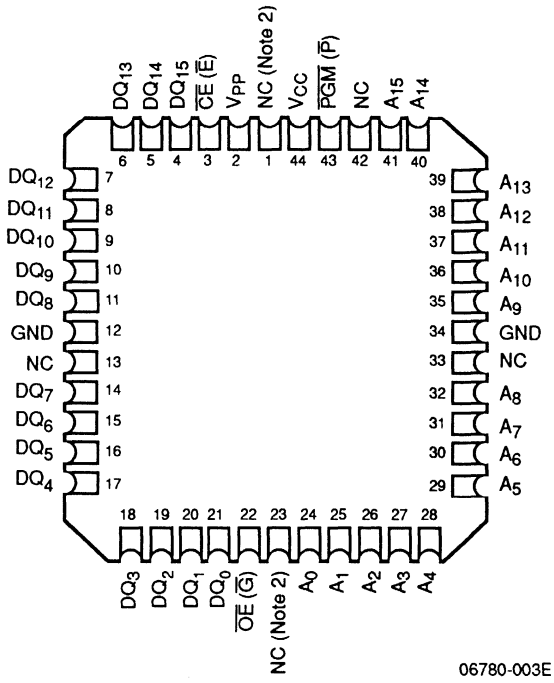
Top View

DIPs



06780-002E

LCC*



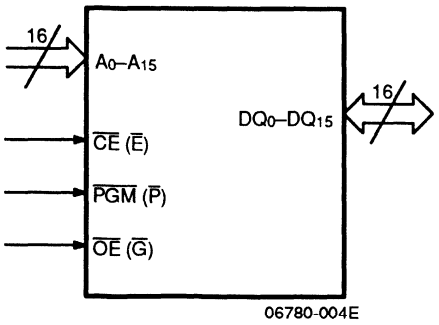
06780-003E

*Also available in a 44-Pin Plastic Leaded Chip Carrier.

Notes:

1. JEDEC nomenclature is in parenthesis.
2. Don't use (DU) for PLCC.

LOGIC SYMBOL



06780-004E

PIN DESCRIPTION

A0–A15
Address Inputs

CE (E)
Chip Enable Input

DQ0–DQ15
Data Input/Outputs

OE (G)
Output Enable Input

PGM (P)
Program Enable Input

VCC
VCC Supply Voltage

VPP
Program Supply Voltage

GND
Ground

NC
No Internal Connect

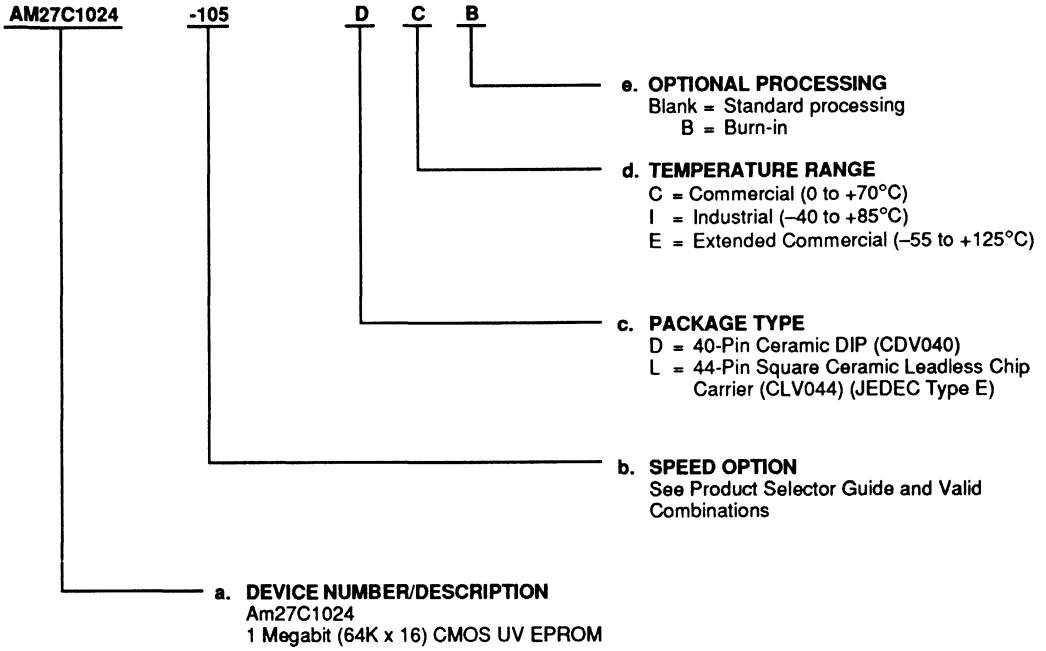
DU
No External Connect

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C1024-105	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C1024-125	
AM27C1024-120	DC, DCB, DI, DIB, DE, DEB, LCB, LIB, LE, LEB, LC, LI
AM27C1024-150	
AM27C1024-200	
AM27C1024-255	

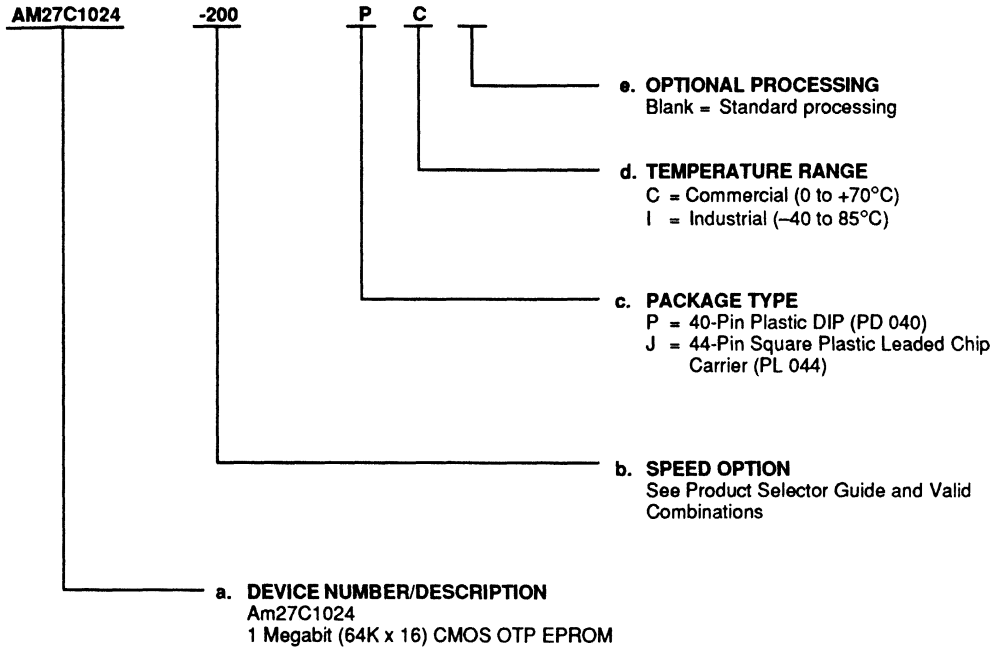
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C1024-200	PC, JC, PI, JI
AM27C1024-255	

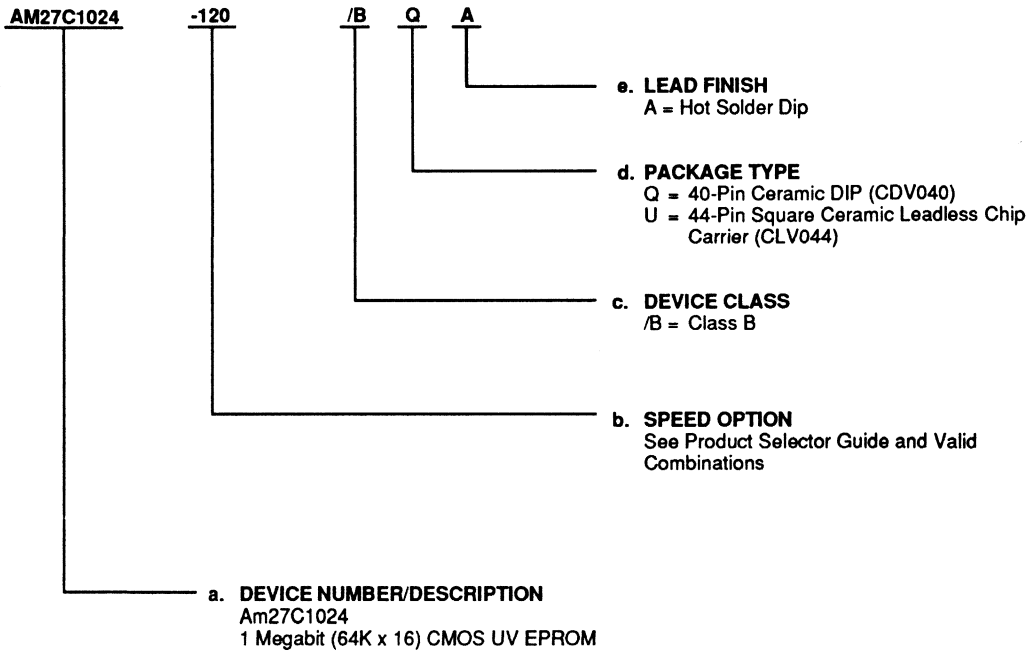
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27C1024-120	/BQA, /BUA
AM27C1024-150	
AM27C1024-200	
AM27C1024-250	

For other Surface Mount Package options, contact NVD Military Marketing.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C1024

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C1024 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C1024. This dosage can be obtained by exposure to an ultraviolet lamp —wavelength of 2537 Angstroms (Å) —with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C1024 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C1024, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C1024 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C1024

Upon delivery, or after each erasure, the Am27C1024 has all 1,048,576 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C1024 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, and $\overline{CE}$ and $\overline{PGM}$ are at V_{IL}.

For programming, the data to be programmed is applied 16 bits in parallel to the data pins.

The Flashrite programming algorithm (shown in Figure 1) reduces programming time by using initial 100 µs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.25 V.

Program Inhibit

Programming of multiple Am27C1024s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C1024 may be common. A TTL low-level program pulse applied to an Am27C1024 $\overline{CE}$ input with V_{PP} = 12.75 ± .25 V and $\overline{PGM}$ LOW will program that Am27C1024. A high-level $\overline{CE}$ input inhibits the other Am27C1024s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$, at V_{IL}, PGM at V_{IH}, and V_{PP} between 12.75 V ± .25 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C1024.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C1024. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A_0 = V_{IL}) represents the manufacturer code, and Byte 1 (A_0 = V_{IH}), the device identifier code. For the Am27C1024, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C1024 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C1024 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C1024 also has a TTL-standby mode which reduce the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a

common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_0	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	V_{IH}	X	X	V_{CC}	D_{OUT}
Output Disable		V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	High Z
Standby (TTL)		V_{IH}	X	X	X	X	V_{CC}	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	V_{CC}	High Z
Program		V_{IL}	X	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_H	V_{CC}	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_H	V_{CC}	8CH

Notes:

1. X can be either V_{IL} or V_{IH}
2. $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$
3. $A_1 - A_8 = A_{10} - A_{15} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	–65 to +125°C
All Other Products	–65 to +150°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC} (Note 1)	–0.6 to V_{CC} +0.6 V
A_9 and V_{PP} (Note 2)	–0.6 to 13.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Notes:

1. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0 to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	–40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (T_C)	–55 to +125°C
Military (M) Devices	
Case Temperature (T_C)	–55 to +125°C
Supply Read Voltages:	
V_{CC}/V_{PP} for Am27C1024-XX5	+4.75 to +5.25 V
V_{CC}/V_{PP} for Am27C1024-XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 4, 5 & 8)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
TTL and NMOS Inputs						
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		10	µA
			E/M Devices		10	
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		50	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	C/I Devices		1.0	mA
			E/M Devices		1.5	
I_{PP1}	V_{PP} Supply Current (Read)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA
CMOS Inputs						
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			V_{CC} – 0.3	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		10	µA
			E/M Devices		10	
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		50	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	C/I Devices		100	µA
			E/M Devices		100	
I_{PP1}	V_{PP} Supply Current (Read) (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV040		CLV044		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	6	10	6	9	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	10	12	7	9	pF
C_{IN3}	$\overline{CE}$ & $\overline{PGM}$ Input Capacitance	V_{IN} = 0 V	10	12	7	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	14	6	9	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution**: The Am27C1024 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. Minimum DC input voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.

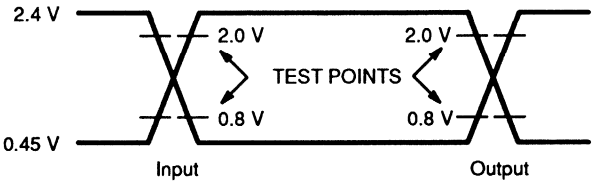
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

JEDEC	Standard	Parameter Description	Test Conditions		Am27C1024					Unit
					-105	-120, -125	-150	-200	-255, -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.						ns
				Max.	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.						ns
				Max.	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.						ns
				Max.	50	50	65	75	100	
t_{EHQZ}, t_{GHQZ}	t_{DF}	Output Enable HIGH to Output Float (Note 2)		Min.	0	0	0	0	0	ns
				Max.	40	50	55	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	ns
				Max.						

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution**: The Am27C1024 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: 20 ns, Input Pulse Levels: 0.45 to 2.4 V, Timing Measurement Reference Level—Inputs: 0.8 V and 2 V, Outputs: 0.8 V and 2 V.

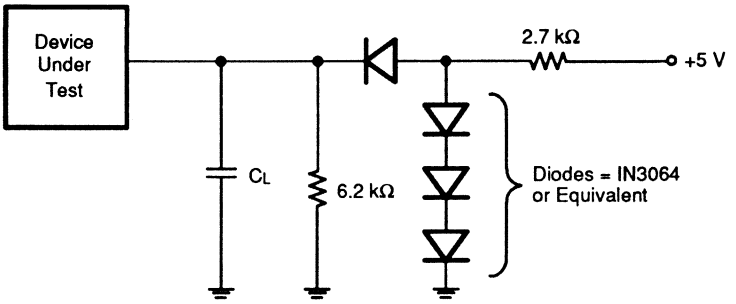
SWITCHING TEST WAVEFORM



06780-005E

AC Testing: Input are driven at 2.4 V for a Logic "1" and 0.45 for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

SWITCHING TEST CIRCUIT



06780-006E

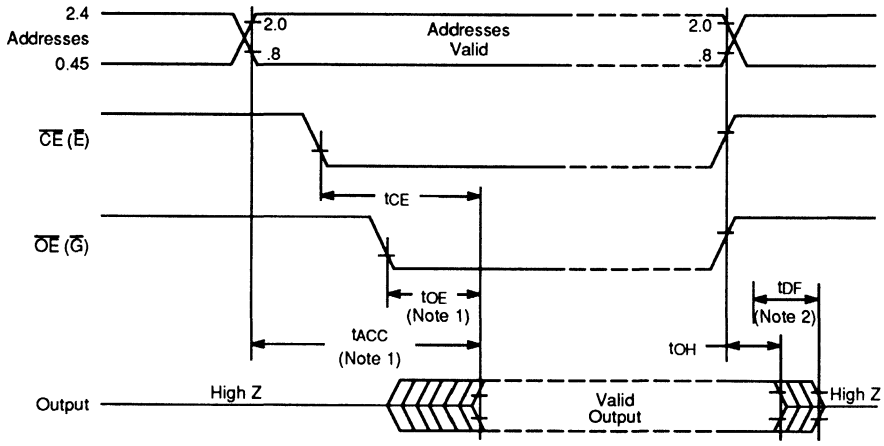
C_L = 100 pF including jig capacitance

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORM



06780-007E

Notes:

1. $\overline{OE}$ ($\overline{G}$) may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ ($\overline{E}$) without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Read Cycle

PROGRAMMING FLOW CHART

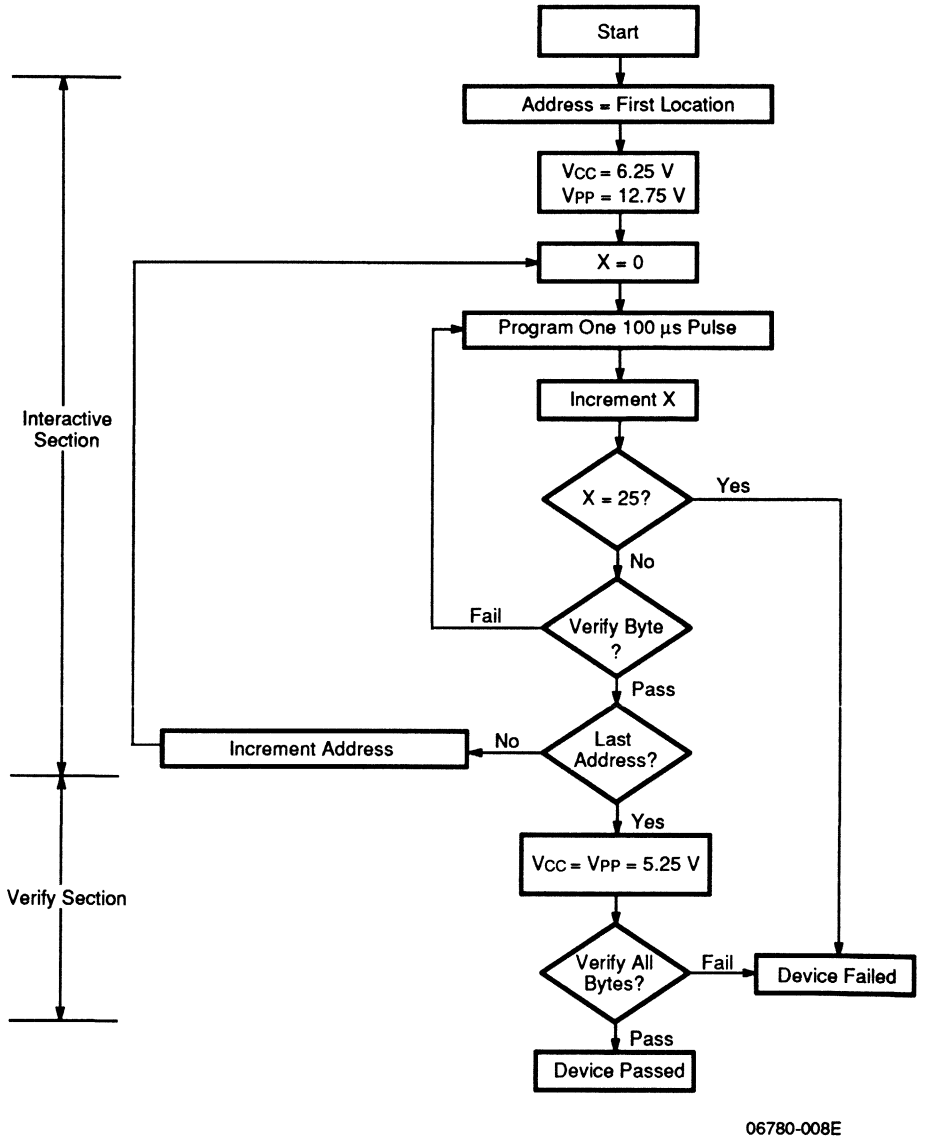


Figure 1. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.3	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC3}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		50	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

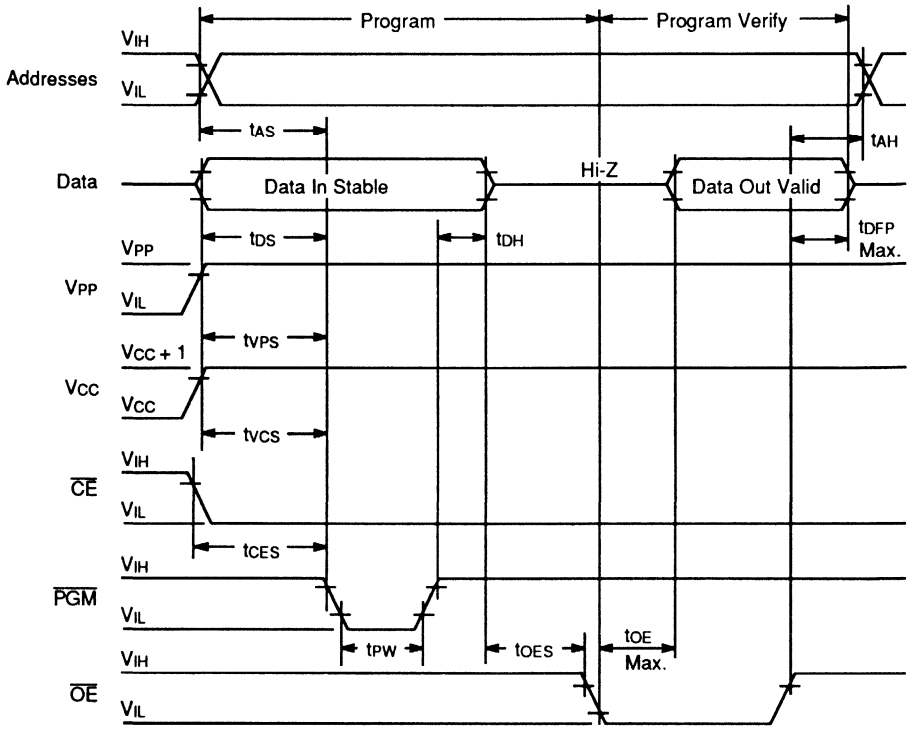
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min.	Max.	Unit
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C1024, a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

PROGRAMMING ALGORITHM WAVEFORM (Notes 1 & 2)



06780-009E

Notes:

1. The input timing reference level is 0.8 for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

Am27C020

2 Megabit (262,144 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - 100 ns
- **Low power consumption:**
  - 20 µA typical CMOS standby current
- **JEDEC-approved pinout**
  - plug in upgrade of 1 Megabit EPROM
  - easy upgrade from 28-pin JEDEC EPROMs
- **Single +5 V power supply**
- **±10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - typical programming time of 30 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Compact 32-pin DIP package requires no hardware change for upgrades to 8 megabits**
- **Versatile features for simple interfacing**
  - both CMOS and TTL input/output compatibility
  - two line control functions

GENERAL DESCRIPTION

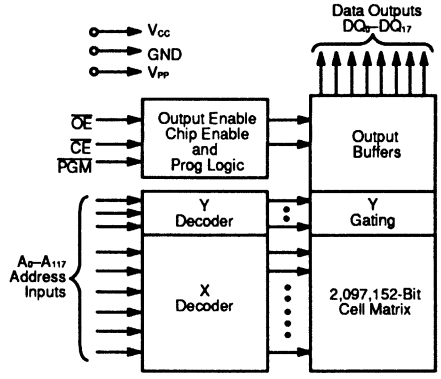
The Am27C020 is a 2 megabit, ultraviolet erasable programmable read-only memory. It is organized as 256K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C020 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C020 supports AMD's Flashrite programming algorithm (100 µs pulses) resulting in typical programming times of 30 seconds.

BLOCK DIAGRAM



11507-001B

PRODUCT SELECTOR GUIDE

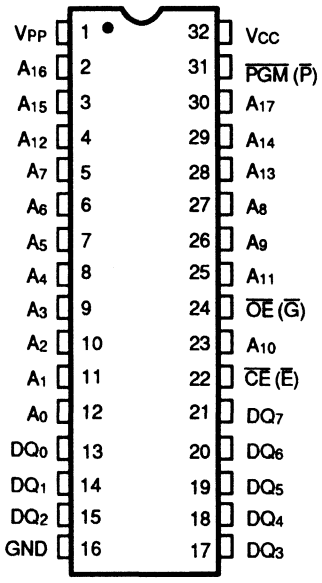
Family Part No.	Am27C020				
Ordering Part No: ±5% Vcc Tolerance	-105	-125			-255
±10% Vcc Tolerance		-120	-150	-200	-250
Max. Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	50	65	75	100

Publication# 11507 Rev. C Amendment/0
Issue Date: March 1991

CONNECTION DIAGRAMS

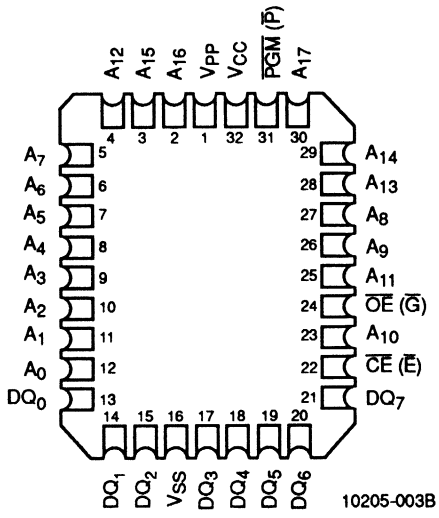
Top View

DIP



11507-003B

LCC*



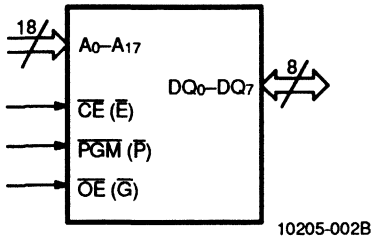
10205-003B

Notes:

1. JEDEC nomenclature is in parenthesis.
2. The 32-pin DIP to 32-pin LCC configuration varies from the JEDEC 28-pin DIP to 32-pin LCC configuration.

*Also available in a 32-pin rectangular Plastic Leaded Chip Carrier.

LOGIC SYMBOL



10205-002B

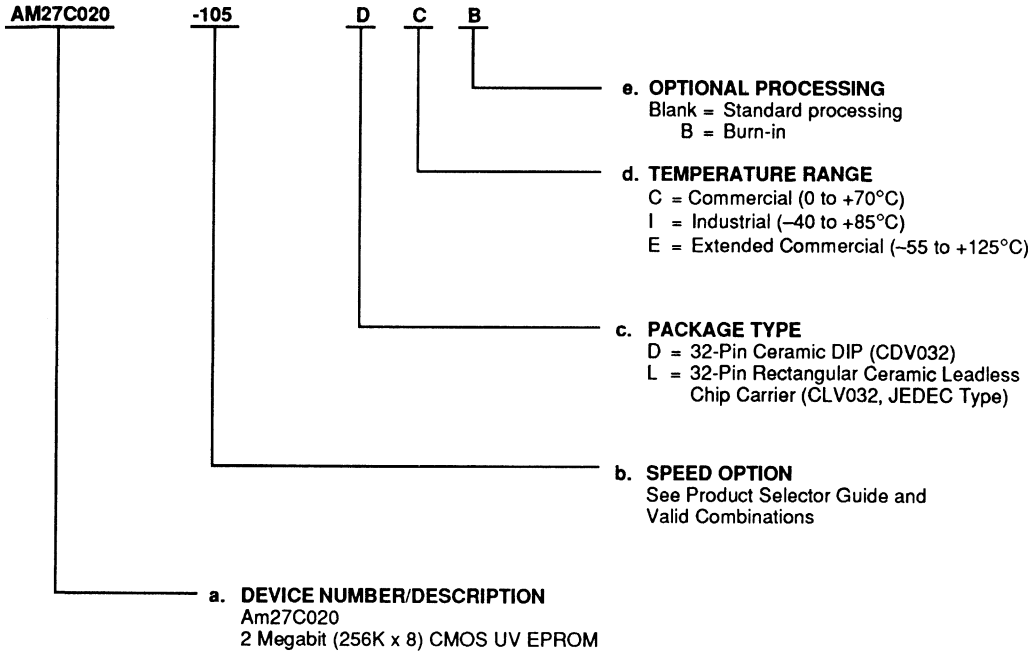
PIN DESCRIPTION

A0–A17	Address Inputs
CE (E)	Chip Enable Input
DQ0–DQ7	Data Input/Outputs
OE (G)	Output Enable Input
PGM (P)	Program Enable Input
VCC	Vcc Supply Voltage
VPP	Program Supply Voltage
GND	Ground

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C020-105	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C020-120	
AM27C020-125	
AM27C020-150	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27C020-200	
AM27C020-255	

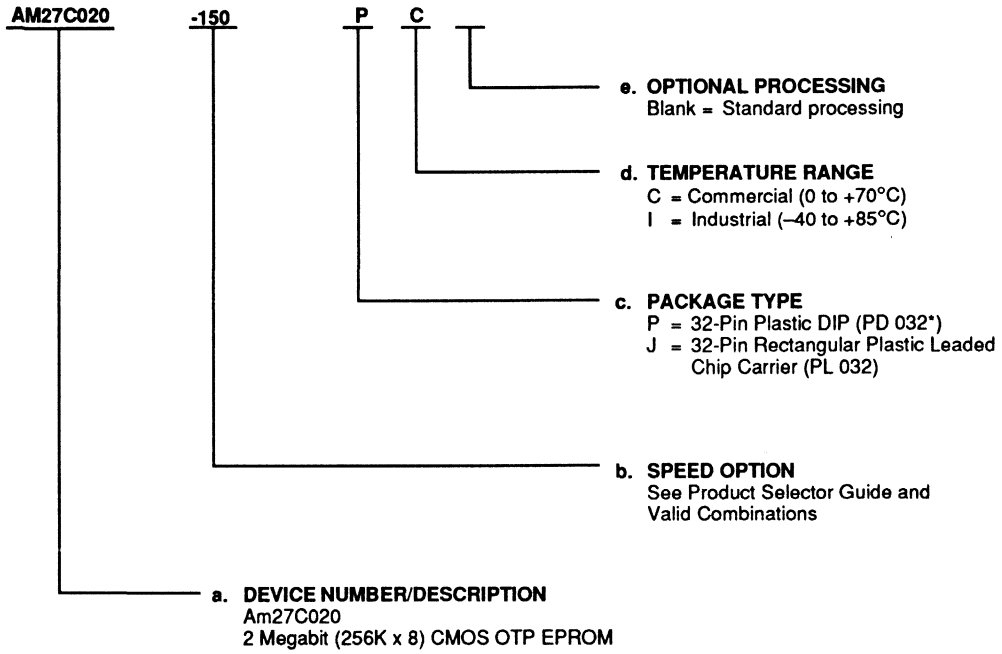
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C020-125	PC, JC, PI, JI
AM27C020-150	
AM27C020-200	
AM27C020-255	

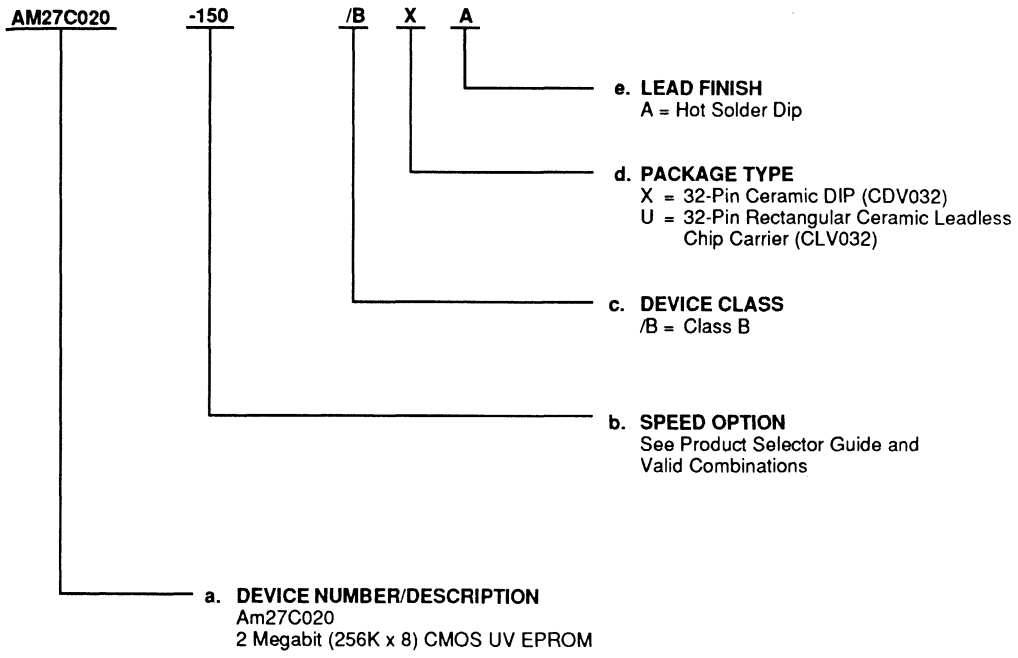
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27C020-150	/BXA, /BUA
AM27C020-200	
AM27C020-250	

For other Surface Mount Package options, contact NVD Military Marketing.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C020

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C020 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C020. This dosage can be obtained by exposure to an ultraviolet lamp —wavelength of 2537 Angstroms (Å) —with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C020 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C020, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C020 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C020

Upon delivery, or after each erasure, the Am27C020 has all 2,097,152 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C020 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ and $\overline{PGM}$ are at V_{IL} and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The flowchart (Figure 2) shows AMD's Flashrite algorithm. The Flashrite algorithm reduces programming time by using 100 µs programming pulse and by giving each address only as many pulses as are necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C020. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at V_{CC} = V_{PP} = 5.25 V.

Program Inhibit

Programming of multiple Am27C020s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C020 may be common. A TTL low-level program pulse applied to an Am27C020 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V, $\overline{PGM}$ LOW, and $\overline{OE}$ HIGH will program that Am27C020. A high-level $\overline{CE}$ input inhibits the other Am27C020s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C020.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C020. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A_0 = V_{IL}) represents the manufacturer code, and Byte 1 (A_0 = V_{IH}), the device identifier code. For the Am27C020, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C020 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C020 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C020 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the outut pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_0	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	X	X	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	X	High Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	97H

Notes:

1. $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$
2. X can be either V_{IL} or V_{IH}
3. $A_1 - A_8 = A_{10} - A_{17} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	–65 to +125°C
All Other Products	–65 to +150°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC} (Note 1)	–0.6 to V_{CC} +0.6 V
A_9 and V_{PP} (Note 2)	–0.6 to 13.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Notes:

1. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0 to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	–40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (T_C)	–55 to +125°C
Military (M) Devices	
Case Temperature (T_C)	–55 to +125°C
Supply Read Voltages:	
V_{CC} for Am27C020-XX5	+4.75 to +5.25 V
V_{CC} for Am27C020-XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 4, 5 & 8)

(for APL products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
TTL and NMOS						
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		5.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Notes 5 & 9)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		30	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH},	C/I Devices		1.0	mA
		$\overline{OE}$ = V_{IL}	E/M Devices		1.0	
I_{PP1}	V_{PP} Supply Current (Read) (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA
CMOS						
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		V_{CC} – 0.8		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			0.7 V_{CC}	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		5.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Notes 5 & 9)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		30	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	C/I Devices		100	µA
			E/M Devices		100	
I_{PP1}	V_{PP} Supply Current (Read) (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

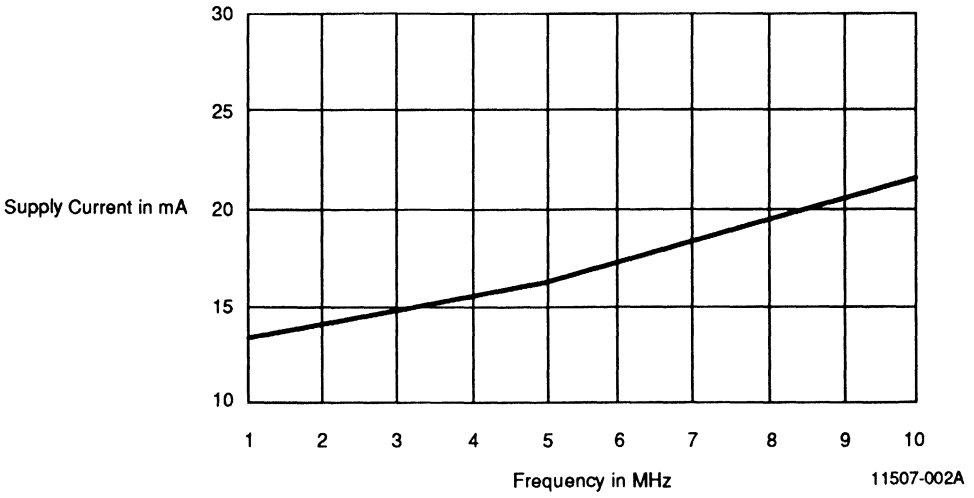


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.0 V, T = 25°C

CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV032		CLV032		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27C020 must not be removed from, or inserted into, a socket or board when V_{CC} or V_{PP} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = +25°C, f = 1 MHz.
8. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns.
   Maximum DC voltage on output pins may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.
9. For typical supply current values at various frequencies, refer to Figure 1.

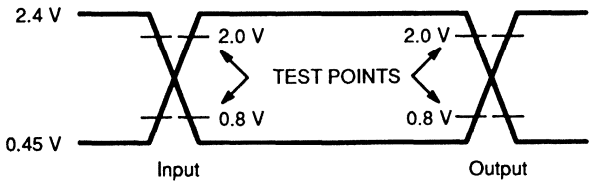
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4) (for APL products, Group A, Subgroups 9, 10, and 11 are tested unless otherwise noted)

PRELIMINARY											
Parameter Symbols		Parameter Description	Test Conditions		Am27C020						
JEDEC	Standard				-105	-120, -125	-150	-200	-250, -255	Unit
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.						ns
				Max.	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.						ns
				Max.	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.						ns
				Max.	50	50	65	75	100	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.	0	0	0	0	0	ns
				Max.	40	40	50	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	ns
				Max.						

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution**: The Am27C020 must not be removed from, or inserted into a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF,
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0.45 to 2.4 V,
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V,
   Outputs: 0.8 V and 2 V.

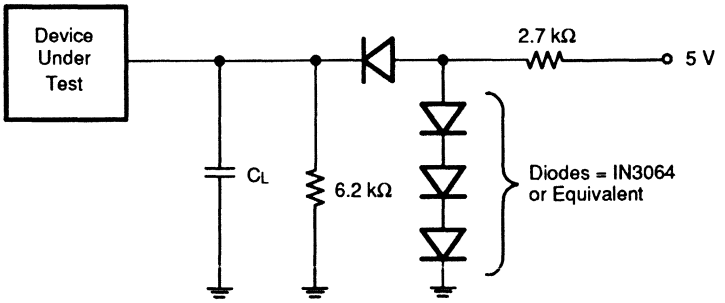
SWITCHING TEST WAVEFORM



10205-009A

AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

SWITCHING TEST CIRCUIT



10205-004A

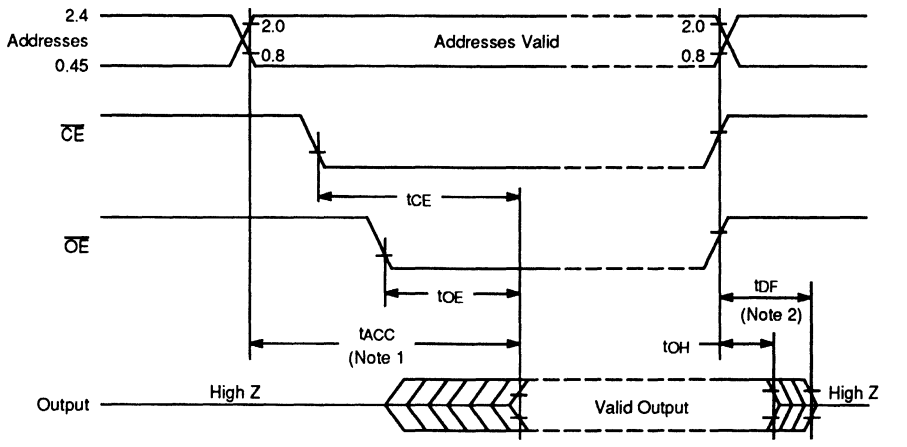
C_L = 100 pF including jig capacitance

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORM



10205-005B

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING FLOW CHART

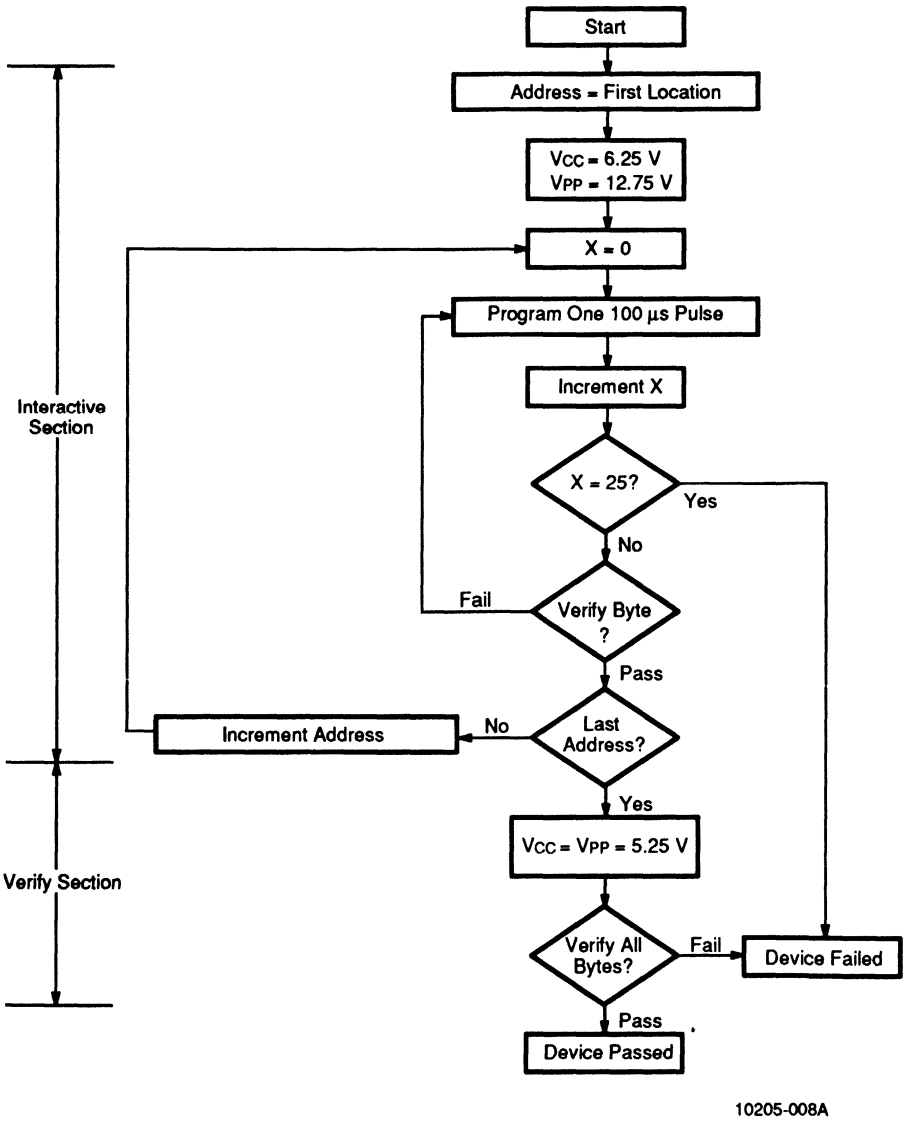


Figure 2. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.5	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

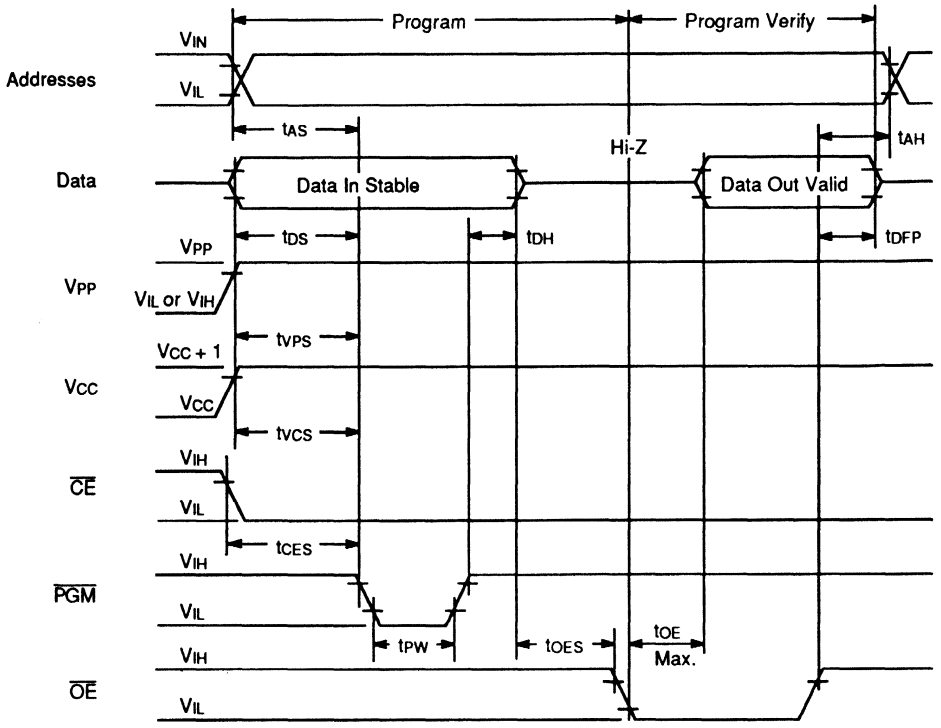
PRELIMINARY

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min.	Max.	Unit
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C020, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

FLASHRITE PROGRAMMING ALGORITHM WAVEFORM (Notes 1 & 2)



10205-006B

Notes:

1. The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

Am27C2048

2 Megabit (131,072 x 16-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - 100 ns
- **Low power consumption**
  - 25 µA typical CMOS standby current
- **JEDEC-approved pinout**
  - plug in upgrade of 1 Megabit EPROM
  - 40-pin DIP/PDIP
  - 44-pin LCC/PLCC
- **Single +5 V power supply**
- **±10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - typical programming time of 15 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - both CMOS and TTL input/output compatibility
  - two line control functions

GENERAL DESCRIPTION

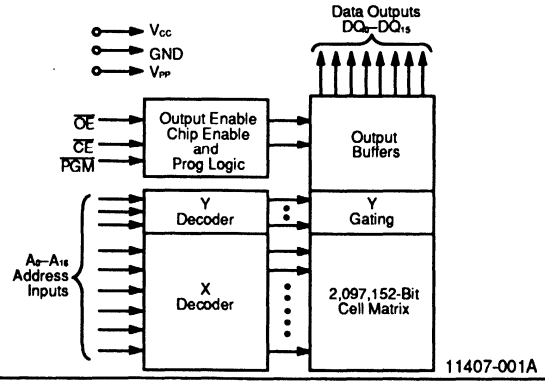
The Am27C2048 is a 2 megabit, ultraviolet erasable programmable read-only memory. It is organized as 128K words by 16 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. The Am27C2048 is ideal for use in 16-bit microprocessor systems. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C2048 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 125 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C2048 supports AMD's Flashrite programming algorithm (100 µs pulses) resulting in typical programming times of 15 seconds.

BLOCK DIAGRAM



11407-001A

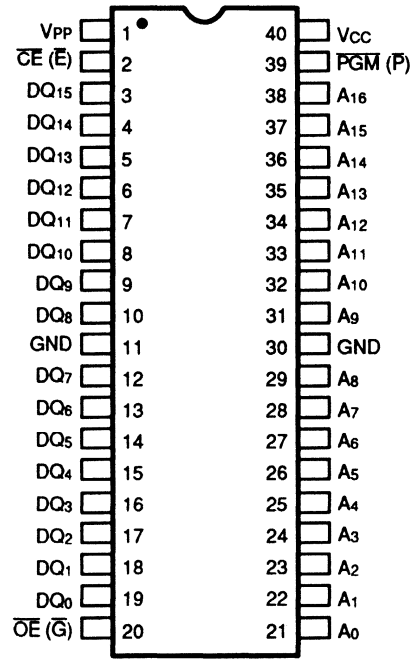
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C2048				
Ordering Part No:					
±5% Vcc Tolerance	-105	-125			-255
±10% Vcc Tolerance		-120	-150	-200	-250
Max. Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	50	65	75	100

Publication# 11407 Rev. C Amendment/0
Issue Date: March 1991

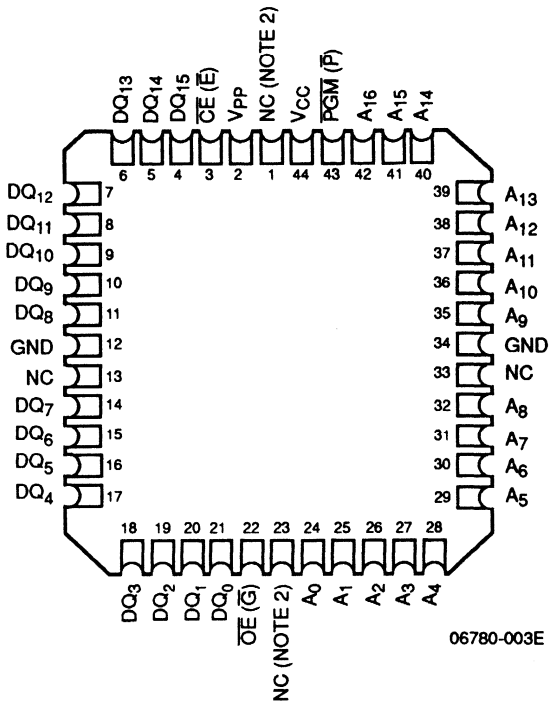
CONNECTION DIAGRAMS
(Top View)

DIPs



11407-002B

LCC*

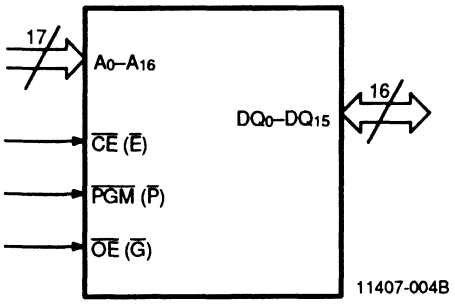


06780-003E

Notes:
1. JEDEC nomenclature is in parenthesis.
2. Don't use (DU) for PLCC.

*Also available in a 44-Pin Plastic Leaded Chip Carrier.

LOGIC SYMBOL



11407-004B

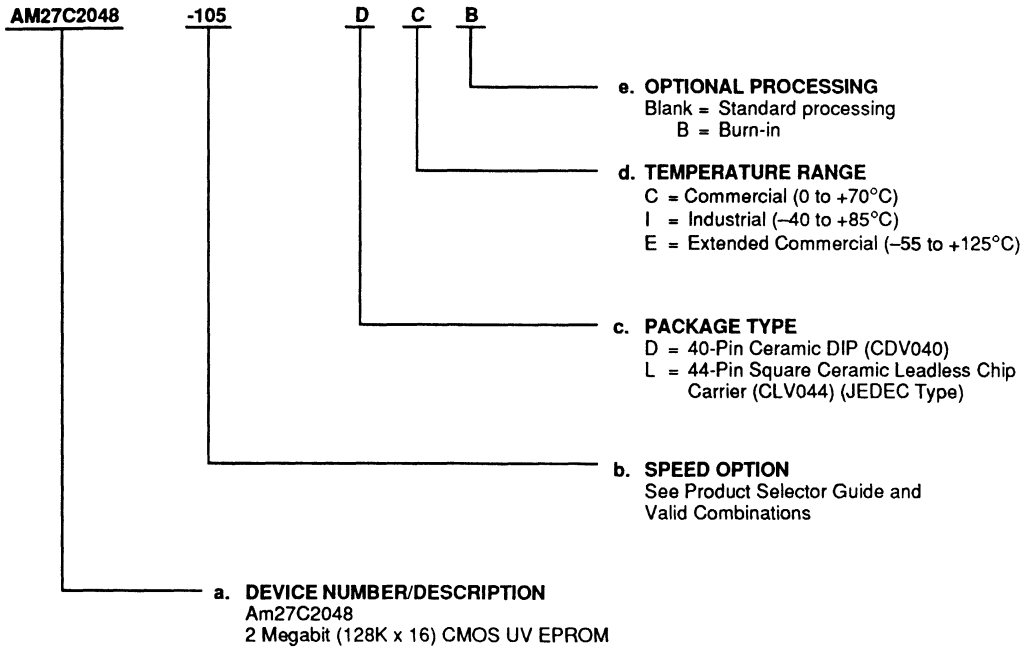
PIN DESCRIPTION

$A_0 - A_{16}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_{15}$	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Program Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connect
DU	=	No External Connect

ORDERING INFORMATION
EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C2048-105	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C2048-120	
AM27C2048-125	
AM27C2048-150	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27C2048-200	
AM27C2048-255	

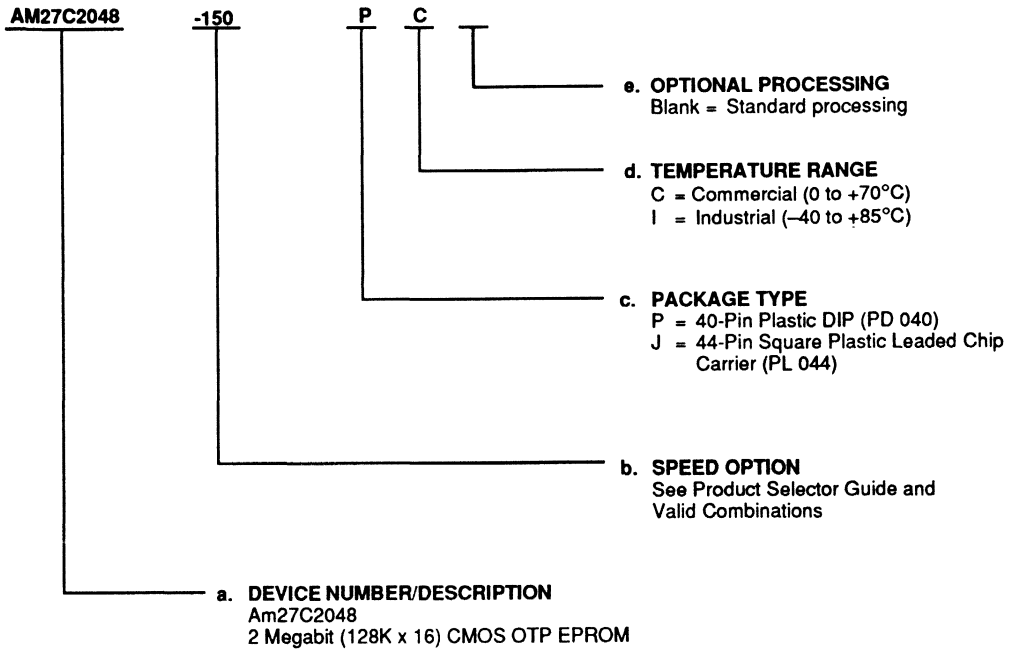
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C2048-125	PC, JC, PI, JI
AM27C2048-150	
AM27C2048-155	
AM27C2048-200	
AM27C2048-255	

Valid Combinations

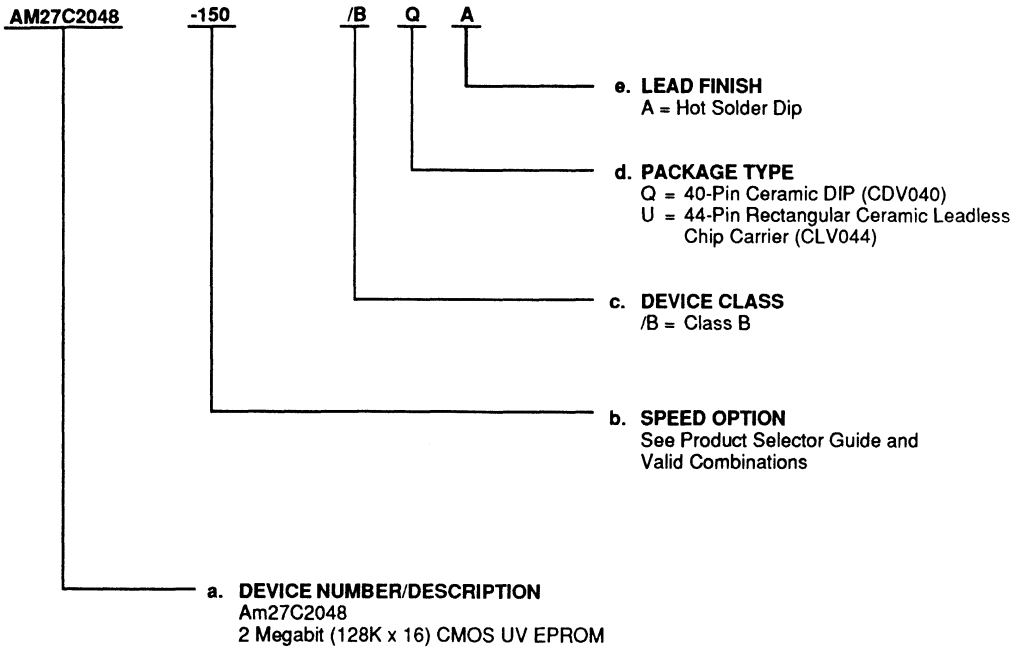
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27C2048-150	/BQA, /BUA
AM27C2048-200	
AM27C2048-250	

For other Surface Mount Package options, contact NVD Military Marketing.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C2048

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C2048 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C2048. This dosage can be obtained by exposure to an ultraviolet lamp —wavelength of 2537 Angstroms (Å) —with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C2048 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C2048, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C2048 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C2048

Upon delivery, or after each erasure, the Am27C2048 has all 2,097,152 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C2048 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, and $\overline{CE}$ and $\overline{PGM}$ are at V_{IL}.

For programming, the data to be programmed is applied 16 bits in parallel to the data pins.

The flowchart (Figure 2) shows AMD's Flashrite algorithm. The Flashrite algorithm reduces programming time by using 100 µs programming pulse and by giving each address only as many pulses as are necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C2048. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP}$ = 5.25 V.

Program Inhibit

Programming of multiple Am27C2048s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C2048 may be common. A TTL low-level program pulse applied to an Am27C2048 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V and $\overline{PGM}$ LOW will program that Am27C2048. A high-level $\overline{CE}$ input inhibits the other Am27C2048 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$, at V_{IL}, PGM at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C2048.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C2048. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and Byte 1 ($A_0 = V_{IH}$), the device identifier code. For the Am27C2048, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C2048 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C2048 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C2048 also has a TTL-standby mode which reduce the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the outut pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_0	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	X	X	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	X	High Z
Program		V_{IL}	X	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	98H

Notes:

1. X can be either V_{IL} or V_{IH}
2. $V_H = 12.0 \text{ V} \pm 0.5 \text{ V}$
3. $A_1 - A_8 = A_{10} - A_{16} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	–65 to +125°C
All Other Products	–65 to +150°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, and V_{CC} (Note 1)	–0.6 to V_{CC} +0.6 V
A_9 and V_{PP} (Note 2)	–0.6 to 13.5 V
V_{CC}	–0.6 to 7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Notes:

1. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0 to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	–40 to +85°C
Extended Commercial (E) Devices	
Case Temperature (T_C)	–55 to +125°C
Military (M) Devices	
Case Temperature (T_C)	–55 to +125°C
Supply Read Voltages:	
V_{CC} for Am27C2048-XX5	+4.75 to +5.25 V
V_{CC} for Am27C2048-XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 4, 5 & 8) (for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted)

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
TTL and NMOS						
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		5.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Notes 5 & 9)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		50	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH},	C/I Devices		1.0	mA
			E/M Devices		1.0	
I_{PP1}	V_{PP} Supply Current (Read) (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA
CMOS						
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		V_{CC} – 0.8		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			0.7 V_{CC}	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		5.0	µA
			E/M Devices		5.0	
I_{CC1}	V_{CC} Active Current (Notes 5 & 9)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		50	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	C/I Devices		100	µA
			E/M Devices		150	
I_{PP1}	V_{PP} Supply Current (Read) (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

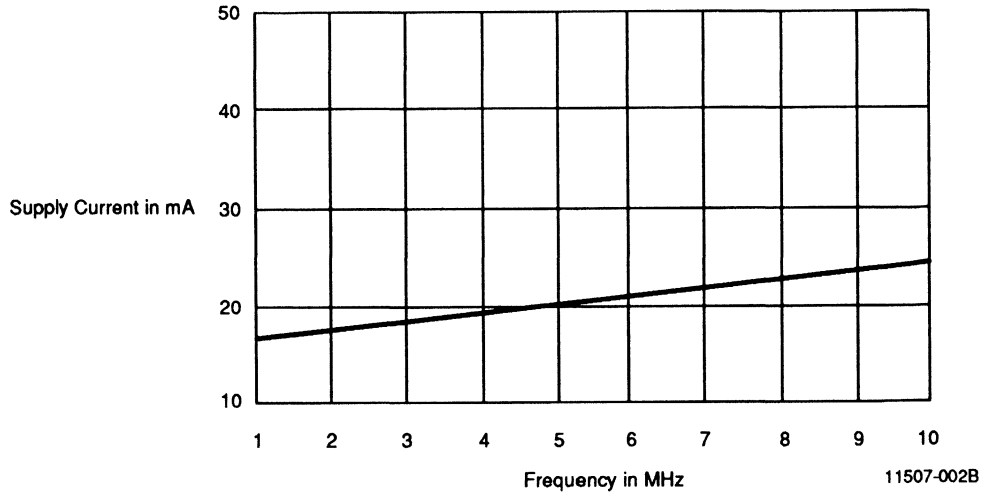


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.0 V, T = 25°C

CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV044		CLV044		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution**: The Am27C2048 must not be removed from, or inserted into, a socket or board when V_{CC} or V_{PP} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. Minimum DC input voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.
9. For typical supply current values at various frequencies, refer to Figure 1.

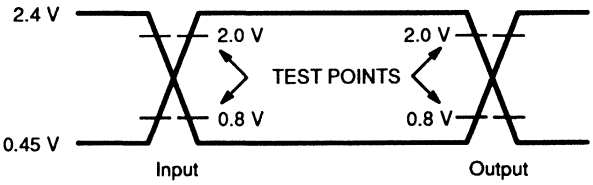
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

PRELIMINARY										
Parameter Symbols		Parameter Description	Test Conditions		Am27C2048					
JEDEC	Standard				-105	-120, -125	-150	-200	-250, -255	Unit
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.						ns
				Max.	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.						ns
				Max.	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.						ns
				Max.	50	50	65	75	100	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.	0	0	0	0	0	ns
				Max.	40	40	50	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	ns
				Max.						

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27C2048 must not be removed from, or inserted into, a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF,
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0.45 to 2.4 V,
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V,
   Outputs: 0.8 V and 2 V.

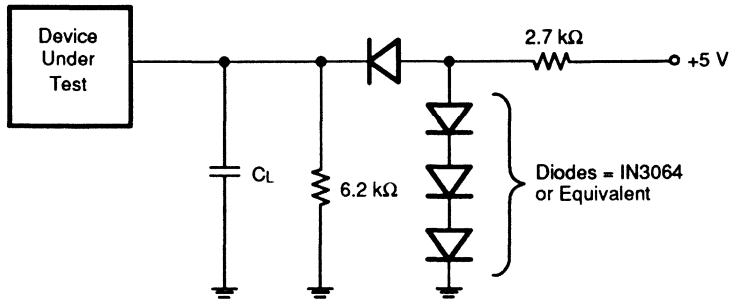
SWITCHING TEST WAVEFORM



10205-009A

AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20 ns.

SWITCHING TEST CIRCUIT



10205-004A

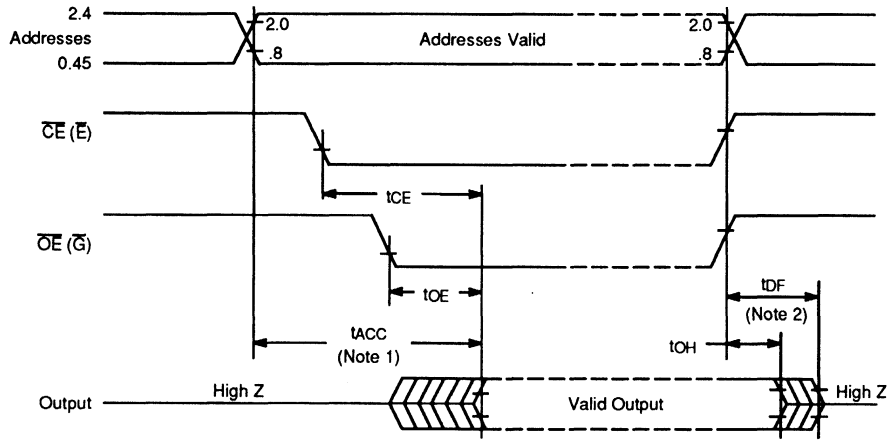
C_L = 100 pF including jig capacitance

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORM



10205-005A

Notes:

1. $\overline{OE}$ ($\overline{G}$) may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING FLOW CHART

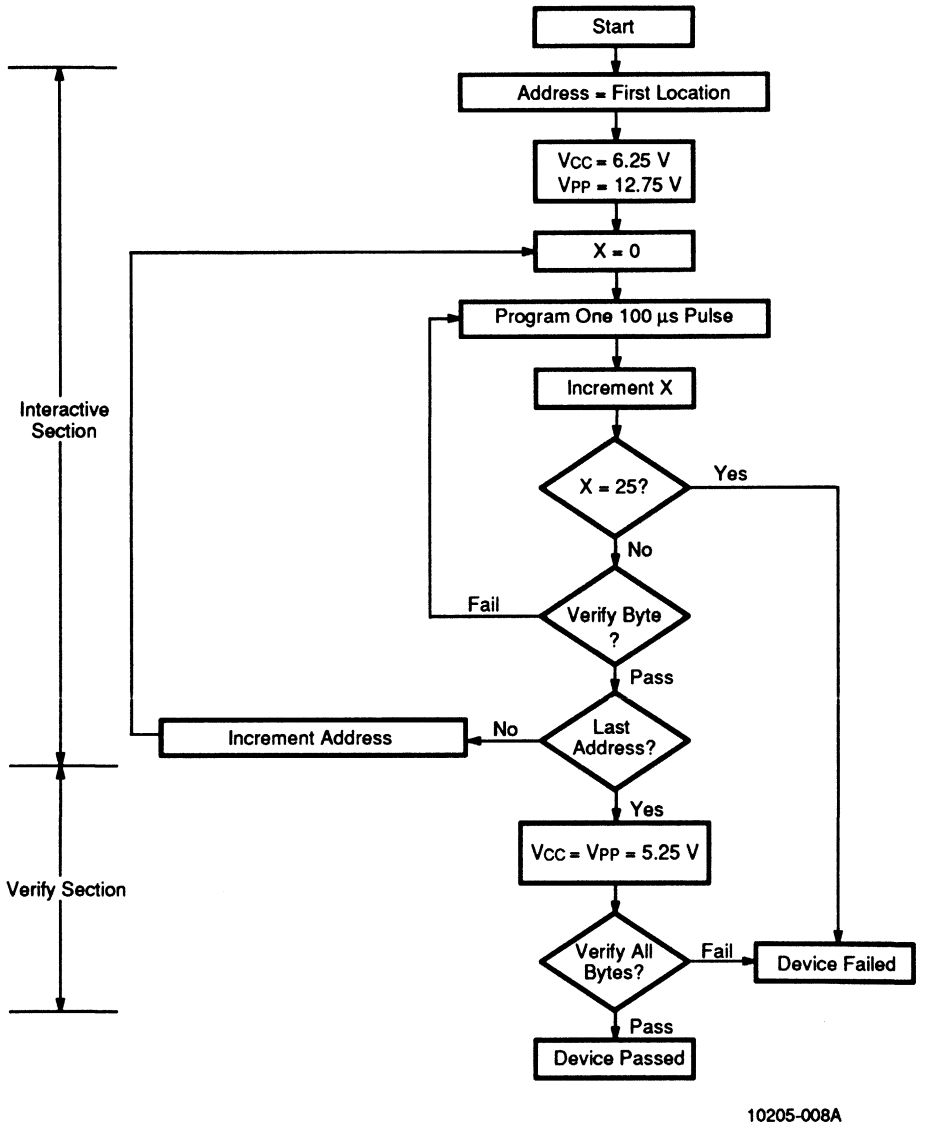


Figure 2. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

PRELIMINARY					
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min.**	**Max.**	**Unit**
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.5	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		50	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

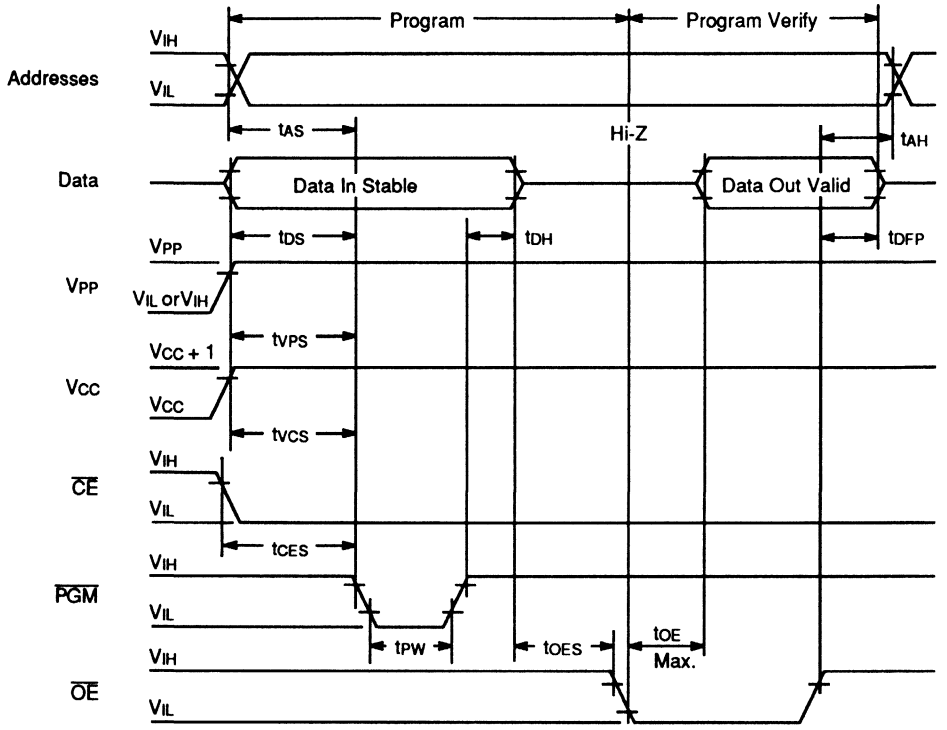
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

PRELIMINARY					
Parameter Symbols					
JEDEC	**Standard**	**Parameter Description**	**Min.**	**Max.**	**Unit**
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C2048, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

FLASHRITE PROGRAMMING ALGORITHM WAVEFORM (Notes 1 & 2)



10205-006B

Notes:

1. The input timing reference level is 0.8 for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

Am27C040

4 Megabit (524,288 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - 90 ns
- **Low power consumption**
  - 20 µA typical CMOS standby current
- **JEDEC-approved pinout**
  - plug in upgrade of 1 Megabit and 2 Megabit EPROMs
  - easy upgrade from 28-pin JEDEC EPROMs
- **Single + 5 V power supply**
- **± 10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - typical programming time of less than 3 minutes
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**
- **High noise immunity**
- **Compact 32-pin DIP, PDIP, LCC and PLCC packages require no hardware change for upgrades to 8 megabits**
- **Versatile features for simple interfacing**
  - both CMOS and TTL input/output compatibility
  - two line control functions

GENERAL DESCRIPTION

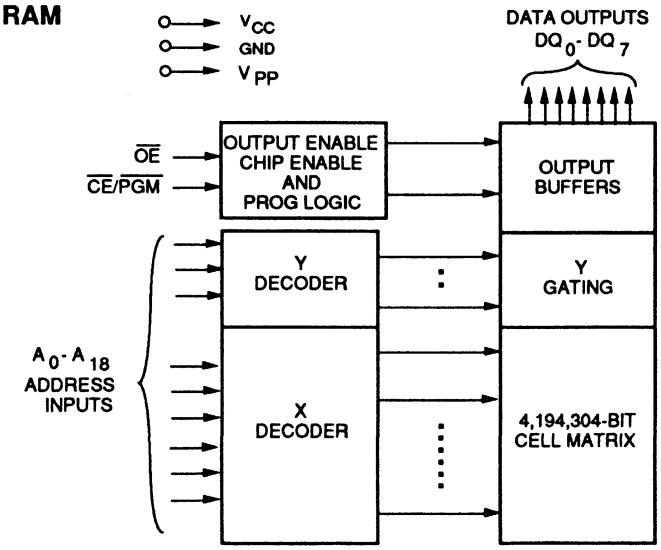
The Am27C040 is a 4 megabit ultraviolet erasable programmable read-only memory. It is organized as 512K words by 8 bits per word, operates from a single + 5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 90 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C040 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C040 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming times of less than 3 minutes.

BLOCK DIAGRAM



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Issue Date: March 1991

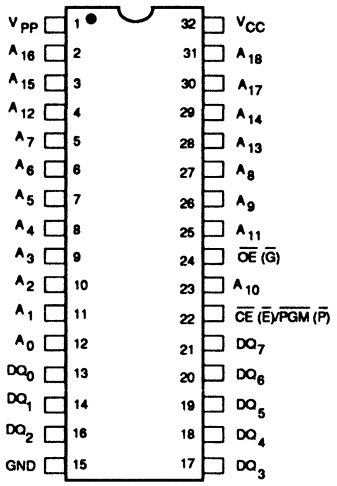
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C040				
Ordering Part Number					
V_{CC} ± 5%	-95	-125	-155		-255
V_{CC} ± 10%	-90	-120	-150	-200	-250
Max. Access Time (ns)	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	40	50	65	75	100

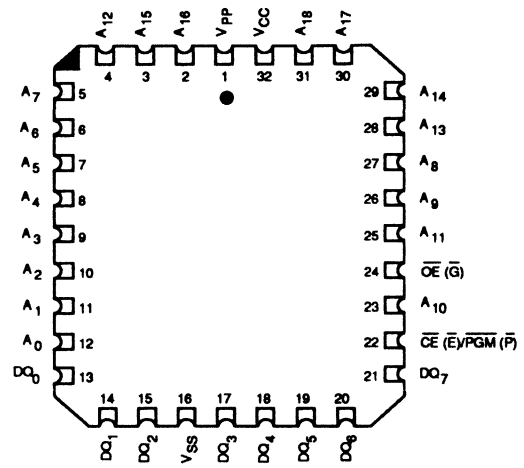
CONNECTION DIAGRAMS

Top View

DIP



LCC*



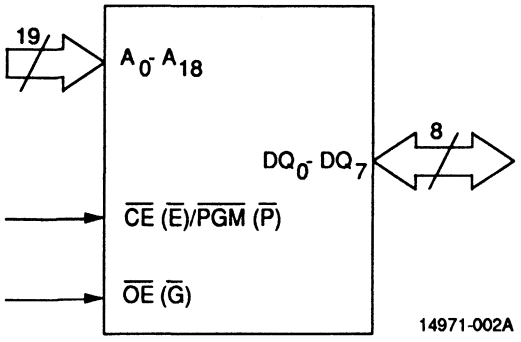
14971-003A

Notes:

1. JEDEC nomenclature is in parentheses.
2. The 32-Pin DIP to 32-Pin LCC configuration varies from the JEDEC 28-Pin DIP to 32-Pin LCC configuration.

* Also available in 32-pin rectangular plastic leaded chip carrier.

LOGIC SYMBOL



14971-002A

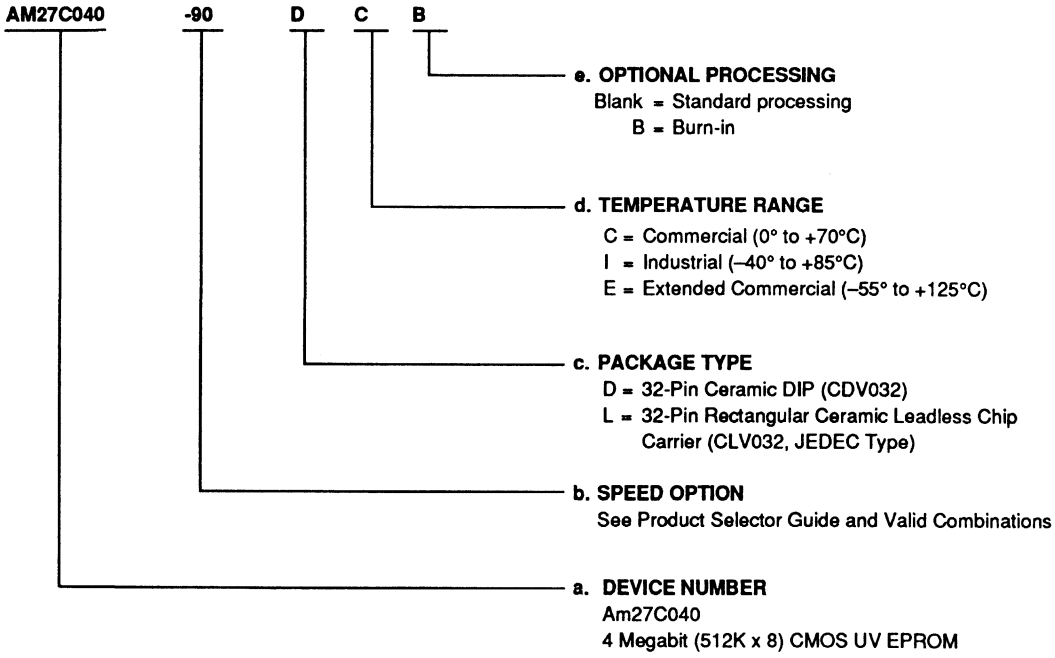
PIN DESCRIPTION

A_0– A_{18}	= Address Inputs
$\overline{CE}$ ($\overline{E}$)/$\overline{PGM}$ ($\overline{P}$)	= Chip and Program Enable Input
DQ_0– DQ_7	= Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	= Output Enable Input
V_{CC}	= V_{CC} Supply Voltage
V_{PP}	= Program Supply Voltage
GND	= Ground

ORDERING INFORMATION
EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM27C040-90	DC, DCB, LC, LCB
AM27C040-95	
AM27C040-120	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C040-125	
AM27C040-150	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27C040-200	
AM27C040-255	

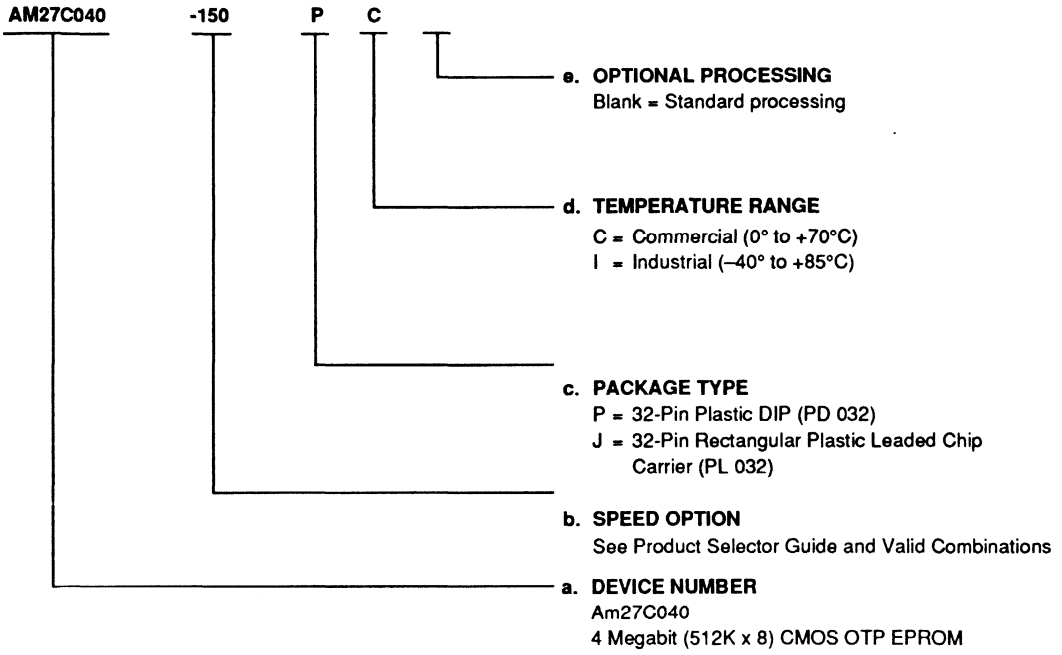
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly-released combinations.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C040-150	PC, JC, PI, JI
AM27C040-155	
AM27C040-200	
AM27C040-250	

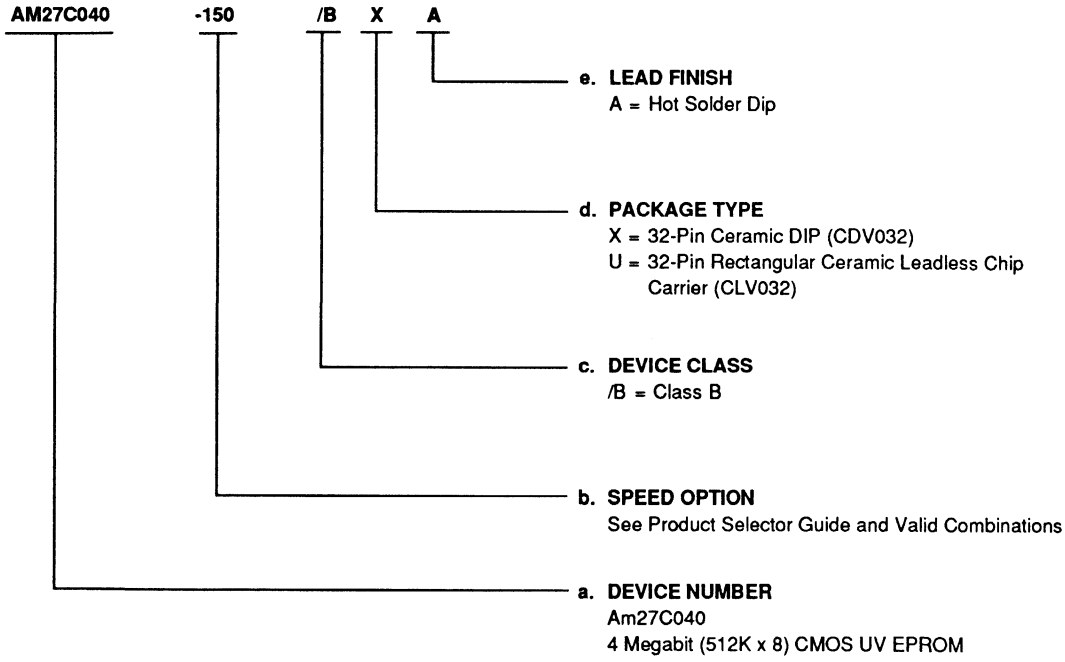
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly-released combinations.

ORDERING INFORMATION
Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27C040-150	/BXA, /BUA
AM27C040-200	
AM27C040-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly-released combinations.

Group A Tests

Group A tests consist of Subgroups 1,2,3,7,8,9,10,11.

For other Surface Mount Package options, contact NVD Military Marketing.

FUNCTIONAL DESCRIPTION

Erasing the Am27C040

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C040 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C040. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C040 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C040 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C040 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C040

Upon delivery or after each erasure the Am27C040 has all 4,194,304 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C040 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ is at V_{IL}, and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The flowchart (Figure 2) shows AMD's Flashrite algorithm. The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C040. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP}$ = 5.25 V.

Program Inhibit

Programming of multiple Am27C040 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C040 may be common. A TTL low-level program pulse applied to an Am27C040 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V, and $\overline{OE}$ HIGH will program that Am27C040. A high-level $\overline{CE}$ input inhibits the other Am27C040 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C040.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C040. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and byte 1($A_0 = V_{IH}$), the device identifier code. For the Am27C040, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C040 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C040 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C040 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A_0	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	Hi-Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	X	9BH

Notes:

1. $V_H = 12.0 \pm 0.5$ V
2. X = Either V_{IH} or V_{IL}
3. $A_1 - A_8 = A_{10} - A_{16} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature

OTP products	–65° to +125°C
All other products	–65° to +150°C
Ambient Temperature with Power Applied	–55° to +125°C

Voltage with Respect to Ground:

All pins except A_9, V_{PP}, V_{CC} (Note 1)	–0.6 to V_{CC} + 0.6 V
A_9 and V_{PP} (Note 2)	–0.6 to +13.5 V
V_{CC}	–0.6 to +7.0 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. During transitions, the inputs may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0° to +70°C

Industrial (I) Devices

Case Temperature (T_C)	–40° to +85°C

Extended Commercial (E) Devices

Case Temperature (T_C)	–55° to +125°C

Military (M) Devices

Case Temperature (T_C)	–55° to +125°C

Supply Read Voltages:

V_{CC} for Am27C040-XX5	+4.75 to +5.25 V
V_{CC} for Am27C040-XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 4, 5, and 8)

(for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted)

TTL and NMOS

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		5.0	µA
			E/M Devices		10.0	
I_{CC1}	V_{CC} Active Current (Notes 5, 9)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		40	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}	C/I Devices		1.0	mA
			E/M Devices		1.0	
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

CMOS

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		V_{CC} – 0.8 V		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			0.7 V_{CC}	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		5.0	µA
			E/M Devices		10.0	
I_{CC1}	V_{CC} Active Current (Notes 5, 9)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		40	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	C/I Devices		100	µA
			E/M Devices		100	
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

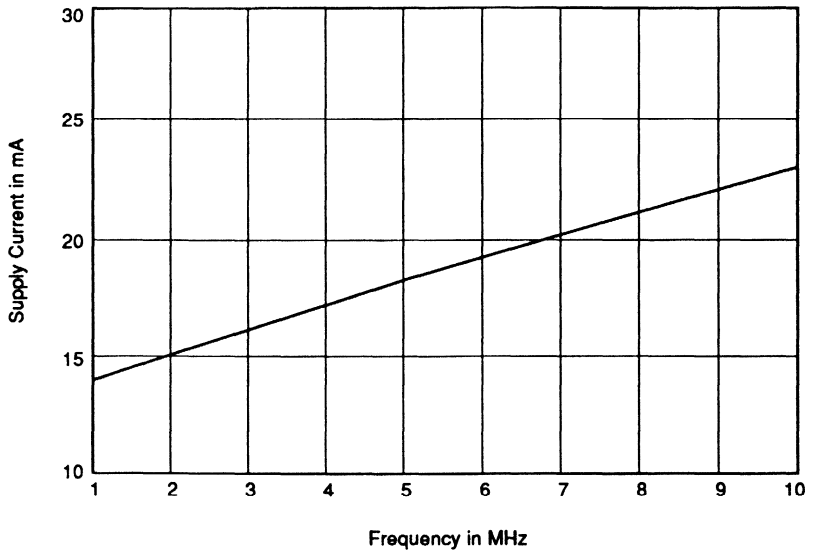


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Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.0 V, T = 25°C

CAPACITANCE (Notes 2, 3, and 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV032		CLV032		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled, not 100% tested.
4. **Caution:** the Am27C040 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
5. I_{CC1} is tested with OE = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = +25°C, f = 1 MHz.
8. Minimum DC Input Voltage is -0.5 V. During transitions, the inputs overshoot to -2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} +2.0 V for periods less than 20 ns.
9. For typical supply current values at various frequencies, refer to Figure 1.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 3, and 4)

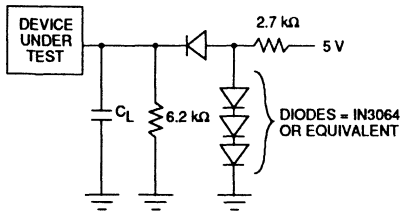
(for APL Products, Group A, Subgroups 9, 10, and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C040					Unit
JEDEC	Standard				-90, -95	-120, -125	-150, -155	-200	-255, -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE}_L = V_I$	Min.	–	–	–	–	–	ns
				Max.	90	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.	–	–	–	–	–	ns
				Max.	90	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.	–	–	–	–	–	ns
				Max.	40	50	65	75	100	
t_{EHQZ} / t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.	–	0	0	0	0	ns
				Max.	30	40	50	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	ns
				Max.	–	–	–	–	–	

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled, not 100% tested.
3. **Caution:** The Am27C040 must not be removed from (or inserted into) a socket or board when V_{pp} or V_{cc} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level — Inputs: 0.8 to 2.0 V
   Outputs: 0.8 to 2.0 V

SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance.

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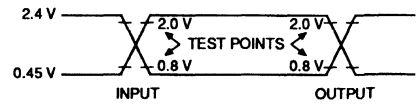
SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Input pulse rise and fall times are ≤ 20 ns.

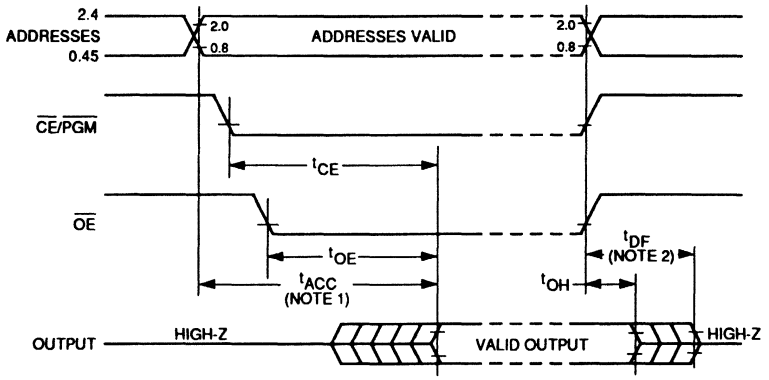
10205B-009A

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



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Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

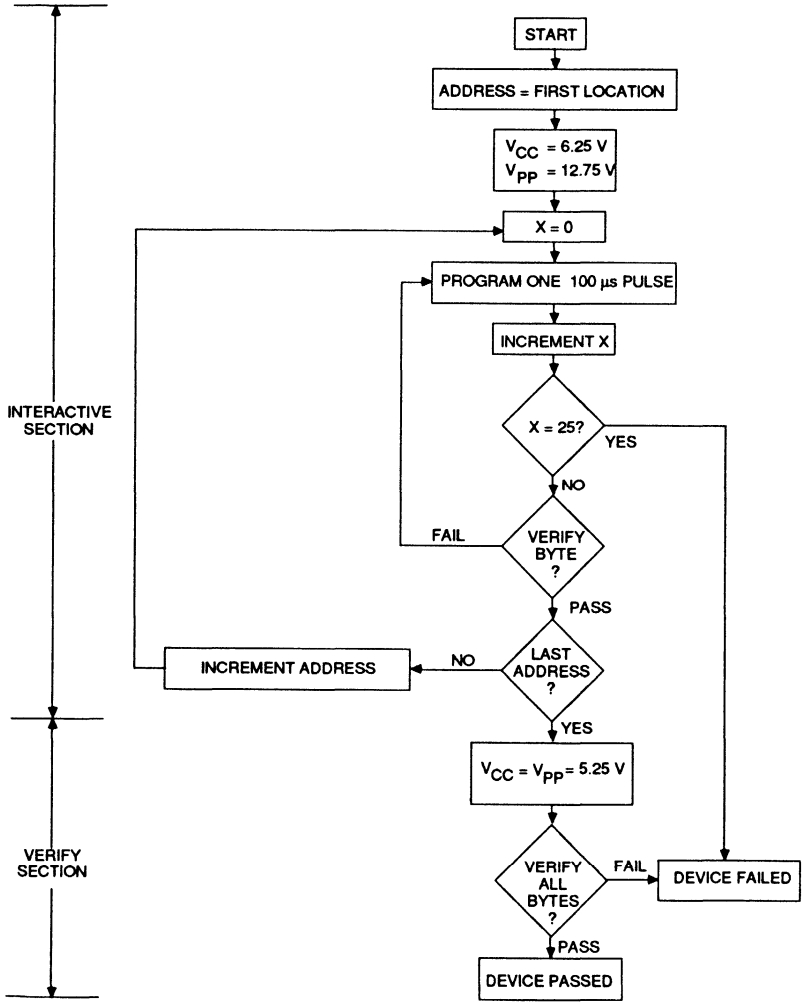

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Figure 2. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ± 5°C) (Notes 1, 2, and 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input LOW Level (All Inputs)		-0.5	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = -400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

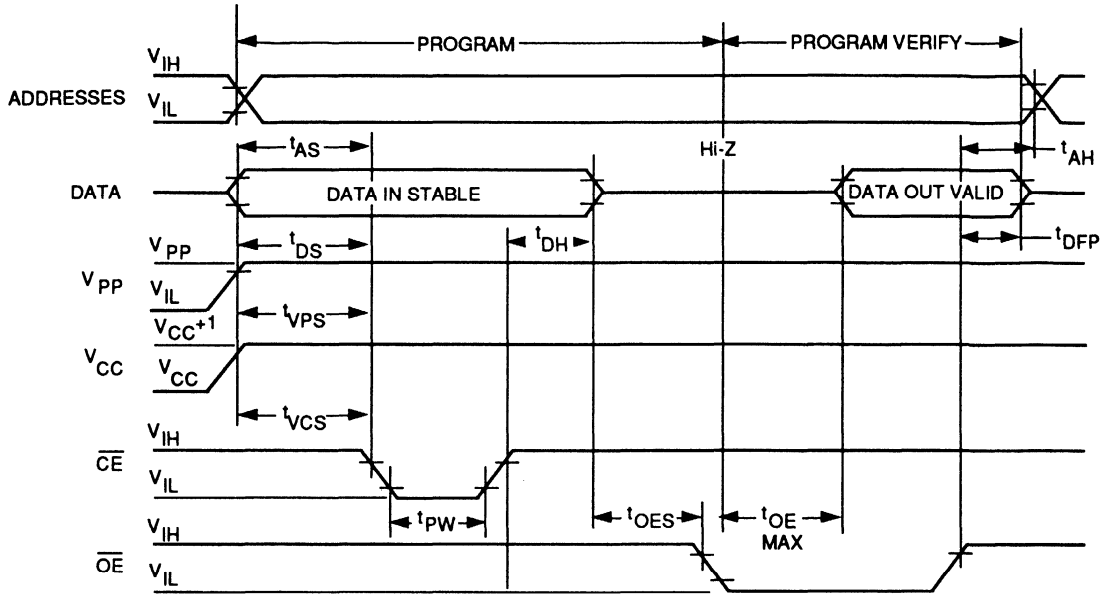
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ± 5°C) (Notes 1, 2, and 3)

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{QZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C040, a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients that may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

FLASHRITE PROGRAMMING ALGORITHM WAVEFORM (Notes 1 and 2)



Notes:

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1. The input timing reference level is 0.8 V for a V_{IL} and 2 V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Preliminary

Am27C400

4 Megabit (524,288 x 8-Bit/262,144 x 16-Bit) ROM Compatible CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - 90 ns
- **Low power consumption**
  - 20 µA typical CMOS standby current
- **Industry standard pinout:**
  - ROM compatible
  - 40-pin DIP, and PDIP packages provide easy upgrade to 8 megabits
- **Single +5 V power supply**
- **±10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - typical programming time of less than 3 minutes
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - both CMOS and TTL input/output compatibility
  - two line control functions

GENERAL DESCRIPTION

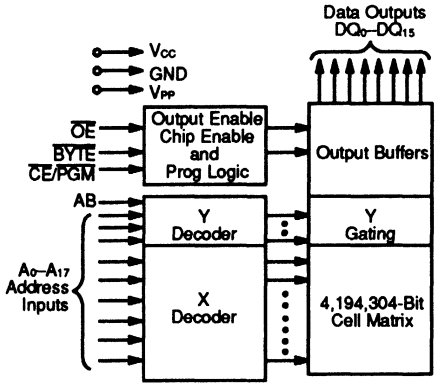
The Am27C400 is a 4 megabit ultraviolet erasable programmable read-only memory that is functionally and pinout compatible with 4 megabit masked ROMs. Under control of the $\overline{BYTE}$ input, the memory can be configured as either a 512K by 8-bit memory or a 256K by 16-bit memory. It operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP packages as well as plastic one time programmable (OTP) PDIP packages.

Typically, any byte can be accessed in less than 90 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C400 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C400 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming times of less than 3 minutes.

BLOCK DIAGRAM



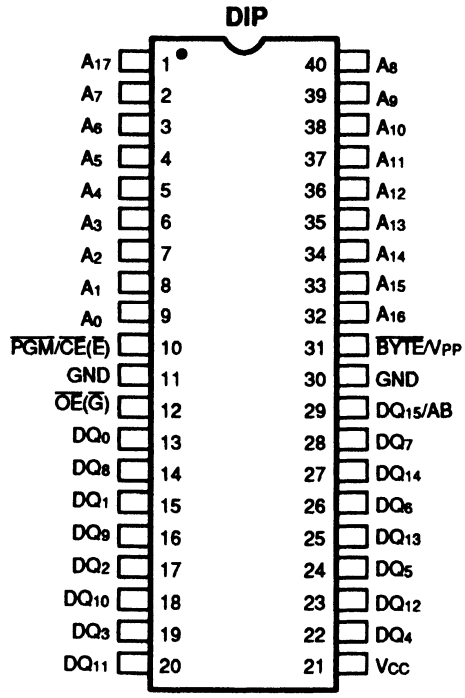
15573A-001A

Publication# 15573 Rev. A Amendment/0
Issue Date: March 1991

PRODUCT SELECTOR GUIDE

Family Part No.	Am27C400				
Ordering Part No: Vcc ± 5%	-95	-125	-155		-255
Vcc ± 10%	-90	-120	-150	-200	
Max. Access Time (ns)	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	40	50	65	75	100

CONNECTION DIAGRAM
Top View



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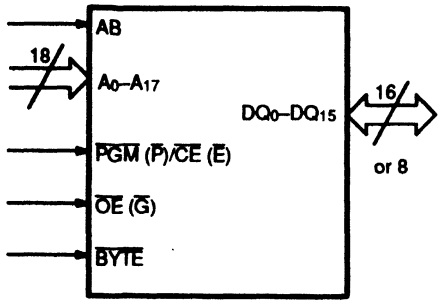
Notes:

1. JEDEC nomenclature is in parenthesis.
2. PLCC connection diagram to be determined

LOGIC SYMBOL



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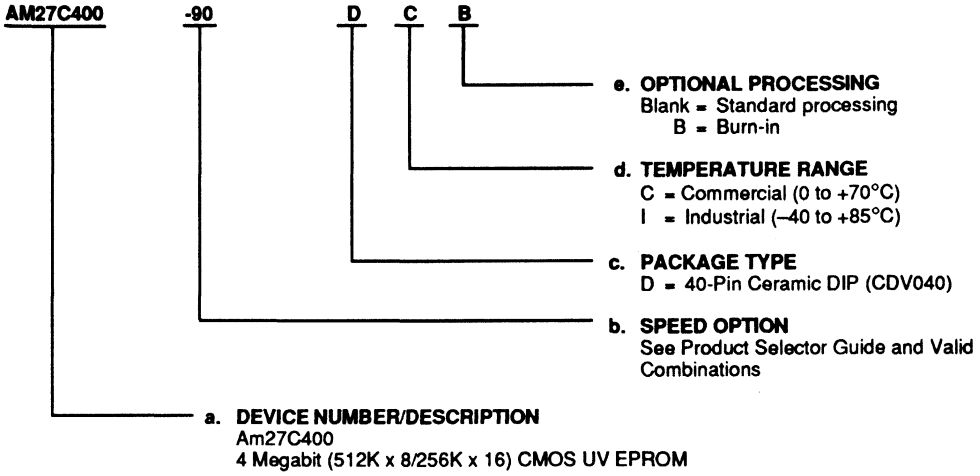
PIN DESCRIPTIONS

AB	=	Address Input ($\overline{BYTE}$ Mode)
A_0–A_{17}	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)/$\overline{PGM}$ ($\overline{P}$)	=	Chip Enable and Program Enable Inputs
DQ_0–DQ_{15}	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
Vcc	=	Vcc Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
$\overline{BYTE}$	=	Byte/Word Switch

ORDERING INFORMATION
EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C400-90	DC, DCB, DI, DIB
AM27C400-95	
AM27C400-120	
AM27C400-125	
AM27C400-150	
AM27C400-200	
AM27C400-255	

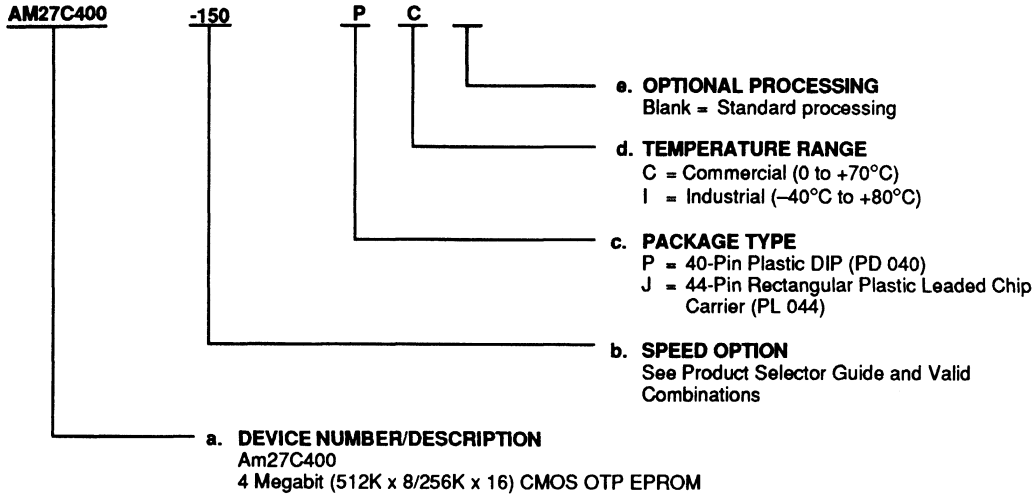
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C400-150	PC, JC, PI, JI
AM27C400-155	
AM27C400-200	
AM27C400-255	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Erasing the Am27C400

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C400 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C400. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2,537 Angstroms (Å) — with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C400 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C400 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2,537Å, exposure to fluorescent light and sunlight will eventually erase the Am27C400 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C400

Upon delivery or after each erasure the Am27C400 has all 4,194,304 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C400 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ is at V_{IL}, and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 16 bits in parallel to the data output pins.

The flowchart (Figure 2) shows AMD's Flashrite algorithm. The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each addresss only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C400. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Program Inhibit

Programming of multiple Am27C400s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C400 may be common. A TTL low-level program pulse applied to an Am27C400 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V, and $\overline{OE}$ HIGH will program that Am27C400. A high-level $\overline{CE}$ input inhibits the other Am27C400 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C400.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C400. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and Byte 1 ($A_0 = V_{IH}$), the device identifier code. For the Am27C400, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C400 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Byte Mode

The user has the option of reading data in either 16-bit words or 8-bit bytes under control of the $\overline{BYTE}$ input. With the $\overline{BYTE}$ input HIGH, inputs $A_0 - A_{17}$ will address 256K words of 16-bit data. When the $\overline{BYTE}$ input is LOW, AB functions as the least significant address input and 512K bytes of data can be accessed. The 8 bits of data will appear on $DQ_0 - DQ_7$.

Standby Mode

The Am27C400 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in

CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C400 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins		$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A_0	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	Hi-Z
Standby (CMOS)		V_{CC} ± 0.3 V	X	X	X	X	Hi-Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	X	9DH

Notes:

1. V_H = 12.0 V ± 0.5 V
2. X = Either V_{IH} or V_{IL}
3. $A_1 - A_8 = A_{10} - A_{15} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	–65 to +125°C
All Other Products	–65 to +150°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, V_{CC} (Note 1)	–0.6 to V_{CC} +0.6 V
A_9 and V_{PP} (Note 2)	–0.6 to +13.5 V
V_{CC}	–0.6 to +7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. During transitions, the inputs may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

2. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0 to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	–40° to +85°C
Supply Read Voltages:	
V_{CC} for Am27C400-XX5	+4.75 to +5.25 V
V_{CC} for Am27C400-XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 4, 5, & 8)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
TTL and NMOS Inputs					
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}		5.0	µA
I_{CC1}	V_{CC} Active Current (Notes 5, 9)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)		40	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}		1.0	mA
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}		100	µA
CMOS Inputs					
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA	V_{CC} – 0.8 V		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA		0.45	V
V_{IH}	Input HIGH Voltage		0.7 V_{CC}	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}		5.0	µA
I_{CC1}	V_{CC} Active Current (Notes 5, 9)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)		40	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V		100	µA
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}		100	µA

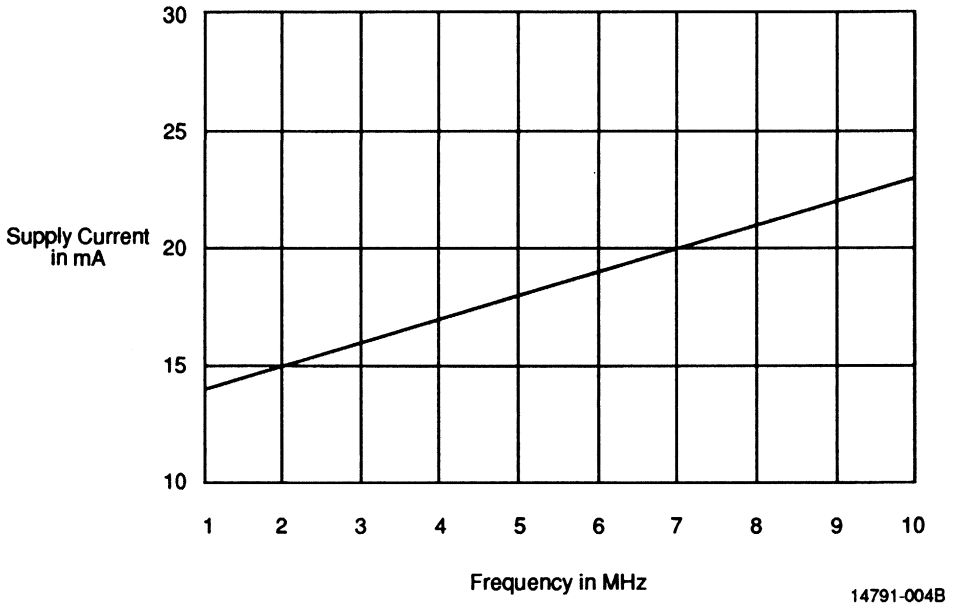


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.0 V, T = 25°C

CAPACITANCE (Notes 2, 3, & 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV040		CLV044		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN}	Input Capacitance	V_{IN} = 0 V	7	12	5	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	10	15	8	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled, not 100% tested.
4. **Caution**: The Am27C400 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = +25°C, f = 1 MHz.
8. Minimum DC input voltage is –0.5 V. During transitions, the inputs overshoot to –2.0 V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.
9. For typical supply current values at various frequencies, refer to Figure 1.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3, & 4)

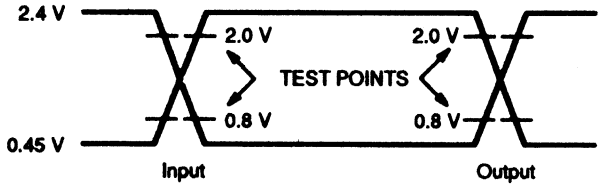
(for APL Products, Group A, Subgroups 9, 10, and 11 are tested unless otherwise noted)

JEDEC	Standard	Parameter Description	Test Conditions		Am27C400 -90, -95	-120, -125	-150, -155	-200	-255	Unit
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.	–	–	–	–	–	ns
				Max.	90	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.	–	–	–	–	–	ns
				Max.	90	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.	–	–	–	–	–	ns
				Max.	40	50	65	75	100	
t_{EHQZ}, t_{GHQZ}	t_{DF} Note 2	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.	–	0	0	0	0	ns
				Max.	30	40	50	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	ns
				Max.	–	–	–	–	–	

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled, not 100% tested.
3. **Caution:** The Am27C400 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level — Inputs: 0.8 and 2.0 V
   Outputs: 0.8 and 2.0 V.

SWITCHING TEST WAVEFORM



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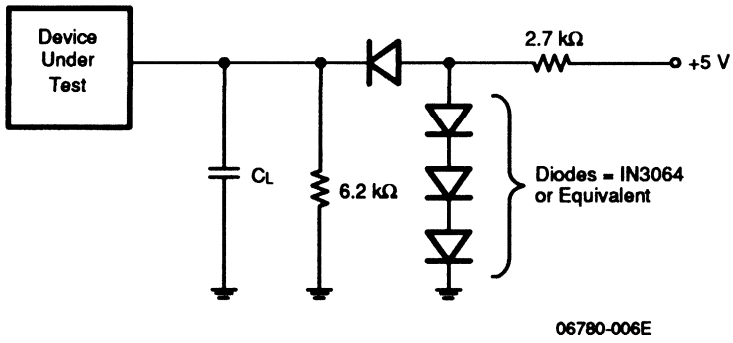
AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 for a logic "0". Input pulse rise and fall times are ≤ 20 ns.



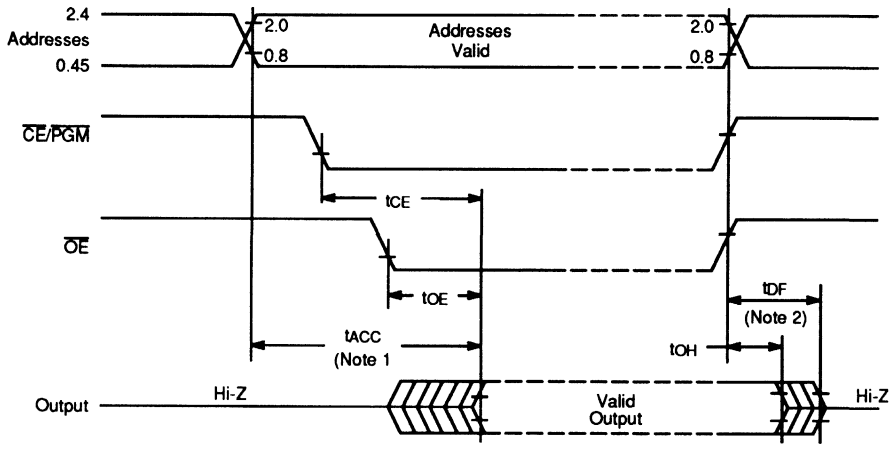
C_L = 100 pF including jig capacitance

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



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Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING FLOW CHART

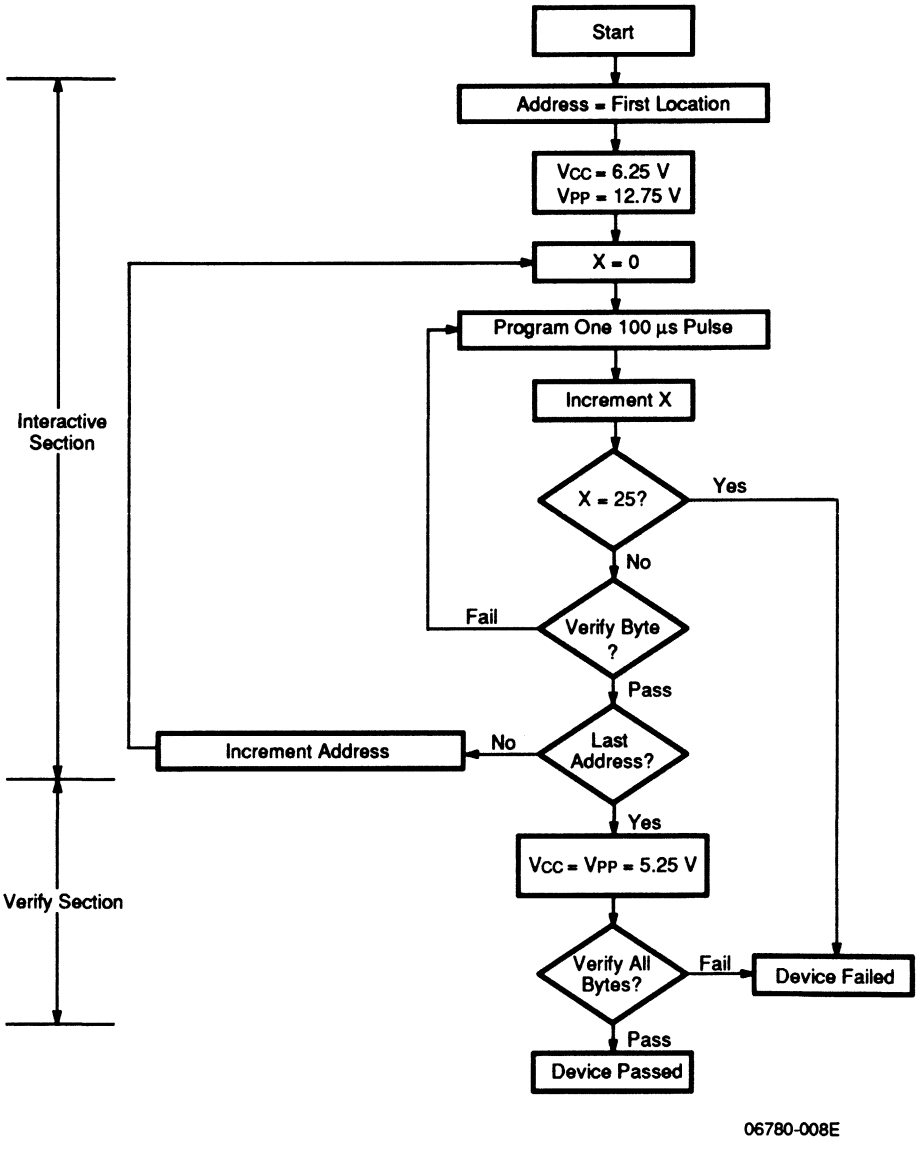


Figure 2. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.5	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

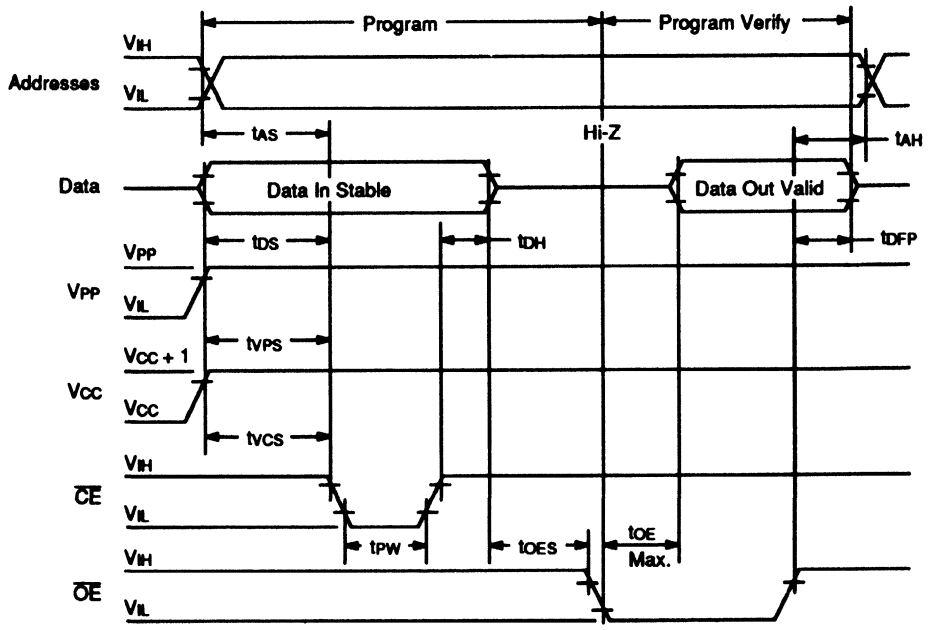
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2, & 3)

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min.	Max.	Unit
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C400, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

FLASHRITE PROGRAMMING ALGORITHM WAVEFORM (Notes 1 & 2)



14971-006B

Notes:

1. The input timing reference level is 0.8 V for a V_{IL} and 2.0 V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Preliminary

Am27C4096

4 Megabit (262,144 x 16-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - 90 ns
- **Low power consumption**
  - 25 µA typical CMOS standby current
- **JEDEC-approved pinout**
  - plug in upgrade of 1 Megabit and 2 Megabit EPROMs
  - 40-pin DIP/PDIP
  - 44-pin LCC/PLCC
- **Single + 5 V power supply**
- **± 10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - typical programming time of 2 minutes
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - both CMOS and TTL input/output compatibility
  - two line control functions

GENERAL DESCRIPTION

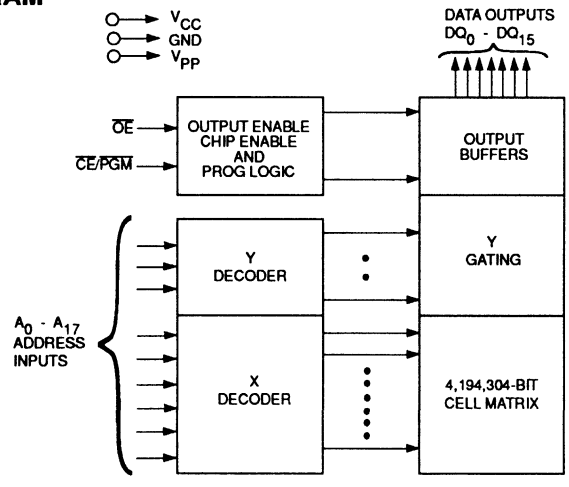
The Am27C4096 is a 4 megabit ultraviolet erasable programmable read-only memory. It is organized as 256K words by 16 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. The Am27C4096 is ideal for use in 16-bit microprocessor systems. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 90 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C4096 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 125 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C4096 supports AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming times of less than 2 minutes.

BLOCK DIAGRAM



11408-001A

Publication# 11408 Rev. B Amendment /0
Issue Date: March 1991

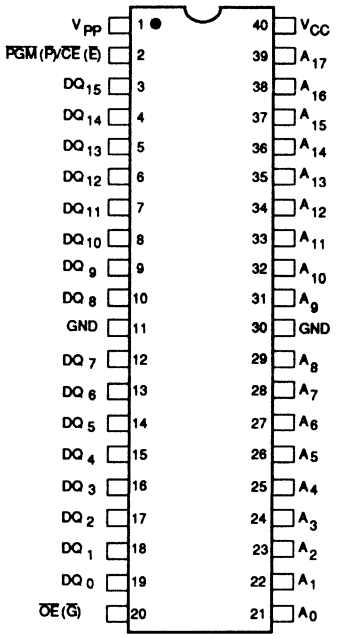
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C4096					
Ordering Part Number V_{CC} ± 5%	-95	-105				-255
V_{CC} ± 10%	-90	-100	-120	-150	-200	-250
Max. Access Time (ns)	90	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	90	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	40	50	50	65	75	100

CONNECTION DIAGRAMS

Top View

DIP



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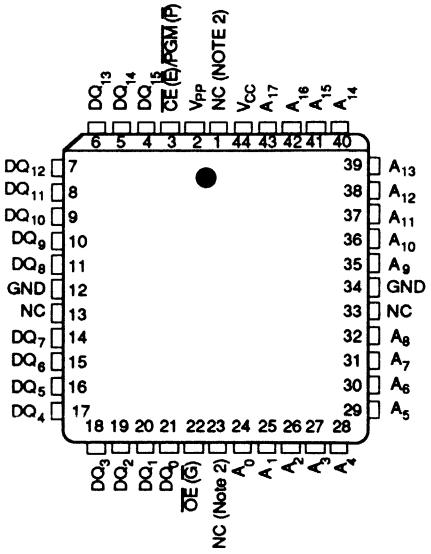
LCC*

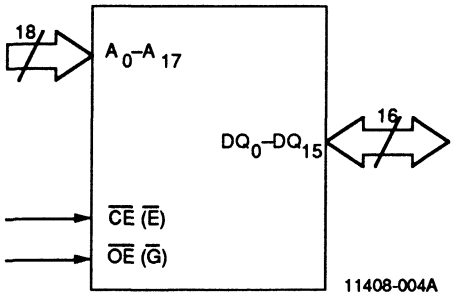


11408-003A

Notes:
1. JEDEC nomenclature is in parentheses.
2. Don't use (DU) for PLCC

* Also available in 44-pin rectangular plastic leaded chip carrier.

LOGIC SYMBOL



11408-004A

PIN DESCRIPTION

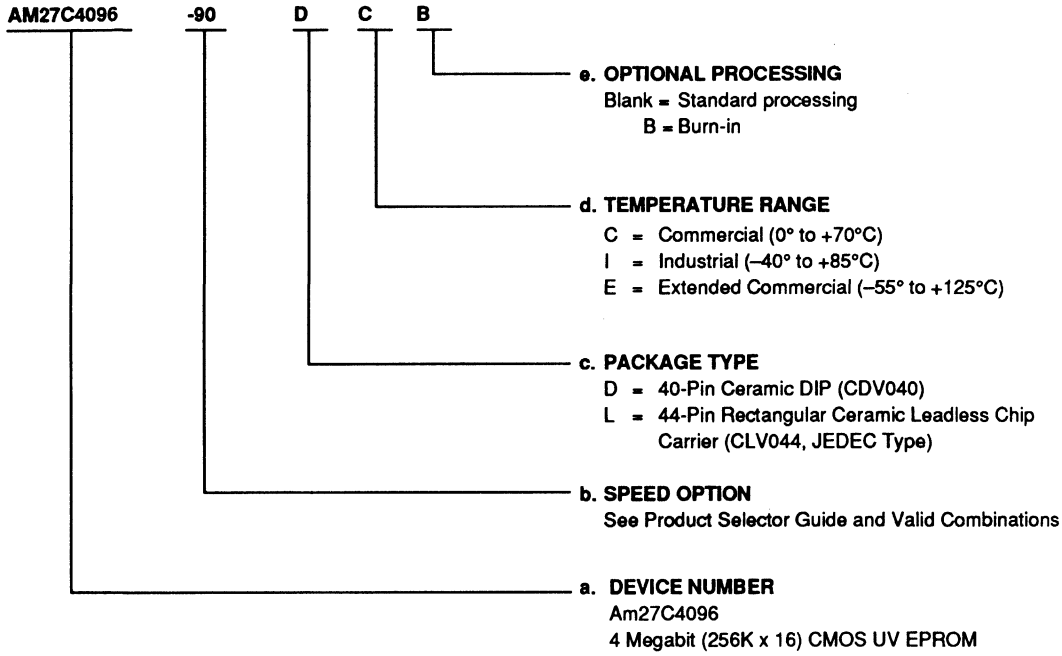
A_0–A_{17}	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ_0–DQ_{15}	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection

ORDERING INFORMATION

EPROM Products

AMD Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C4096-90	DC, DCB, DI, DIB
AM27C4096-95	
AM27C4096-100	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C4096-105	
AM27C4096-120	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27C4096-150	
AM27C4096-200	
AM27C4096-255	

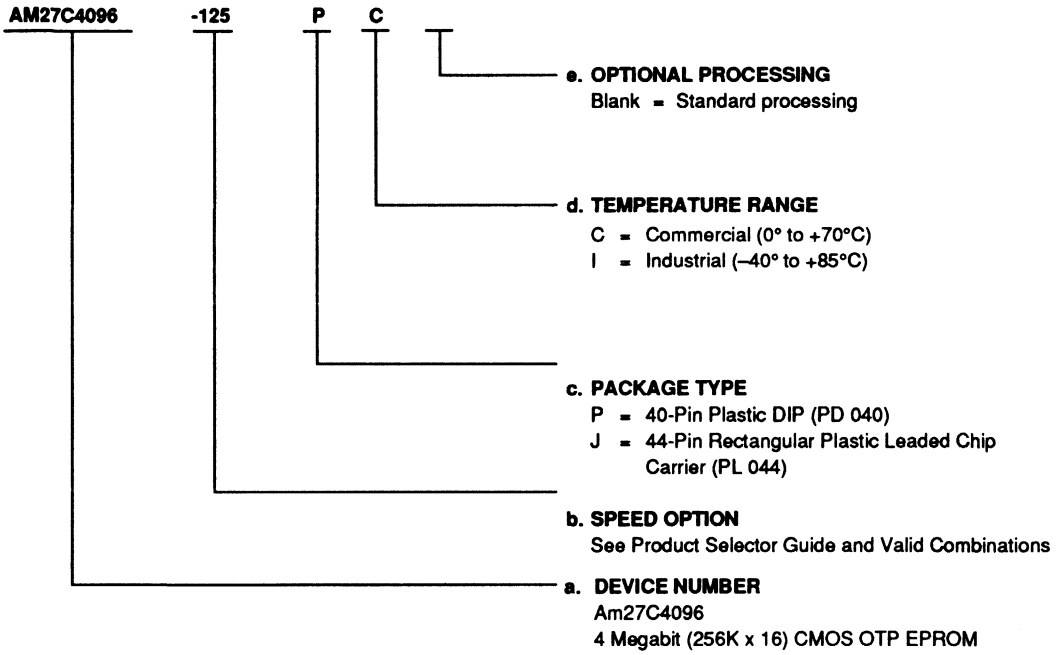
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly-released combinations.

ORDERING INFORMATION
OTP Products (Preliminary)

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM27C4096-125	PC, JC, PI, JI
AM27C4096-150	
AM27C4096-200	
AM27C4096-255	

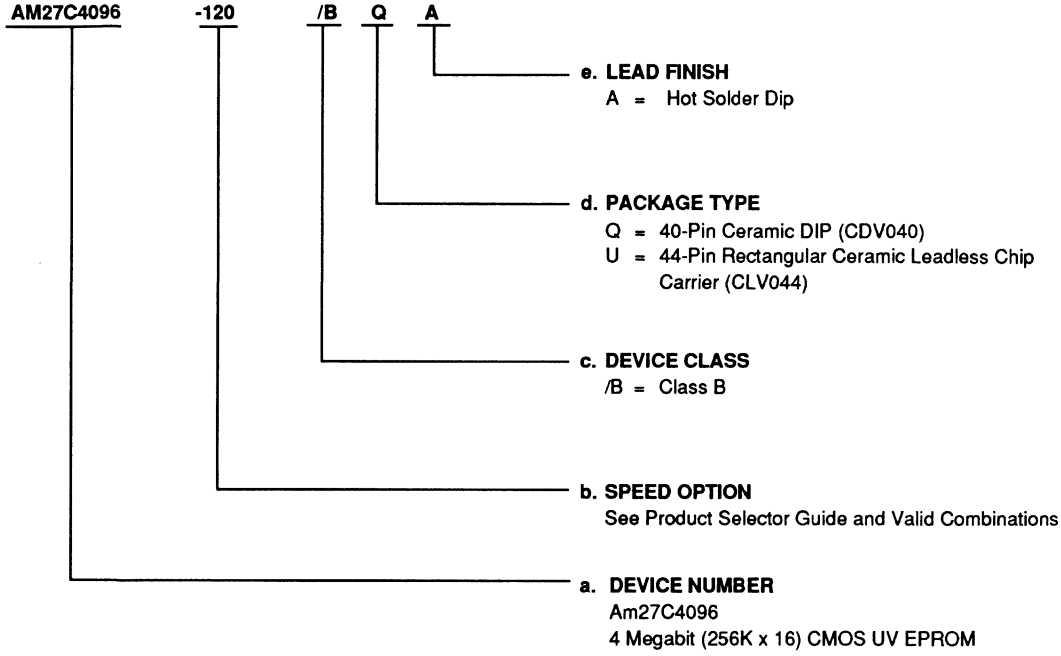
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly-released combinations.

ORDERING INFORMATION
Military APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM27C4096-120	/BQA, /BUA
AM27C4096-150	
AM27C4096-200	
AM27C4096-250	

For other Surface Mount Package options, contact NVD Military Marketing.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly-released combinations.

Group A Tests

Group A tests consist of Subgroups 1,2,3,7,8,9,10,11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C4096

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C4096 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27C4096. This dosage can be obtained by exposure to an ultraviolet lamp—wavelength of 2537 Angstroms (Å)—with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27C4096 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C4096 and similar devices will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, exposure to fluorescent light and sunlight will eventually erase the Am27C4096 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C4096

Upon delivery or after each erasure the Am27C4096 has all 4,194,304 bits in the "ONE" or HIGH state. "ZEROs" are loaded into the Am27C4096 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 16 bits in parallel to the data output pins.

The flowchart (Figure 2) shows AMD's Flashrite algorithm. The Flashrite algorithm reduces programming time by using 100 µs programming pulses and by giving each address only as many pulses as are necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C4096. This part of the algorithm is done at V_{CC} = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5.25$ V.

Program Inhibit

Programming of multiple Am27C4096 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27C4096 may be common. A TTL low-level program pulse applied to an Am27C4096 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V and $\overline{OE}$ HIGH will program that Am27C4096. A high-level $\overline{CE}$ input inhibits the other Am27C4096 devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C4096.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A_9 of the Am27C4096. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code, and byte 1 ($A_0 = V_{IH}$), the device identifier code. For the Am27C4096, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ_7) defined as the parity bit.

Read Mode

The Am27C4096 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27C4096 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27C4096 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1-µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7-µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode \ Pins		$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A_0	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	Hi-Z
Standby (TTL)		V_{IH}	X	X	X	X	Hi-Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	Hi-Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IH}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	Hi-Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	X	19H

Notes:

1. X = Either V_{IH} or V_{IL}
2. V_H = 12.0 ± 0.5 V
3. $A_1 - A_8 = A_{10} - A_{17} = V_{IL}$
4. See DC Programming Characteristics for V_{PP} voltage during programming.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature

OTP products	–65° to +125°C
All other products	–65° to +150°C
Ambient Temperature with Power Applied	–55° to +125°C
Voltage with Respect to Ground:	
All pins except A_9, V_{PP}, V_{CC} (Note 1)	–0.6 to V_{CC} + 0.6 V
A_9 and V_{PP} (Note 2)	–0.6 to +13.5 V
V_{CC}	–0.6 to +7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:

1. During transitions, the inputs may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.
2. During transitions, A_9 and V_{PP} may overshoot GND to –2.0 V for periods of up to 20 ns. A_9 and V_{PP} must not exceed 13.5 V for any period of time.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0° to +70°C

Industrial (I) Devices

Case Temperature (T_C)	–40° to +85°C

Extended Commercial (E) Devices

Case Temperature (T_C)	–55° to +125°C

Military (M) Devices

Case Temperature (T_C)	–55° to +125°C

Supply Read Voltages:

V_{CC} for Am27C4096-XX5	+4.75 to +5.25 V
V_{CC} for Am27C4096-XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 4, 5, and 8)

(for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted)

TTL and NMOS

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current		C/I Devices		5.0	µA
			E/M Devices		10.0	
I_{CC1}	V_{CC} Active Current (Notes 5 & 9)	$\overline{CE}$ = V_{IL}, f = 5 MHz I_{OUT} = 0 mA (Open Outputs)	C/I Devices		50	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}	C/I Devices		1.0	mA
			E/M Devices		1.0	
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

CMOS

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA		V_{CC} – 0.8		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			0.7 V_{CC}	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		5.0	µA
			E/M Devices		10.0	
I_{CC1}	V_{CC} Active Current (Notes 5 & 9)	$\overline{CE}$ = V_{IL}, f = 5 MHz I_{OUT} = 0 mA (Open Outputs)	C/I Devices		50	mA
			E/M Devices		60	
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	C/I Devices		100	µA
			E/M Devices		150	
I_{PP1}	V_{PP} Current During Read (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

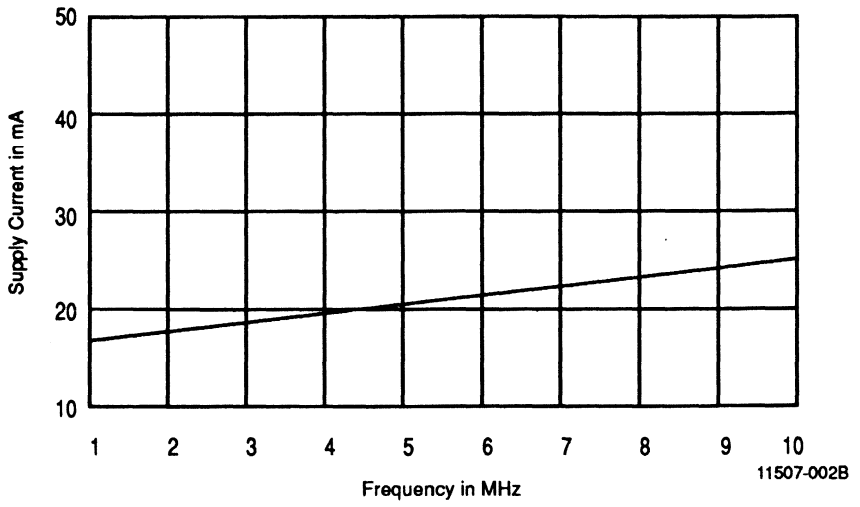


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.0 V, T = 25°C

CAPACITANCE (Notes 2, 3, and 7)

Parameter Symbol	Parameter Description	Test Conditions	CDV040		CLV044		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN}	Input Capacitance	V_{IN} = 0 V	7	12	5	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	10	15	8	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled, not 100% tested.
4. **Caution:** the Am27C4096 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
5. I_{CC1} is tested with OE = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = +25°C, f = 1 MHz.
8. Minimum DC Input Voltage is -0.5 V. During transitions, the inputs overshoot to -2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} +2.0 V for periods less than 20 ns.
9. For typical supply current values at various frequencies, refer to Figure 1.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified. (Notes 1, 3, and 4)

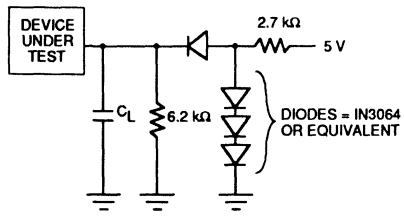
(for APL Products, Group A, Subgroups 9, 10, and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C4096						Unit
JEDEC	Standard				-90, -95	-100, -105	-120, -125	-150	-200	-255 -250	
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min.	–	–	–	–	–	–	ns
				Max.	90	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min.	–	–	–	–	–	–	ns
				Max.	90	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min.	–	–	–	–	–	–	ns
				Max.	40	50	50	65	75	100	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.	0	–	0	0	0	0	ns
				Max.	30	40	40	50	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, CE, or OE, whichever ocurred first		Min.	0	0	0	0	0	0	ns
				Max.	–	–	–	–	–	–	

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled, not 100% tested.
3. **Caution:** The Am27C4096 must not be removed from (or inserted into) a socket or board when V_{pp} or V_{cc} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level — Inputs: 0.8 to 2.0 V
   Outputs: 0.8 to 2.0 V

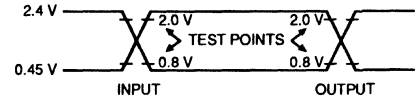
SWITCHING TEST CIRCUIT



C_L = 100 pF including jig capacitance.

10205A-004A

SWITCHING TEST WAVEFORM



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Input pulse rise and fall times are ≤ 20 ns.

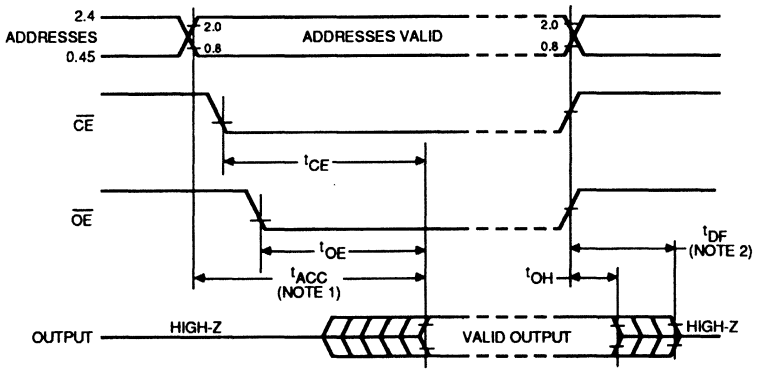
10205B-009A

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

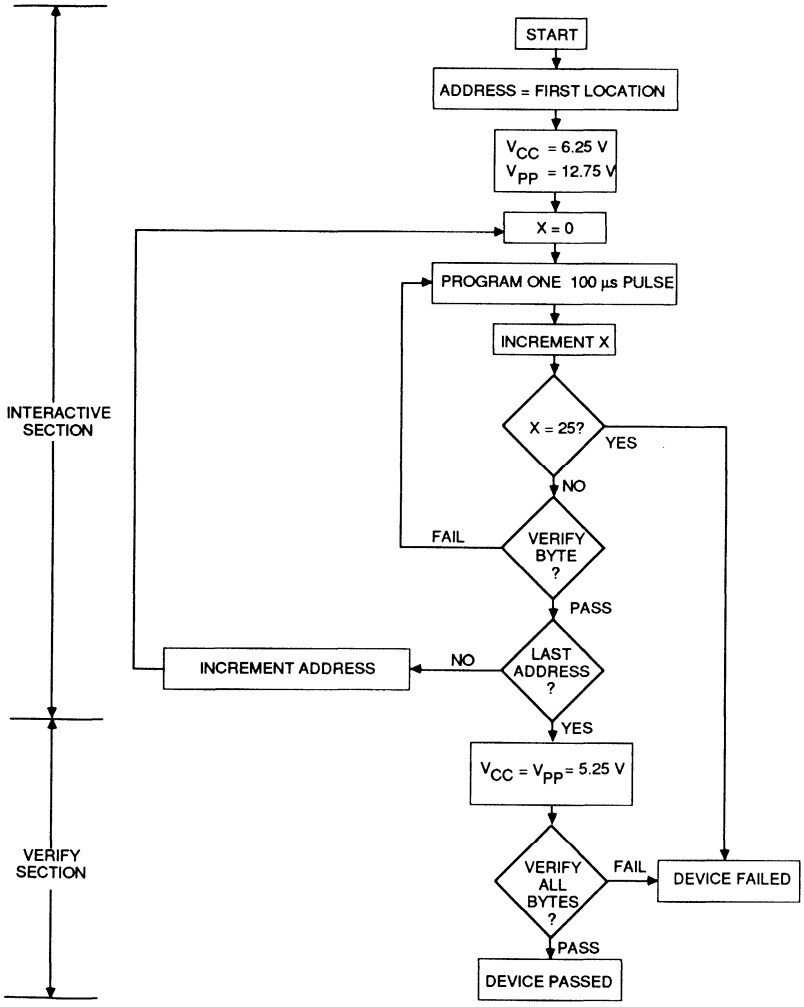
SWITCHING WAVEFORMS



10205A-005A

Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.



10205B-008A

Figure 2. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ± 5°C) (Notes 1, 2, and 3)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.5	0.8	V
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC3}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		50	mA
V_{CC1}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP1}	Flashrite Programming Voltage		12.5	13.0	V

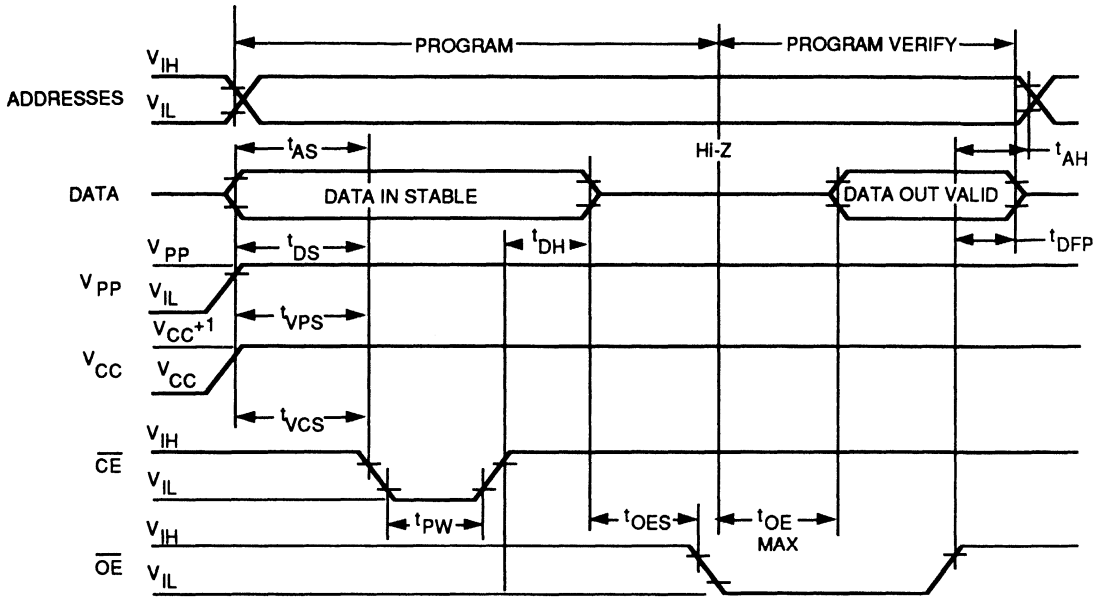
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ± 5°C) (Notes 1, 2, and 3)

Parameter Symbols		Parameter Description	Min.	Max.	Unit
JEDEC	Standard				
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. When programming the Am27C4096, a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients that may damage the device.
3. Programming characteristics are sampled but not 100% tested at worst-case conditions.

FLASHRITE PROGRAMMING ALGORITHM WAVEFORM (Notes 1 and 2)



Notes: 14971-006B

1. The input timing reference level is 0.8 V for a V_{IL} and 2.0 V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Advance Information

Am27C080

8 Megabit (1,048,576 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - 120 ns
- **Low power consumption**
  - 25 µA typical CMOS standby current
- **JEDEC-approved pinout**
  - plug in upgrade of 2 and 4 Megabit EPROMs
  - easy upgrade from 28-pin JEDEC EPROMs
- **Single + 5 V power supply**
- **± 10% power supply tolerance available**
- **100% Flashrite™ programming**
  - typical programming time of less than 5 minutes
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**
- **High noise immunity**
- **Compact 32-pin DIP, PDIP, LCC and PLCC packages**
- **Versatile features for simple interfacing**
  - both CMOS and TTL input/output compatibility
  - two line control functions

GENERAL DESCRIPTION

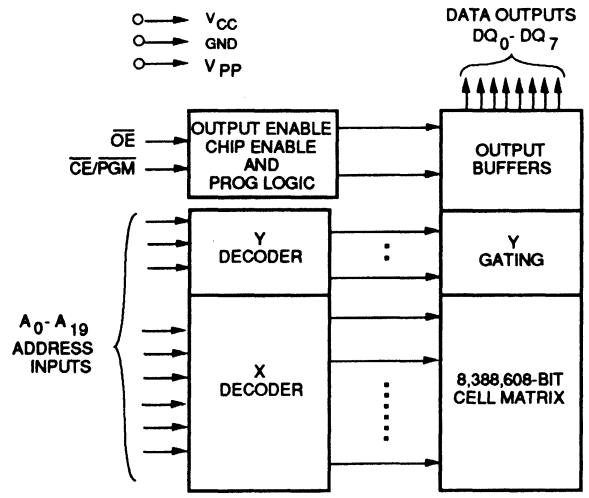
The Am27C080 is an 8 megabit ultraviolet erasable programmable read-only memory. It is organized as 1,024K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any byte can be accessed in less than 120 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C080 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C080 supports AMD's Flashrite™ programming algorithm (10 µs pulses) resulting in typical programming times of less than 5 minutes.

BLOCK DIAGRAM



15453-001A

Publication# 15453 Rev. A Amendment /0
Issue Date: March 1991

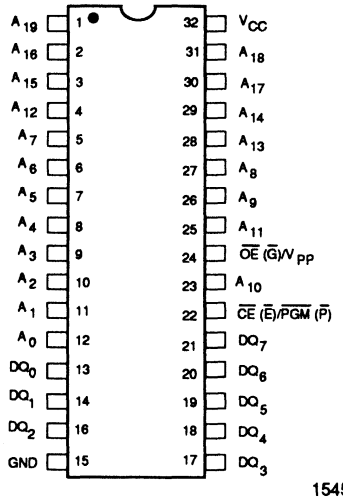
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C080			
Ordering Part Number V_{CC} ± 5%	-125			-255
V_{CC} ± 10%	-120	-150	-200	-250
Max. Access Time (ns)	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	50	65	75	100

CONNECTION DIAGRAMS

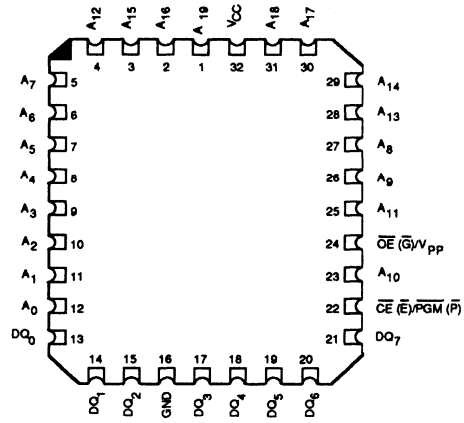
Top View

DIPs



15453-002A

LCC*



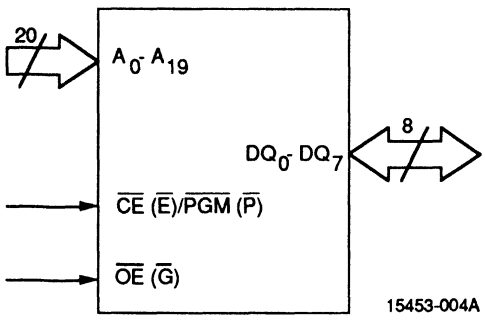
15453-003A

Notes:

1. JEDEC nomenclature is in parentheses.
2. The 32-Pin DIP to 32-Pin LCC configuration varies from the JEDEC 28-Pin DIP to 32-Pin LCC configuration.

* Also available in 32-pin rectangular plastic leaded chip carrier.

LOGIC SYMBOL



15453-004A

PIN DESCRIPTION

A_0– A_{19}	= Address Inputs
$\overline{CE}$ ($\overline{E}$)/$\overline{PGM}$ ($\overline{P}$)	= Chip and Program Enable Input
DQ_0– DQ_7	= Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	= Output Enable Input
V_{CC}	= V_{CC} Supply Voltage
V_{PP}	= Program Supply Voltage
GND	= Ground

Advance Information

Am27C800

8 Megabit (1,048,576 x 8-bit/524,288 x 16-Bit) ROM Compatible CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - 120 ns
- **Low power consumption**
  - 25 µA typical CMOS standby current
- **Industry standard pinout**
  - ROM compatible
  - 42-pin DIP/PDIP
  - 44-pin LCC/PLCC
- **Single +5 V power supply**
- **±10% power supply tolerance standard on most speeds**
- **100% Flashrite™ programming**
  - typical programming time of 5 minutes
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**
- **High noise immunity**
- **Versatile features for simple interfacing**
  - both CMOS and TTL input/output compatibility
  - two line control functions

GENERAL DESCRIPTION

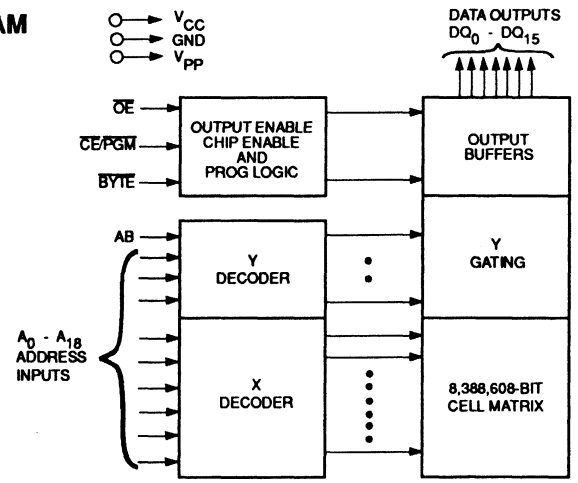
The Am27C800 is an 8 megabit ultraviolet erasable programmable read-only memory that is functionally and pinout compatible with 8 megabit masked ROMs. Under control of the $\overline{BYTE}$ input, the memory can be configured as either a 1024K by 8 bit memory or a 512K by 16 bit memory. It operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages as well as plastic one time programmable (OTP) PDIP and PLCC packages.

Typically, any word can be accessed in less than 120 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C800 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 125 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C800 supports AMD's Flashrite™ programming algorithm (10 µs pulses) resulting in typical programming times of 5 minutes.

BLOCK DIAGRAM



15452-001A

Publication# 15452 Rev. A Amendment /0
Issue Date: March 1991

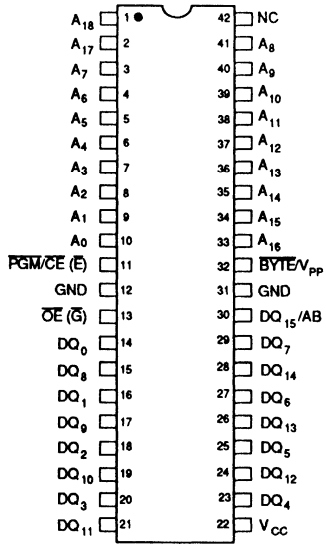
PRODUCT SELECTOR GUIDE

Family Part No.	Am27C800				
Ordering Part Number					
V_{CC} ± 5%	-125				-255
V_{CC} ± 10%	-120	-150	-170	-200	-250
Max. Access Time (ns)	120	150	170	200	250
$\overline{CE}$ ($\overline{E}$) Access Time (ns)	120	150	170	200	250
$\overline{OE}$ ($\overline{G}$) Access Time (ns)	50	65	65	75	100

CONNECTION DIAGRAMS

Top View

42-pin DIP

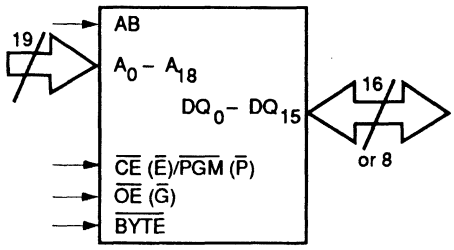


15452-002A

Note:

1. JEDEC nomenclature is in parentheses.
2. LCC and PLCC connection diagrams to be determined.

LOGIC SYMBOL



15452-005A

PIN DESCRIPTION

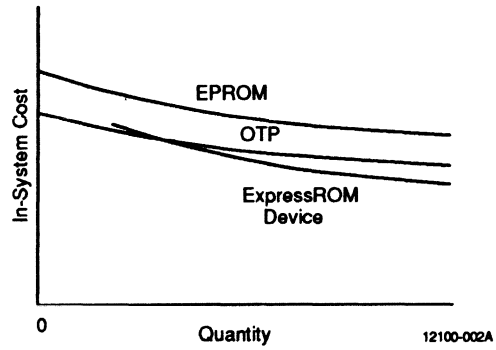
AB	=	Address Input ($\overline{BYTE}$ mode)
A_0–A_{18}	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)/$\overline{PGM}$ ($\overline{P}$)	=	Chip Enable and Program Enable Input
DQ_0–DQ_{15}	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	V_{CC} Supply Voltage
V_{PP}	=	Program Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
$\overline{BYTE}$	=	Byte/Word Switch

Section 3
ExpressROM™ Memories

Section 3
Introduction to ExpressROM™ Memories

ExpressROM Memories are an exciting new product family created by Advanced Micro Devices to offer the system manufacturer a cost savings over standard EPROMs while eliminating many of the disadvantages associated with traditional ROMs. These new memory products provide a lower cost alternative for volume production with stable codes.

ExpressROM Devices are delivered pre-programmed in a low cost plastic package and are 100% compatible with the EPROMs they replace. They address two critical needs of system manufacturers which are vital in today's marketplace: reduced cost and time-to-market. Typically ExpressROM Devices become cost-effective at volumes of 5000 units and offer leadtimes as short as 3-4 weeks.



Pricing Relationships Between ExpressROM Device/EPROM/OTP

An ExpressROM Device is manufactured with the same process as AMD's standard U.V. EPROM equivalent, with the topside passivation layer for plastic encapsulation. Since a standard EPROM die is used, you are assured that the ExpressROM family is identical in architecture, density, and pinout to both AMD's current and future generations of high performance CMOS EPROMs.

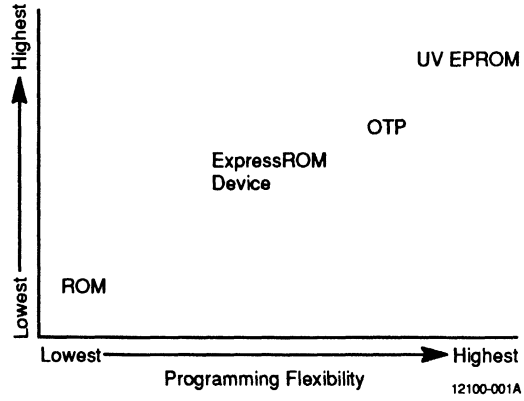
ExpressROM wafers are inventoried untested and unprogrammed. Upon verification of your code, the wafers are sorted, packaged and tested. Every device is rigorously tested with your code under both AC and DC operating conditions prior to shipment. Also, because ExpressROM Memories are shipped board-ready with factory guaranteed quality, your ship-to-stock or Just-In-Time programs can be easily implemented. At Advanced Micro Devices, we ship them the way you want them—ready for your system. And there are none of the delays, costs or risks normally associated with custom ROMs.

Non-Volatile Memory Alternatives

	UV EPROM	OTP	ExpressROM Device	ROM
Leadtime	Manufacturers Leadtime	Manufacturers Leadtime	3 - 4 Weeks	8 - 12 Weeks
Set-up Charge	No	No	No	Yes
Minimum Quantity	0	0	5K	25K
Fully Tested Custom Pattern	No	No	Yes	Yes
User Programming Required	Yes	Yes	No	No
Auto Insertion	No	Yes	Yes	Yes
Flexibility	Total	Cannot Reprogram	Fixed 4 Weeks Prior To Use	Fixed 12 Weeks Prior to Use

Plastic packaging inherently provides a cost savings over standard EPROMs packaged in expensive windowed ceramic DIPs. Due to simplified test requirements, ExpressROM Devices can even cost less than unprogrammed OTP EPROMs. However, component price is only a small part of your true in-system cost. ExpressROM Devices allow you to eliminate or reduce costs in several other areas: programming, testing, labeling and production. Since ExpressROM Memories are delivered with your code, you will reap savings by eliminating programming costs and associated yield losses. Incoming inspection may often be eliminated since your ExpressROM Devices have been thoroughly tested and are guaranteed to operate to full specifications with your code! Additional in-house cost savings can be attained by using automatic insertion equipment in lieu of manual placement into sockets.

ExpressROM Devices were designed to provide a low cost alternative for EPROM users without the liabilities of other non-volatile memory alternatives. Although ROMs have a lower component cost, they are economically feasible only at high volume and have the risks of long leadtimes and limited manufacturing flexibility. While OTP EPROMs offer the systems manufacturer the ability to respond to varying codes during production, they force the user to incur additional and sometimes hidden costs.



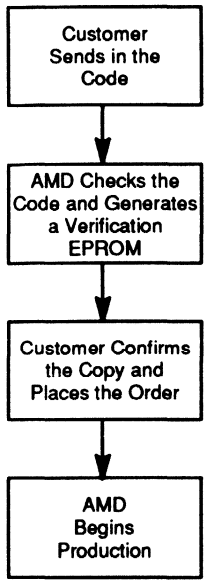
Non-Volatile Memory Alternatives

Our mission at AMD is to deliver you the service and products you demand to build the cost competitive systems that are needed to win in your markets. The ExpressROM Memory provides this opportunity. As one of the world's five largest IC manufacturers and the first to market with a 1 megabit EPROM, we appreciate the value of efficient manufacturing. Compressing time-to-market cycles, improving yields and providing high levels of

quality are invaluable strategies for today's manufacturer. At Advanced Micro Devices we are proud to offer another tool to give our customers this strategic advantage, the ExpressROM Memory: the ROM without the wait!

ORDERING ExpressROM DEVICES

The following procedure outlines the method for ordering an ExpressROM Device. For more information, contact your local AMD sales representative.



1) Send In The Code

Please have your field sales representative provide you with the latest version of the ExpressROM Code Approval Form (see Figure 1). This form will provide all the necessary information required for processing your order. After receiving this form, fill out the Code Transmittal and Ordering Information sections. Then send the form with two (2) master copies of each code being ordered to your field sales representative. To minimize the verification turnaround process, supply two master copies of each code using JEDEC standard dual-in-line (DIP) EPROMs identical in architecture and density as the ExpressROM Device being ordered. Two master copies per code are required in order to guarantee proper code transmission. Please be sure the checksum is clearly identified on each master EPROM.

2) AMD Checks The Code And Generates A Verification EPROM

We check that both EPROMs contain the same code to make certain there was not a mix-up in shipping your codes to the factory as well as ensuring that the integrity of your code has been preserved. After confirming this, a unique 5-digit code designation is assigned. The ordering part number is formed by adding the 5-digit code designation as a suffix to the ExpressROM Device number. See below:

Am27X010–125PC 9 9 9 9 9

DEVICE NUMBER — CODE DESIGNATION

AMD then logs in your code with the 5-digit code designation and generates a verification EPROM in a standard dual-in-line (DIP) package. The verification EPROM along with one of your master EPROMs and the ExpressROM Code Approval Form should be back in your hand for final approval within 2-3 days. The other master EPROM remains at AMD for our records. Please note: the verification EPROM is simply a means of transferring the code and is not necessarily indicative of the ExpressROM product being ordered.

3) Confirm The Copy And Place The Order

Once the verification EPROM is approved, sign the Approval Section of the ExpressROM Code Approval Form and return it to AMD with your purchase order. Upon receipt of the signed form and a purchase order, AMD enters the order and begins production. Logged codes are maintained for 60 days and then deleted if there is no purchase order placed.

TERMS AND CONDITIONS

You should be aware of the following when ordering ExpressROM Devices.

1) AMD will maintain customer code confidentiality.

2) AMD will absorb all initial set-up costs.

3) All orders are subject to minimum quantities.

4) AMD may begin production 30 days in advance of the original schedule date covered by a purchase order and requires 30 days notification for code changes. The customer is liable for all work-in-process covered by the same purchase order.

5) No schedule changes may be made within 30 days of current schedule date.

6) The customer will accept quantities from 95% up to 105% of original ordering quantity per code and be billed accordingly.

7) All unpackaged die product procured by the customer is for use exclusively in the customer's end products. Any other use of die product must be approved in writing by AMD.

ExpressROM™ Code Approval Form

CODE TRANSMITTAL AND ORDERING INFORMATION SECTION

Rev. 3 2/1/91

Please complete items 1 thru 10. To minimize the verification turn-around process, supply 2 master copies of each code using JEDEC standard dual-in-line (DIP) EPROMs of the same architecture and density as the ExpressROM™ Device being ordered. Also, be sure the checksum is clearly identified on each master EPROM.

CODE TRANSMITTAL SECTION

1. *Company Name:* _____ 2. *Date:* _____

3. *Incoming Masters part #:* _____ 4. *Masters Checksum:* _____

ORDERING INFORMATION SECTION

Please check the appropriate ExpressROM™ Memory data sheet for valid combinations and mark appropriate boxes below:

5. *Part#:*
- ❑ Am27X64
- ❑ Am27X128
- ❑ Am27X256
- ❑ Am27X512
- ❑ Am27X010
- ❑ Am27X100
- ❑ Am27X1024
- ❑ Am27X020
- ❑ Am27X2048
- ❑ Am27X040
- ❑ Am27X400
- ❑ Am27X4096

6. *Speed and Vcc:*
- ❑ 100ns
- ❑ 120ns
- ❑ 150ns
- ❑ 170ns
- ❑ 200ns
- ❑ 250ns
- ❑ ±5%
- ❑ ±10%

7. *Package and Temperature:*
- ❑ Plastic Dip
- ❑ PLCC
- ❑ Die
- ❑ Commercial (0°C to +70°C)
- ❑ Industrial (-40°C to +85°C)

8. *AMD Standard Part Number:* _____

9. *Customer Ordering Part Number:* _____

10. *Please select a, b or c for exact marking and complete the blank sections (12 characters per line including spaces, © = 2 spaces).*

a. *AMD Standard:*
AMD Logo
ExpressROM™ Logo
AM27X_____
Date Code

b. *AMD Standard+Customer Part:*
AMD Logo
ExpressROM™ Logo
AM27X_____
_____
Date Code

c. *Customer Part #:*
AMD Logo
ExpressROM™ Logo
_____
©_____
Date Code

APPROVAL SECTION TERMS AND CONDITIONS

AMD will maintain customer code confidentiality.
AMD will absorb all initial set-up costs.
AMD may begin production 30 days in advance of the original schedule date covered by a purchase order and requires 30 days minimum notification for code changes.
The customer is liable for all work-in-process covered by the same purchase order.
No schedule changes may be made within 30 days of current schedule date.
All unpackaged die product procurred by the customer is for use exclusively in the customer's end products. Any other use of die product must be approved in writing by AMD.
All orders are subject to minimum quantities.
The customer will accept quantities from 95% to 105% of original ordering quantitiy per code and be billed accordingly.

AMD Standard Part # Am27X _____ Checksum _____

Customer Signature: _____ Date: _____

Name (Print): _____ Title: _____

Figure 1. Sample of the ExpressROM Code Approval Form

Contact your local AMD sales representative for latest version

Am27X64

8,192 x 8-Bit CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - Factory optimized programming
  - Fully tested and guaranteed
  - Lower cost
- **As a Mask ROM alternative:**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High noise immunity**
- **High performance CMOS technology**
  - Fast access time — 100 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP, plastic leaded chip carrier (PLCC), and in DIE form**
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**

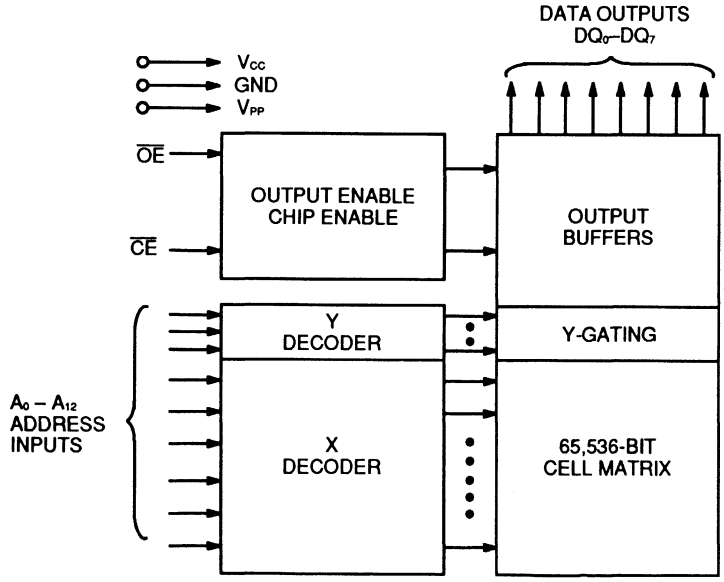
GENERAL DESCRIPTION

The Am27X64 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 8,192 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM Devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 100 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X64 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

BLOCK DIAGRAM



12081B-001

Publication # 12084 Rev. C Amendment/0
Issue Date: March 1991

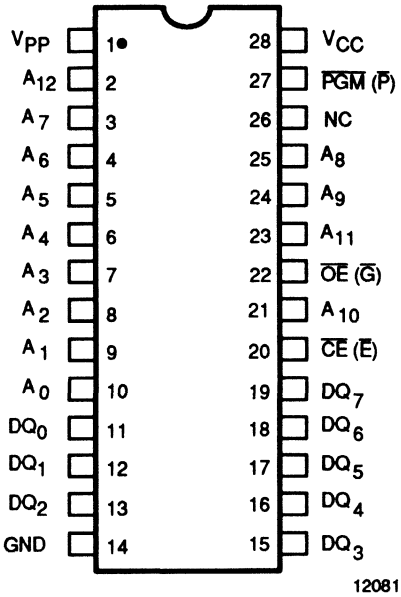
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X64				
Ordering part No: ±5% VCC Tolerance	-105	-125			
±10% VCC Tolerance	—	-120	-150	-200	-250
Max Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	50	65	75	100

CONNECTION DIAGRAMS

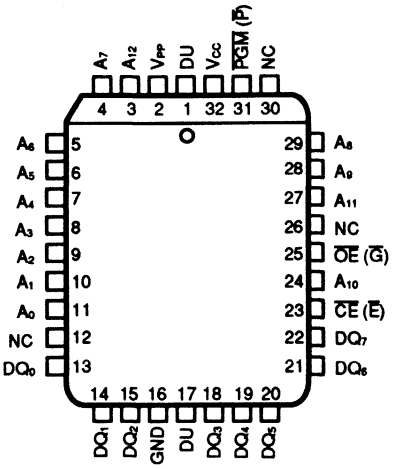
Top View

PLASTIC DIP



12081B-002

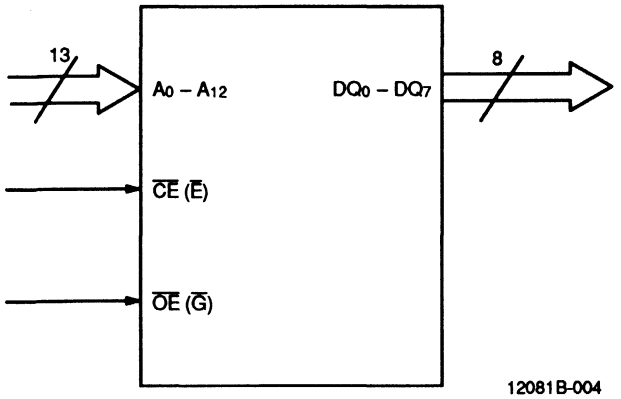
PLCC



12084-009A

Note: JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



12081B-004

PIN DESCRIPTION

$A_0 - A_{12}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_7$	=	Data Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{PP}	=	Vcc Supply Voltage
Vcc	=	Vcc Supply Voltage
$\overline{PGM}$ ($\overline{P}$)	=	Enable Input
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation

AM27X64 -105 P C 99999

e. CODE DESIGNATION
Assigned by AMD

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)

c. PACKAGE TYPE
P = 28-Pin Plastic DIP (PD 028)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
X = Die

b. SPEED OPTION
See Product Selector Guide and Valid Combinations

a. DEVICE NUMBER/DESCRIPTION
Am27X64
8K x 8-Bit CMOS ExpressROM Device

Valid Combinations	
AM27X64-105 AM27X64-120 AM27X64-125 AM27X64-150 AM27X64-200 AM27X64-250	PC, JC, XC, PI, JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X64 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X64 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X64 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM Device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	High Z
Standby (TTL)	V_{IH}	X	X	X	High Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC}	–0.6 to V_{CC} + 0.6 V
V_{CC}	–0.6 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note:
During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to +70°C

Industrial (I) Devices

Case Temperature (T_C)	–40 to +85°C

Supply Read Voltages:

V_{CC} for Am27X64–XX5	+4.75 to +5.25 V
V_{CC} for Am27X64–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
TTL and NMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{PP}	V_{CC} Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA
CMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		25	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA
I_{PP}	V_{CC} Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 2, 3 & 7)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	9	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27X64 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns.
   Maximum DC voltage on input and output may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

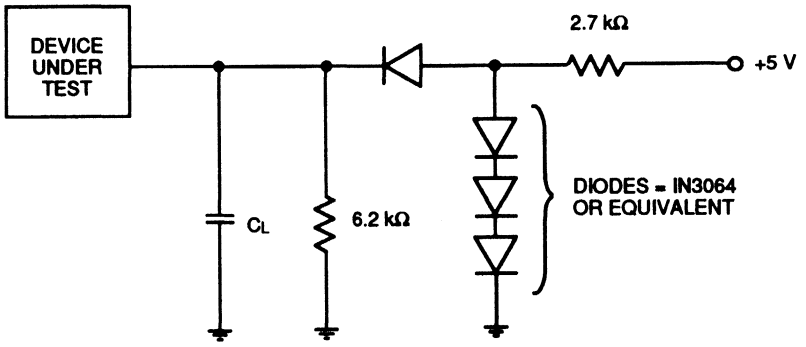
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 & 4)

Parameter Symbol		Parameter Description	Test Conditions		-105	-125 -120	-150	-200	-250	Unit
JEDEC	Standard									
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.						ns
				Max.	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.						ns
				Max.	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.						ns
				Max.	40	50	65	75	100	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.						ns
				Max.	30	30	30	30	30	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	ns
				Max.						

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X64 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level — Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

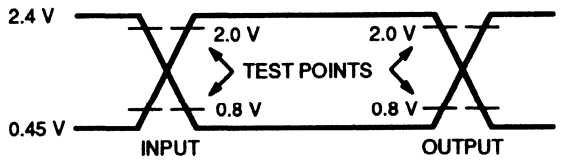
SWITCHING TEST CIRCUIT



10205-004A

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



10205-009A

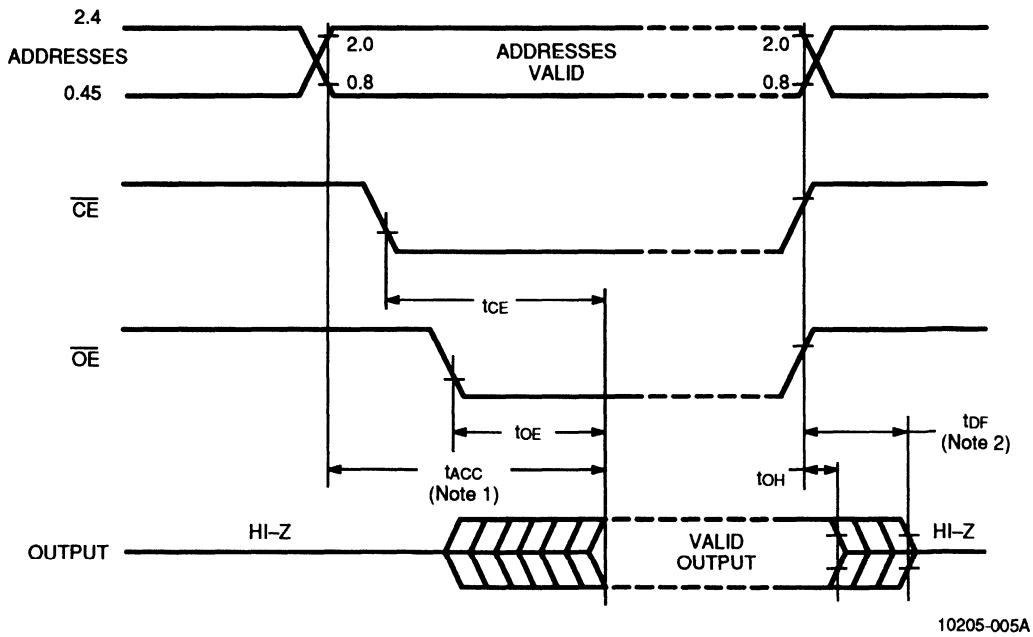
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



10205-005A

Note:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Am27X128

16,384 x 8-Bit CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - Factory optimized programming
  - Fully tested and guaranteed
  - Lower cost
- **As a Mask ROM alternative:**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High noise immunity**
- **High performance CMOS technology**
  - Fast access time — 100 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP, plastic leaded chip carrier (PLCC), and in DIE form**
- **Latch-up protected to 100 mA from −1 V to V_{CC} + 1 V**

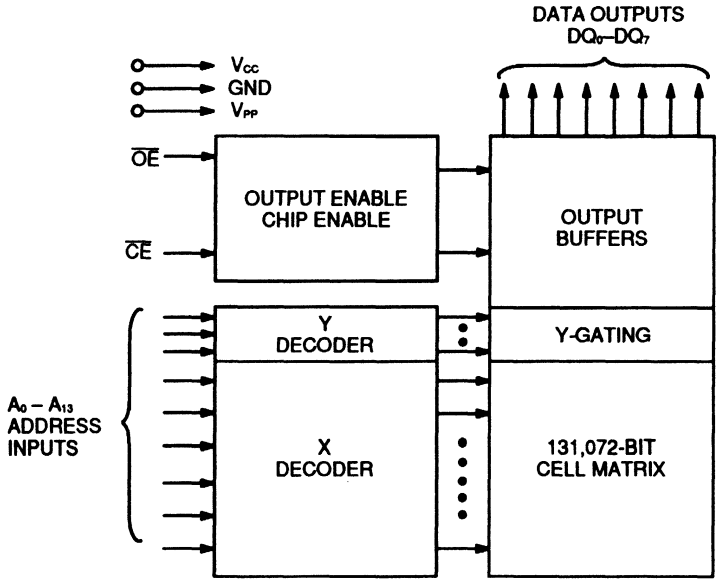
GENERAL DESCRIPTION

The Am27X128 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 16,384 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM Devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 100 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X128 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

BLOCK DIAGRAM



12081B-001

Publication # 12063 Rev. C Amendment/0
Issue Date: March 1991

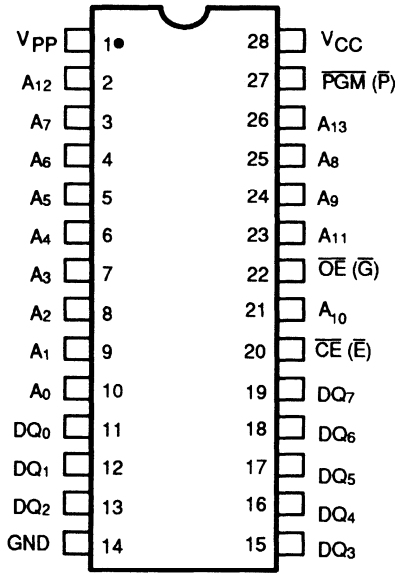
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X128				
Ordering part No: ±5% VCC Tolerance	-105	-125			
±10% VCC Tolerance	—	-120	-150	-200	-250
Max Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	50	65	75	100

CONNECTION DIAGRAMS

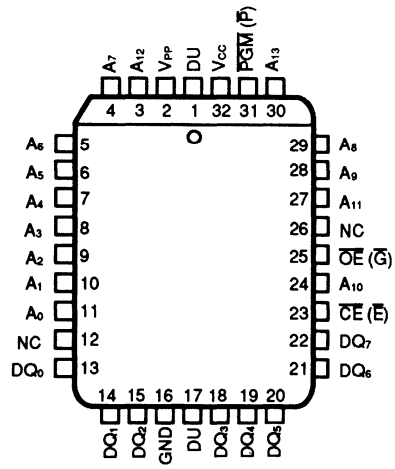
Top View

PLASTIC DIP



12081B-002

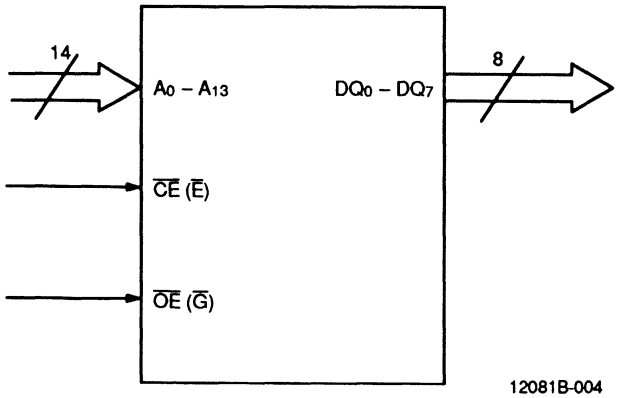
PLCC



12083-009A

Note: JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



12081B-004

PIN DESCRIPTION

A0 – A13	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0 – DQ7	=	Data Inputs/Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
VPP	=	Vcc Supply Voltage
Vcc	=	Vcc Supply Voltage
$\overline{PGM}$ ($\overline{P}$)	=	Enable Input
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation

AM27X128 -105 P C 99999

e. CODE DESIGNATION
Assigned by AMD

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)

c. PACKAGE TYPE
P = 28-Pin Plastic DIP (PD 028)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
X = Die

b. SPEED OPTION
See Product Selector Guide and Valid Combinations

a. DEVICE NUMBER/DESCRIPTION
Am27X128
8K x 8-Bit CMOS ExpressROM Device

Valid Combinations	
AM27X128-105 AM27X128-120 AM27X128-125 AM27X128-150 AM27X128-200 AM27X128-250	PC, JC, XC, PI, JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X128 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X128 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X128 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM Device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	High Z
Standby (TTL)	V_{IH}	X	X	X	High Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC}	–0.6 to V_{CC} + 0.6 V
V_{CC}	–0.6 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note:
During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to +70°C

Industrial (I) Devices

Case Temperature (T_C)	–40 to +85°C

Supply Read Voltages:

V_{CC} for Am27X128–XX5	+4.75 to +5.25 V
V_{CC} for Am27X128–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
TTL and NMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	Vcc Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	Vcc Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{PP}	Vcc Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA
CMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	Vcc Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		25	mA
I_{CC2}	Vcc Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA
I_{PP}	Vcc Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 2, 3 & 7)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	9	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27X128 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns.
   Maximum DC voltage on input and output may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

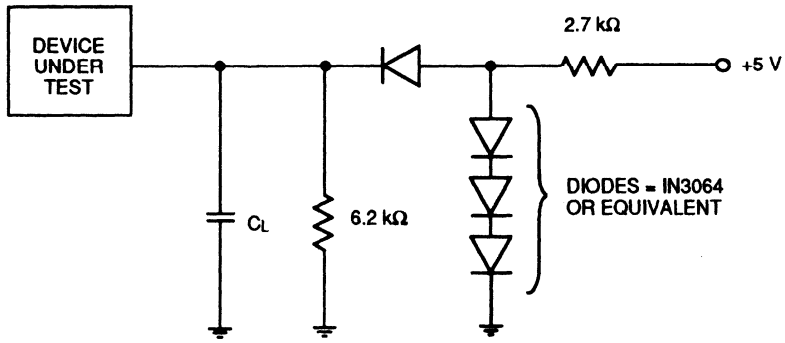
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 & 4)

Parameter Symbol		Parameter Description	Test Conditions		-105	-125 -120	-150	-200	-250	Unit
JEDEC	Standard									
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.						ns
				Max.	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.						ns
				Max.	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.						ns
				Max.	40	50	65	75	100	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.						ns
				Max.	30	30	30	30	30	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	ns
				Max.						

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X128 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level — Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

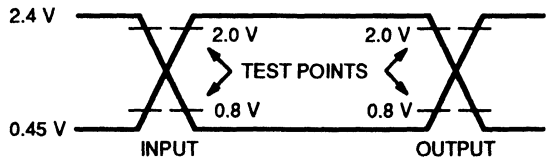
SWITCHING TEST CIRCUIT



10205-004A

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



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AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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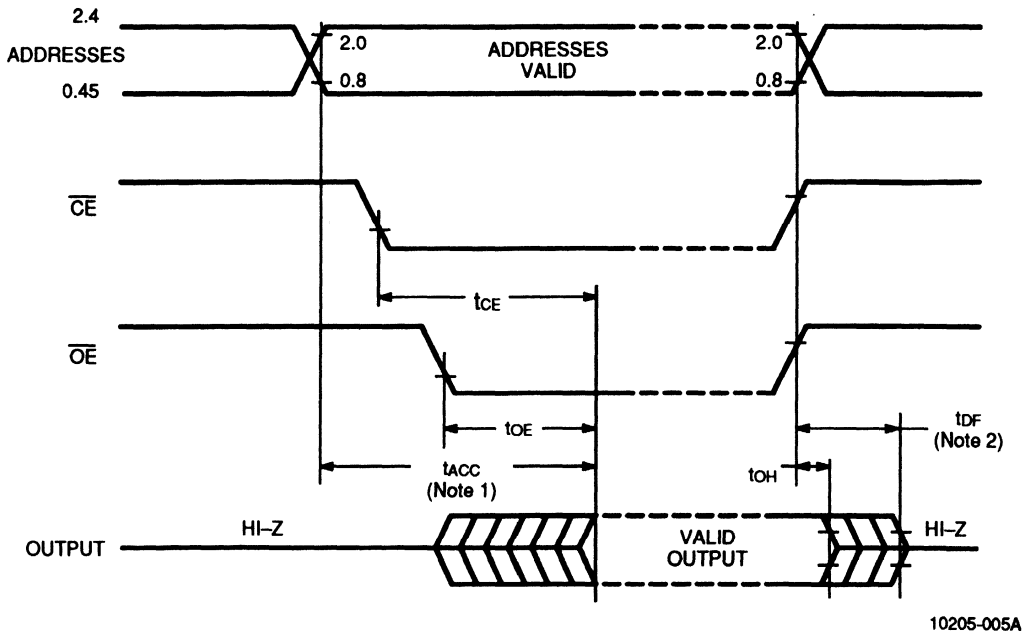
SWITCHING WAVEFORMS



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Note:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Am27X256

32,768 x 8-Bit CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - Factory optimized programming
  - Fully tested and guaranteed
  - Lower cost
- **As a Mask ROM alternative:**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High noise immunity**
- **High performance CMOS technology**
  - Fast access time — 100 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier (PLCC), and in DIE form**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**

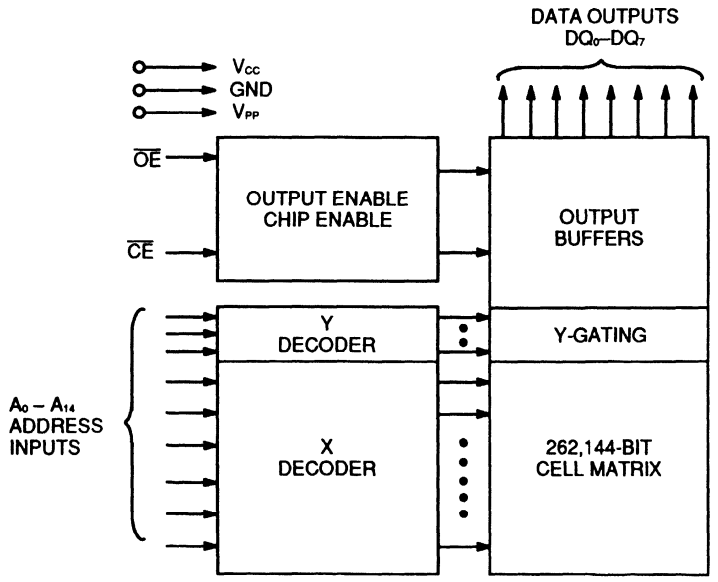
GENERAL DESCRIPTION

The Am27X256 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 32,768 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM Devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 100 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X256 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

BLOCK DIAGRAM



12081B-001

Publication # 12082 Rev. C Amendment/0
Issue Date: March 1991

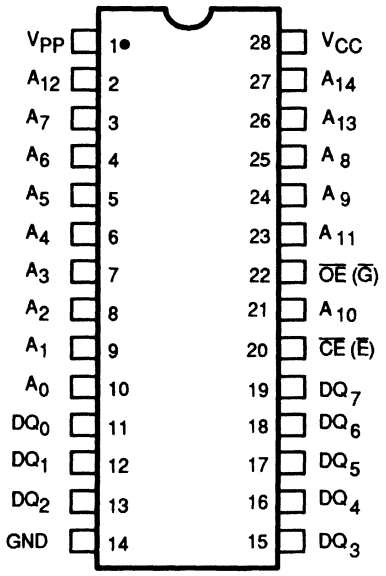
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X256				
Ordering part No: ±5% VCC Tolerance	-105	-125			
±10% VCC Tolerance	—	-120	-150	-200	-250
Max Access Time (ns)	100	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	100	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	50	65	75	100

CONNECTION DIAGRAMS

Top View

PLASTIC DIP



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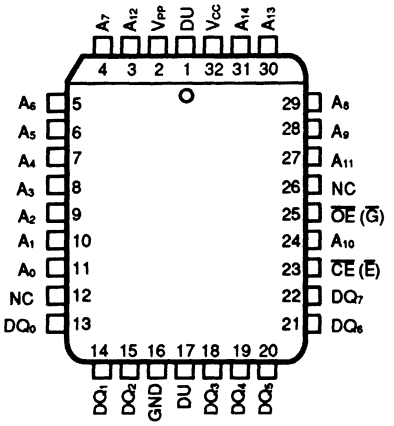
PLCC



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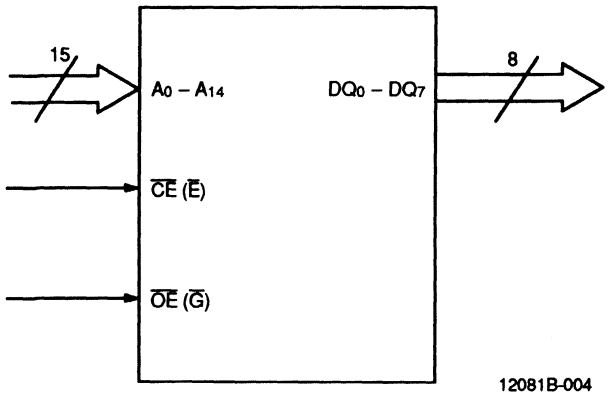
Note: JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



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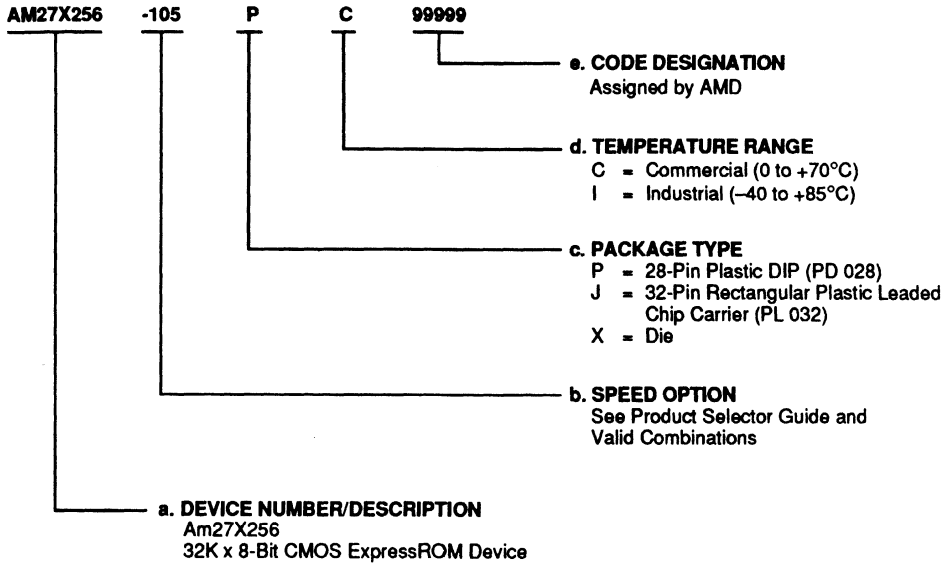
PIN DESCRIPTION

$A_0 - A_{14}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_7$	=	Data Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
V_{CC}	=	Vcc Supply Voltage
V_{PP}	=	Vcc Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation



Valid Combinations	
AM27X256-105 AM27X256-120 AM27X256-125 AM27X256-150 AM27X256-200 AM27X256-250	PC, JC, XC, PI, JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X256 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X256 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM Device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	High Z
Standby (TTL)	V_{IH}	X	X	High Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC}	–0.6 to V_{CC} + 0.6 V
V_{CC}	–0.6 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note:
During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to +70°C

Industrial (I) Devices

Case Temperature (T_C)	–40 to +85°C

Supply Read Voltages:

V_{CC} for Am27X256–XX5	+4.75 to +5.25 V
V_{CC} for Am27X256–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
TTL and NMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	Vcc Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	Vcc Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{PP}	Vcc Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA
CMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	Vcc Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		25	mA
I_{CC2}	Vcc Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA
I_{PP}	Vcc Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 2, 3 & 7)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	8	12	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	9	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27X256 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns.
   Maximum DC voltage on input and output may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

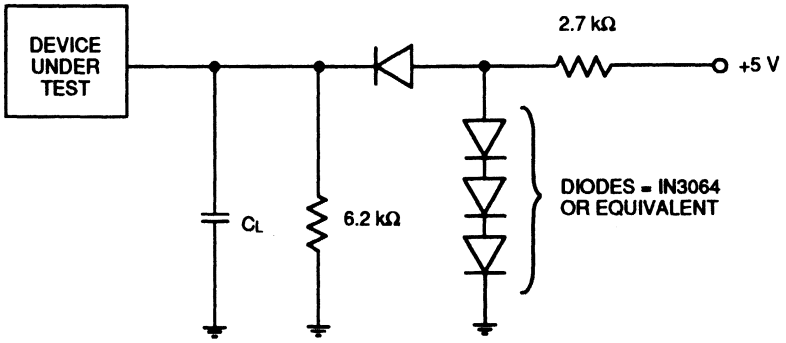
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 & 4)

Parameter Symbol		Parameter Description	Test Conditions		-105	-125 -120	-150	-200	-250	Unit
JEDEC	Standard									
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.						ns
				Max.	100	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.						ns
				Max.	100	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.						ns
				Max.	40	50	65	75	100	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.						ns
				Max.	30	30	30	30	30	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	0	ns
				Max.						

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X256 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level — Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

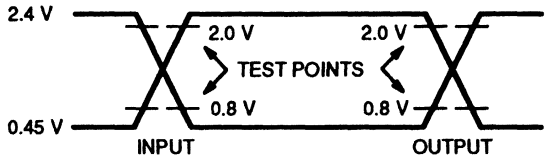
SWITCHING TEST CIRCUIT



10205-004A

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



10205-009A

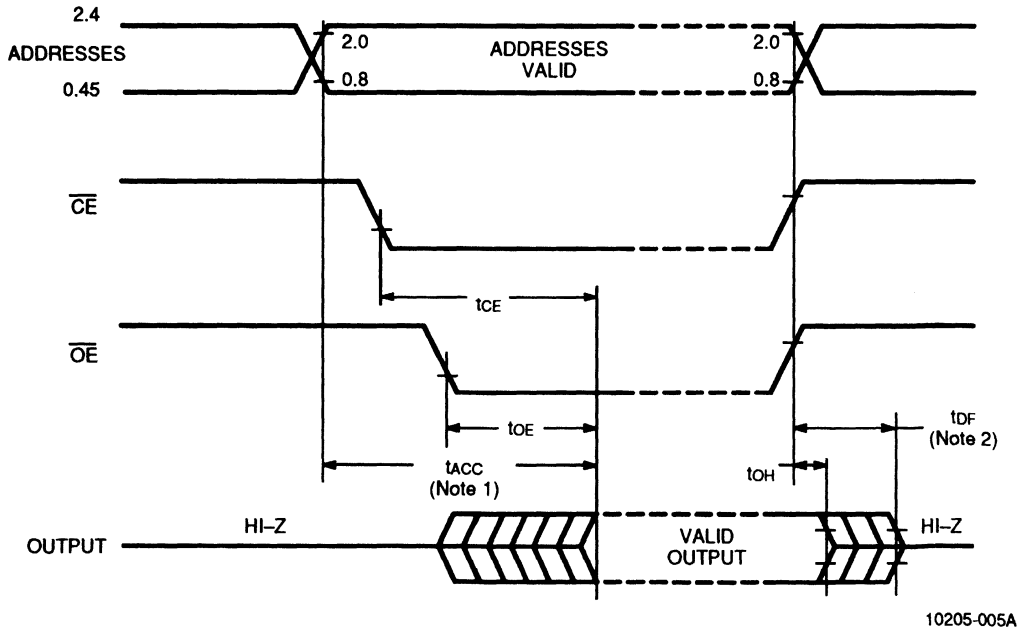
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



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Note:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Am27X512

65,536 x 8-Bit CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - Factory optimized programming
  - Fully tested and guaranteed
  - Lower cost
- **As a Mask ROM alternative:**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High noise immunity**
- **High performance CMOS technology**
  - Fast access time — 120 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier (PLCC), and in DIE form**
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**

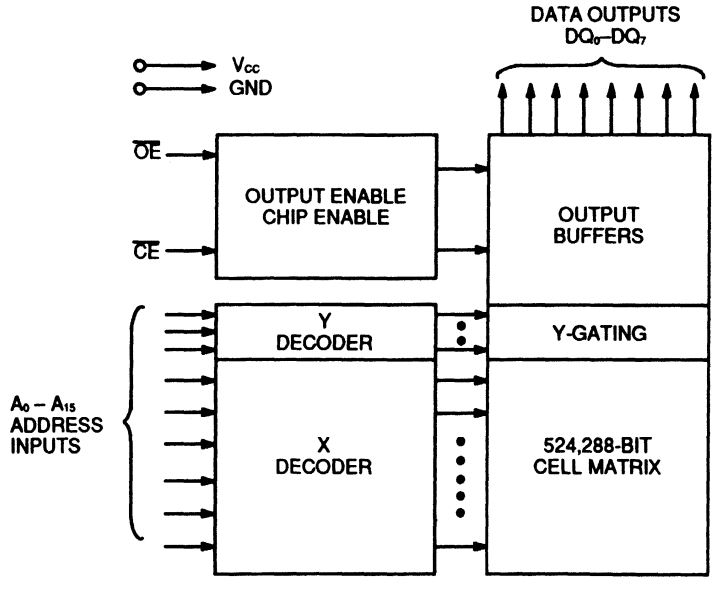
GENERAL DESCRIPTION

The Am27X512 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 65,536 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM Devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 120 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X512 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

BLOCK DIAGRAM



12081B-001

Publication # 12081 Rev. C Amendment/0
Issue Date: March 1991

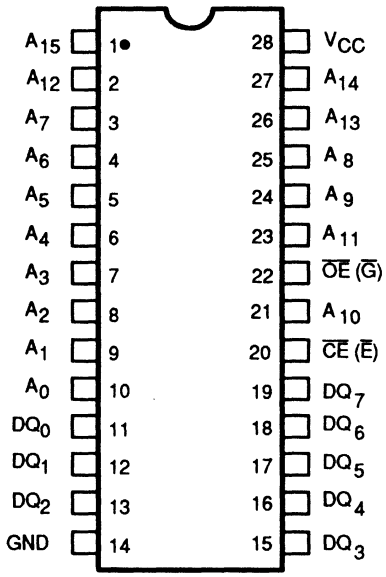
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X512			
Ordering part No:				
±5% VCC Tolerance	-125	-155		
±10% VCC Tolerance	—	-150	-200	-250
Max Access Time (ns)	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	50	75	100

CONNECTION DIAGRAMS

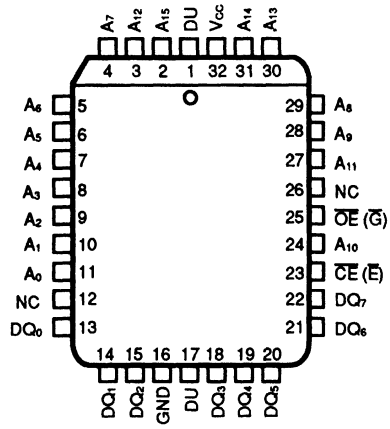
Top View

PLASTIC DIP



12081B-002

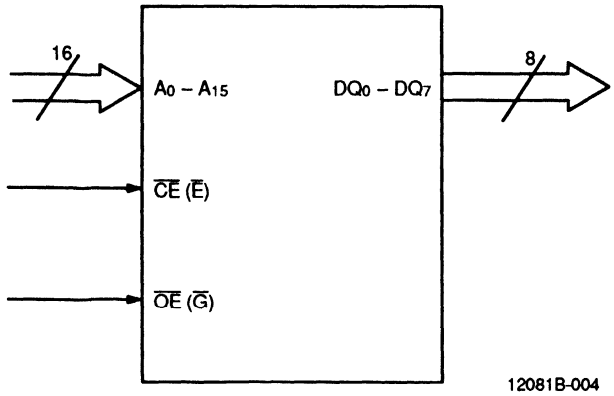
PLCC



11557-003A

Note: JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



12081B-004

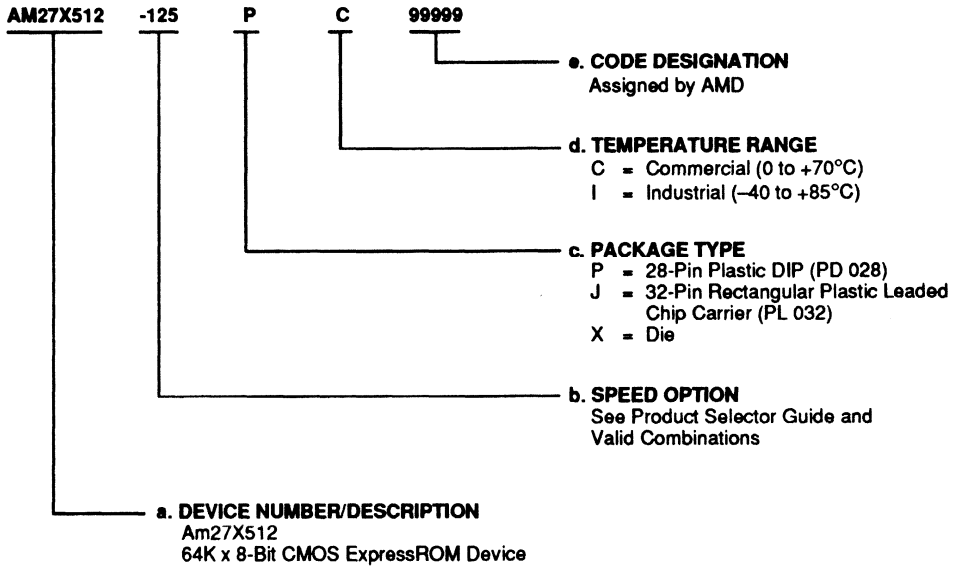
PIN DESCRIPTION

$A_0 - A_{15}$	= Address Inputs
$\overline{CE}$ ($\overline{E}$)	= Chip Enable Input
$DQ_0 - DQ_7$	= Data Outputs
$\overline{OE}$ ($\overline{G}$)	= Output Enable Input
V_{CC}	= V_{CC} Supply Voltage
GND	= Ground
NC	= No Internal Connection
DU	= No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation



Valid Combinations	
AM27X512-125 AM27X512-150 AM27X512-155 AM27X512-200 AM27X512-250	PC, JC, XC, PI, JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X512 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X512 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM Device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	Outputs
Read	V_{IL}	V_{IL}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	High Z
Standby (TTL)	V_{IH}	X	High Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC}	–0.6 to V_{CC} + 0.6 V
V_{CC}	–0.6 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note:
During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to +70°C

Industrial (I) Devices

Case Temperature (T_C)	–40 to +85°C

Supply Read Voltages:

V_{CC} for Am27X512–XX5	+4.75 to +5.25 V
V_{CC} for Am27X512–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 3, 4 & 6)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
TTL and NMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 10 MHz, $I_{OUT} = 0$ mA (Open Outputs)		40	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$		1	mA
CMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	V_{CC} Active Current (Note 4)	$\overline{CE} = V_{IL}$, f = 10 MHz, $I_{OUT} = 0$ mA (Open Outputs)		40	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA

CAPACITANCE (Notes 1, 2 & 5)

Parameter Symbol	Parameter Description	Test Conditions	Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	10	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	12	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	10	pF

Notes:

1. Typical values are for nominal supply voltages.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X512 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
4. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
5. T_A = 25°C, f = 1 MHz.
6. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns.

   Maximum DC voltage on input and output may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

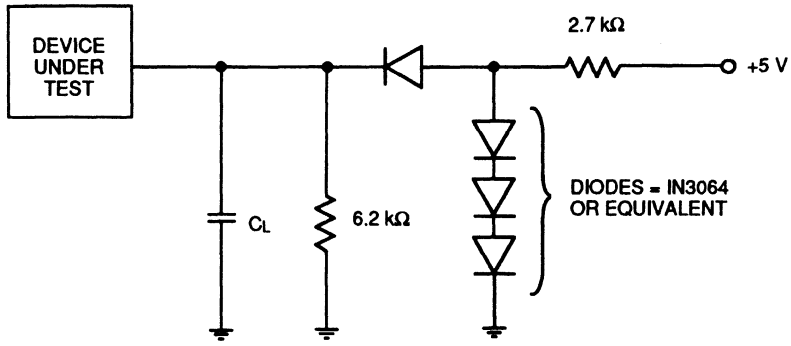
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 2 & 3)

Parameter Symbol		Parameter Description	Test Conditions		-125	-155 -150	-200	-250	Unit
JEDEC	Standard								
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.					ns
				Max.	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.					ns
				Max.	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.					ns
				Max.	50	65	75	100	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 1)	Output Enable HIGH to Output Float		Min.					ns
				Max.	30	30	30	30	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	ns
				Max.					

Notes:

1. This parameter is only sampled and not 100% tested.
2. **Caution:** The Am27X512 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
3. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

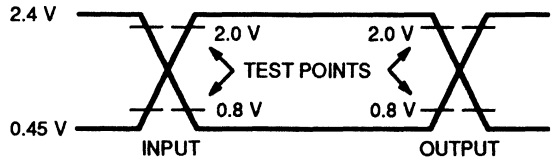
SWITCHING TEST CIRCUIT



10205-004A

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



10205-009A

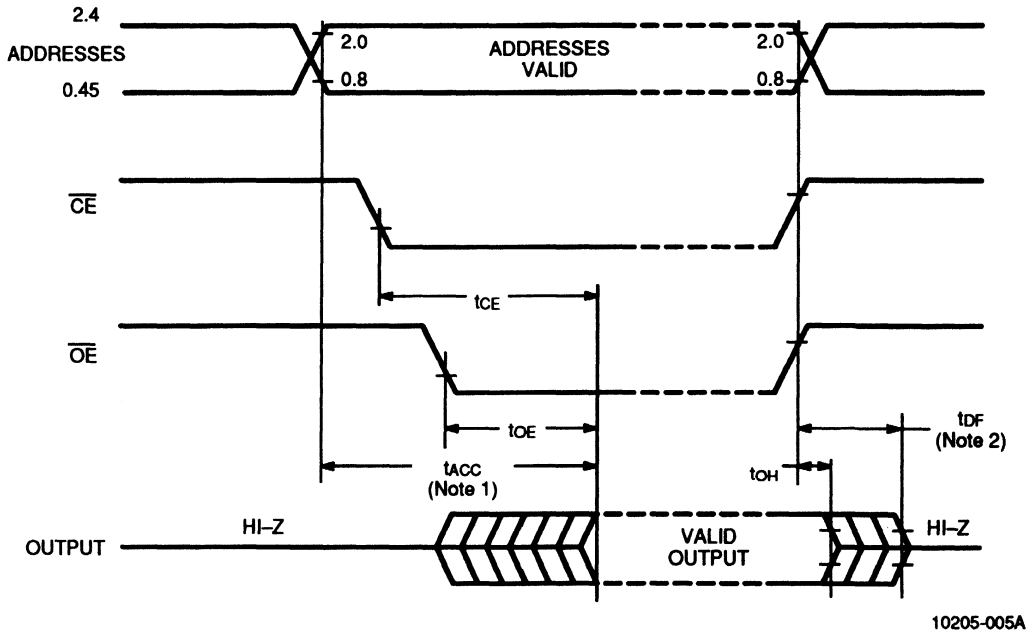
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



10205-005A

Note:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Am27X010

1 Megabit (131,072 x 8-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - Factory optimized programming
  - Fully tested and guaranteed
  - Lower cost
- **As a Mask ROM alternative:**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High noise immunity**
- **High performance CMOS technology**
  - Fast access time—120 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier (PLCC), and in DIE form**
- **Latch-up protected to 100mA from –1 V to Vcc + 1 V**

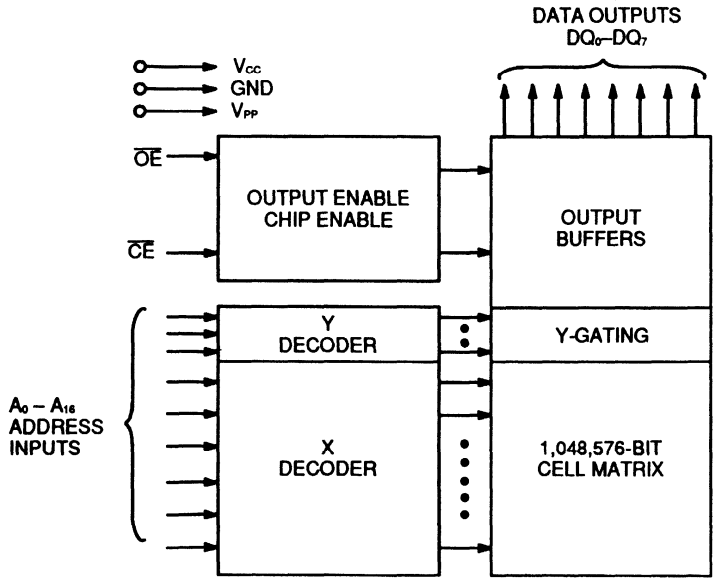
GENERAL DESCRIPTION

The Am27X010 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 131,072 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM Devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 120 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X010 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

BLOCK DIAGRAM



12081B-001

Publication # 12080 Rev. C Amendment/0
Issue Date: March 1991

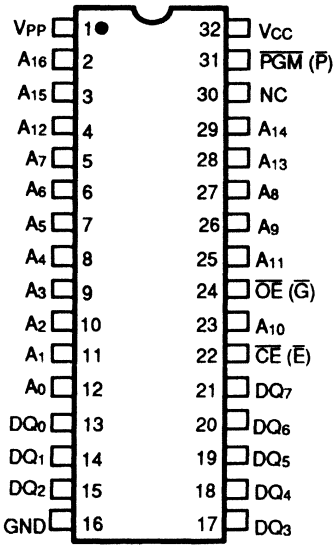
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X010			
Ordering part No:				
±5% VCC Tolerance	-125	-155		
±10% VCC Tolerance	—	-150	-200	-250
Max Access Time (ns)	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	65	75	100

CONNECTION DIAGRAMS

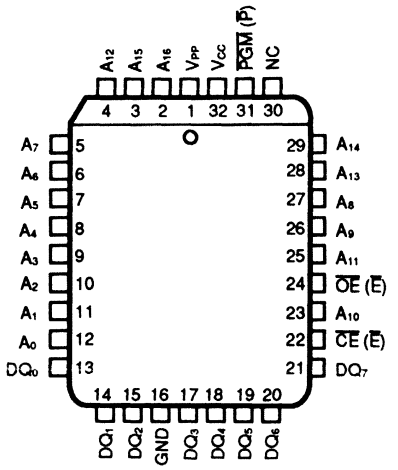
Top View

PLASTIC DIP



12081-002A

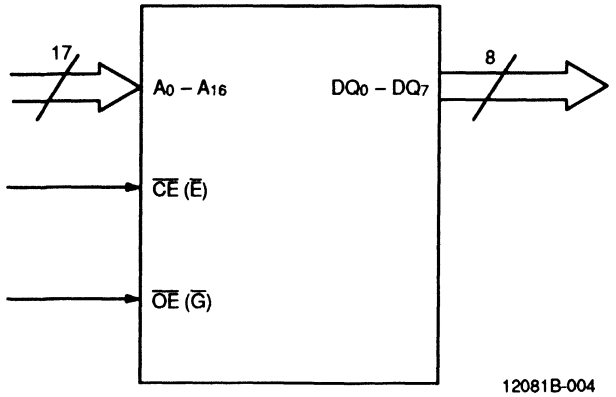
PLCC



12080-009A

Note: 1. JEDEC nomenclature is in parentheses.
2. The 32-Pin DIP to 32-Pin PLCC configuration varies from the JEDEC 28-Pin DIP to 32-Pin PLCC configuration.

LOGIC SYMBOL



12081B-004

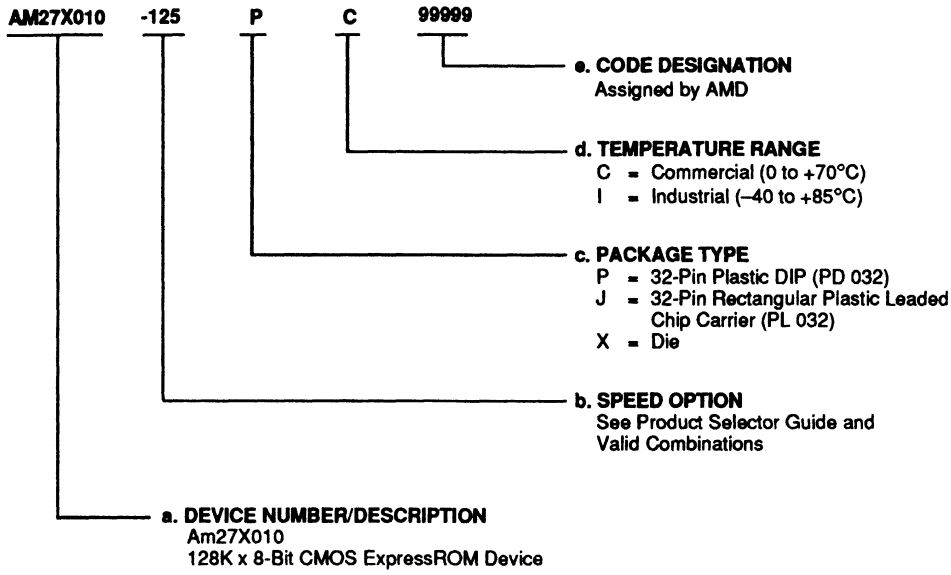
PIN DESCRIPTION

A0 – A16	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0 – DQ7	=	Data Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Enable Input
VPP	=	Vcc Supply Voltage
Vcc	=	Vcc Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation



Valid Combinations	
AM27X010-125 AM27X010-150 AM27X010-155 AM27X010-200 AM27X010-250	PC, JC, XC, PI, JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X010 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X010 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X010 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM Device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	High Z
Standby (TTL)	V_{IH}	X	X	X	High Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	X	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC}	–0.6 to V_{CC} + 0.6 V
V_{CC}	–0.6 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note:
During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to +70°C

Industrial (I) Devices

Case Temperature (T_C)	–40 to +85°C

Supply Read Voltages:

V_{CC} for Am27X010–XX5	+4.75 to +5.25 V
V_{CC} for Am27X010–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
TTL and NMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	Vcc Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	Vcc Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{PP}	Vcc Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA
CMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	Vcc Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	Vcc Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA
I_{PP}	Vcc Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 2, 3 & 7)

Parameter Symbol	Parameter Description	Test Conditions	PD032		PL032		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27X010 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns.
   Maximum DC voltage on input and output may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

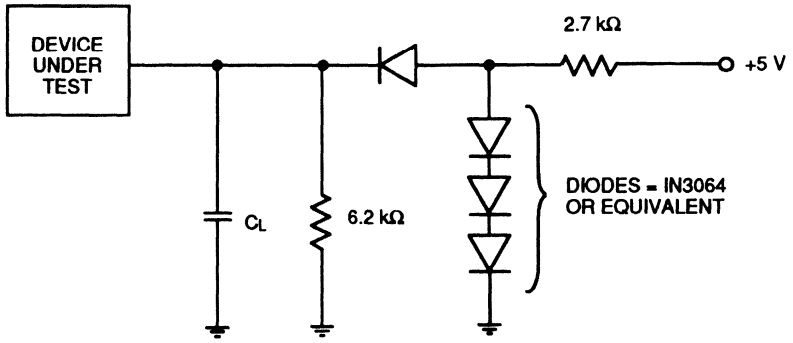
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 & 4)

Parameter Symbol		Parameter Description	Test Conditions		-125	-155 -150	-200	-250	Unit
JEDEC	Standard								
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.					ns
				Max.	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.					ns
				Max.	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.					ns
				Max.	50	65	75	100	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.					ns
				Max.	35	35	40	40	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	ns
				Max.					

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X010 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

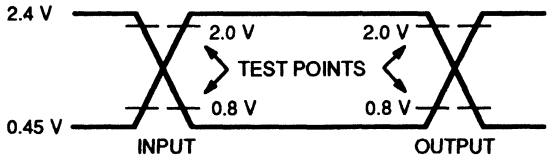
SWITCHING TEST CIRCUIT



10205-004A

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



10205-009A

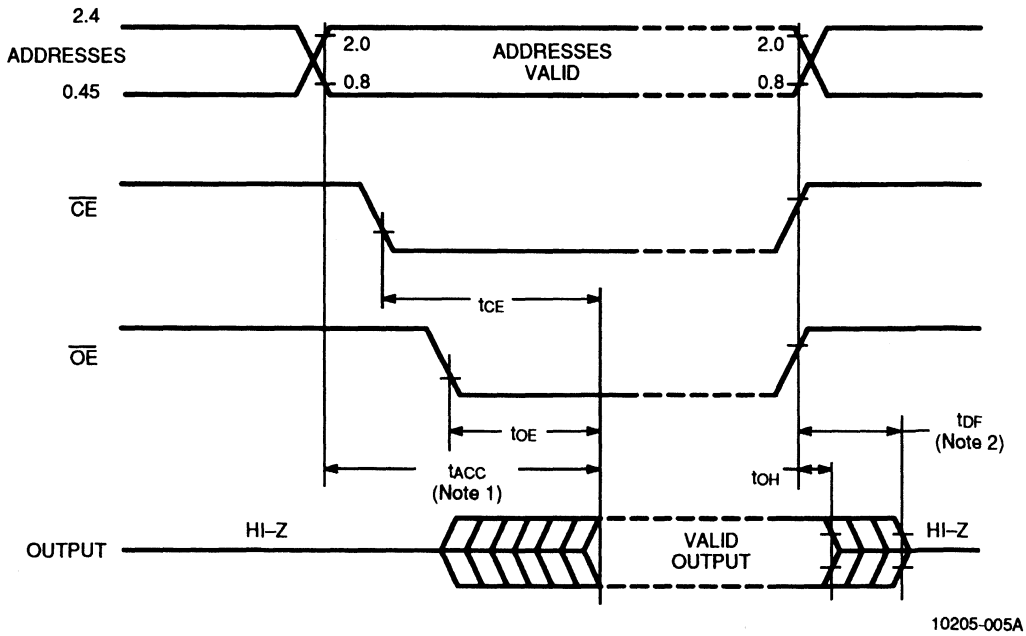
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



10205-005A

Note:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Am27X100

1 Megabit (131,072 x 8-Bit) ROM Compatible CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - Factory optimized programming
  - Fully tested and guaranteed
  - Lower cost
- **As a Mask ROM alternative:**
  - Pinout compatible with ROMs
  - Shorter leadtime
  - Lower volume per code
- **Compatible with EIAJ-approved ROM pinout**
- **High noise immunity**
- **High performance CMOS technology**
  - Fast access time—120 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP, plastic leaded chip carrier (PLCC), and in DIE form**
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**

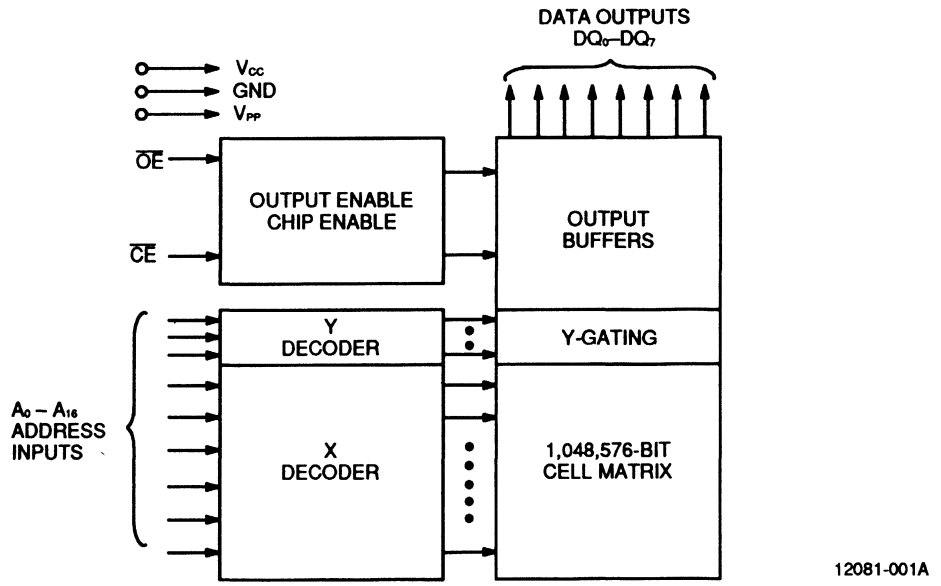
GENERAL DESCRIPTION

The Am27X100 is a wafer-level programmed EPROM with a standard topside for plastic packaging. The 32 pin EIAJ pinout is compatible with 28 pin megabit ROMs. The memory is organized as 131,072 by 8 bits and is available in a plastic DIP package as well as a plastic leaded chip carrier (PLCC). ExpressROM Devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 120 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X100 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 250 µW in standby mode.

BLOCK DIAGRAM



12081-001A

Publication # 12619 Rev. B Amendment/0
Issue Date: March 1991

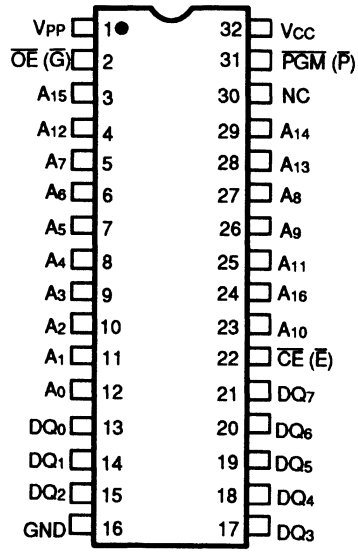
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X100			
Ordering part No: ±5% VCC Tolerance	-125	-155		
±10% VCC Tolerance	—	-150	-200	-250
Max Access Time (ns)	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	65	75	100

CONNECTION DIAGRAMS

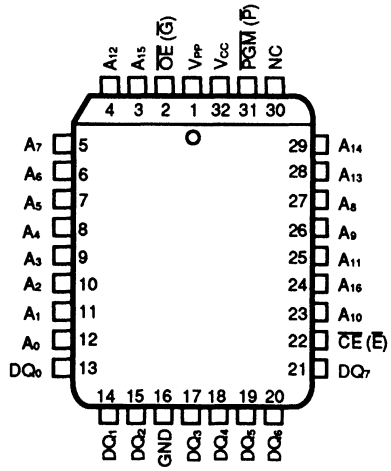
Top View

PLASTIC DIP



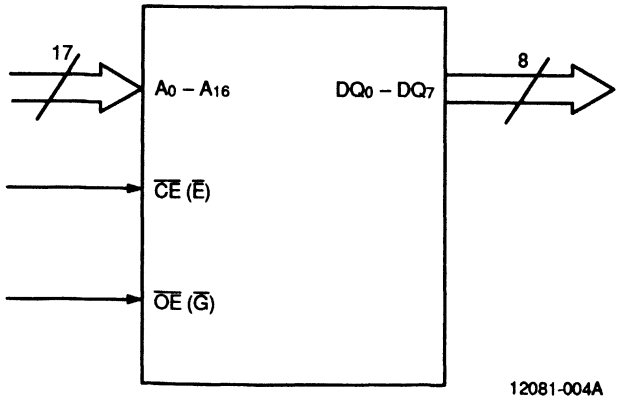
12081-002A

PLCC



Note: 1. JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



12081-004A

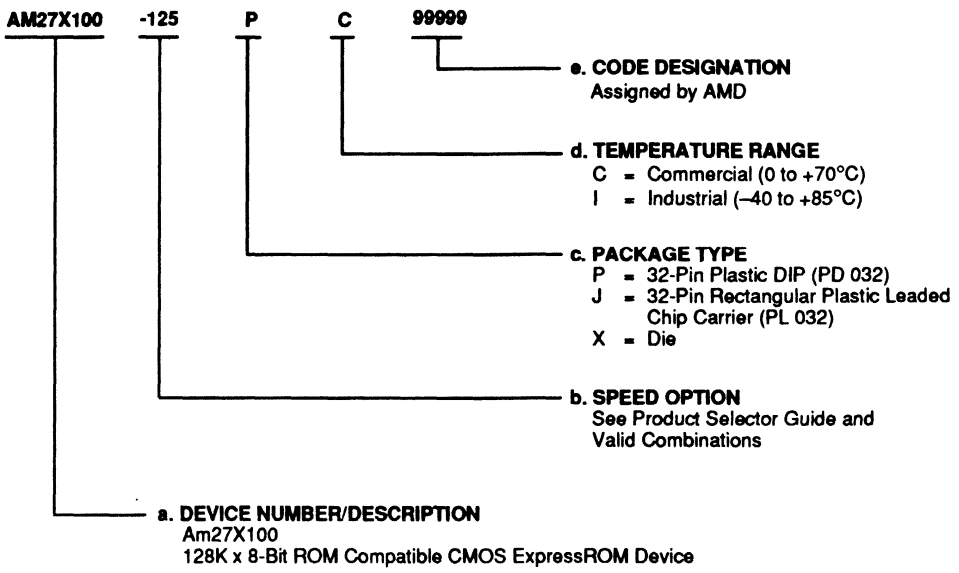
PIN DESCRIPTION

A0 – A16	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0 – DQ7	=	Data Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Enable Input
VPP	=	Vcc Supply Voltage
Vcc	=	Vcc Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation



Valid Combinations	
AM27X100-125	PC, JC, XC, PI, JI
AM27X100-150	
AM27X100-155	
AM27X100-200	
AM27X100-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X100 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X100 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X100 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM Device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	High Z
Standby (TTL)	V_{IH}	X	X	X	High Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC}	–0.6 to V_{CC} + 0.6 V
V_{CC}	–0.6 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note:
During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to +70°C

Industrial (I) Devices

Case Temperature (T_C)	–40 to +85°C

Supply Read Voltages:

V_{CC} for Am27X100–XX5	+4.75 to +5.25 V
V_{CC} for Am27X100–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
TTL and NMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{PP}	V_{CC} Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA
CMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA
I_{PP}	V_{CC} Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 2, 3 & 7)

Parameter Symbol	Parameter Description	Test Conditions	PD 032 Typ.	PD 032 Max.	Unit
C_{IN}	Address Input Capacitance	V_{IN} = 0 V	12	14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	14	17	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27X100 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns.
   Maximum DC voltage on input and output may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

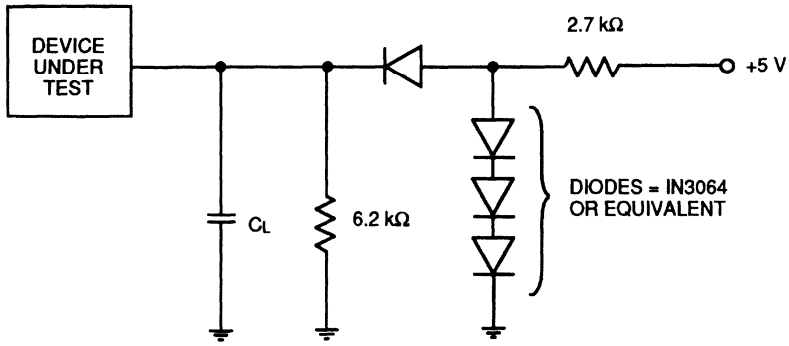
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 & 4)

Parameter Symbol JEDEC	Parameter Symbol Standard	Parameter Description	Test Conditions		-125	-155 -150	-200	-250	Unit
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.					ns
				Max.	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.					ns
				Max.	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.					ns
				Max.	50	65	75	100	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.					ns
				Max.	35	35	40	40	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	ns
				Max.					

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X100 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

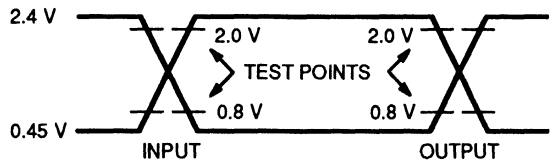
SWITCHING TEST CIRCUIT



10205-004A

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



10205-009A

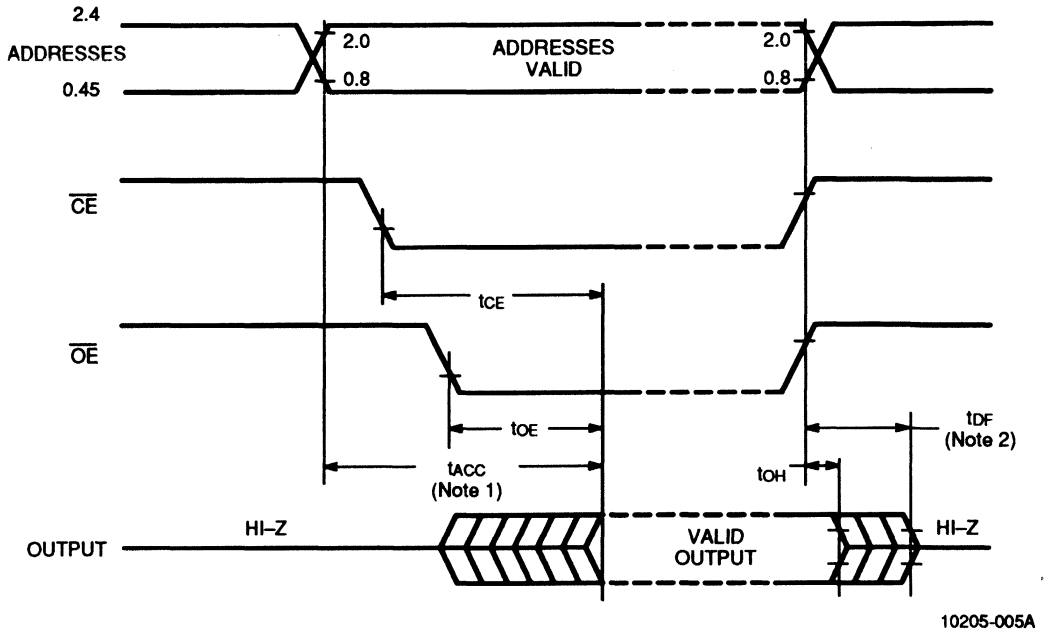
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORM



10205-005A

Note:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Am27X1024

1 Megabit (65,536 x 16-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - Factory optimized programming
  - Fully tested and guaranteed
  - Lower cost
- **As a Mask ROM alternative:**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High noise immunity**
- **High performance CMOS technology**
  - Fast access time — 170 ns
  - Low power dissipation
    200 µA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier (PLCC), and in DIE form**
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**

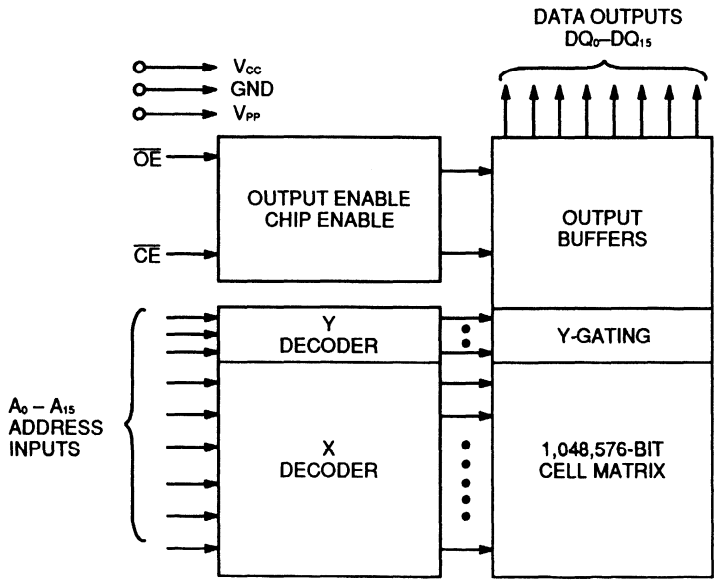
GENERAL DESCRIPTION

The Am27X1024 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 65,536 by 16 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM Devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 170 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X1024 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 350 µW in standby mode.

BLOCK DIAGRAM



12081B-001

Publication # 12079 Rev. C Amendment/0
Issue Date: March 1991

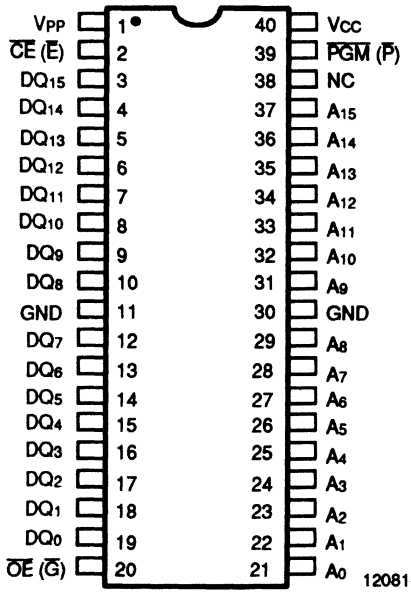
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X1024		
Ordering part No: ±5% VCC Tolerance	-175	-205	
±10% VCC Tolerance	—	-200	-250
Max Access Time (ns)	170	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	170	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	65	75	100

CONNECTION DIAGRAMS

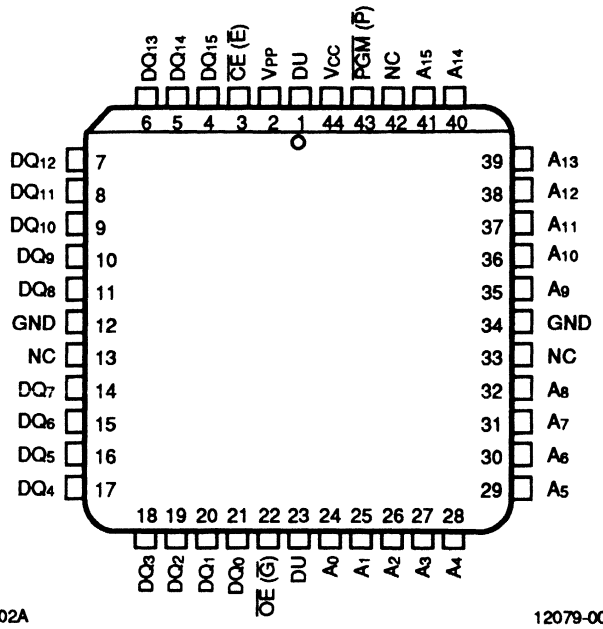
Top View

PLASTIC DIP



12081-002A

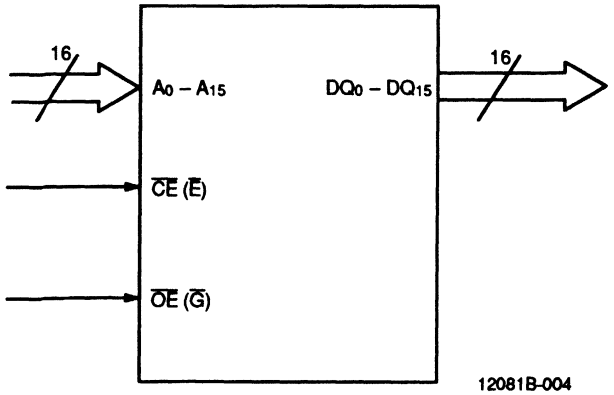
PLCC



12079-009A

Note: JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



12081B-004

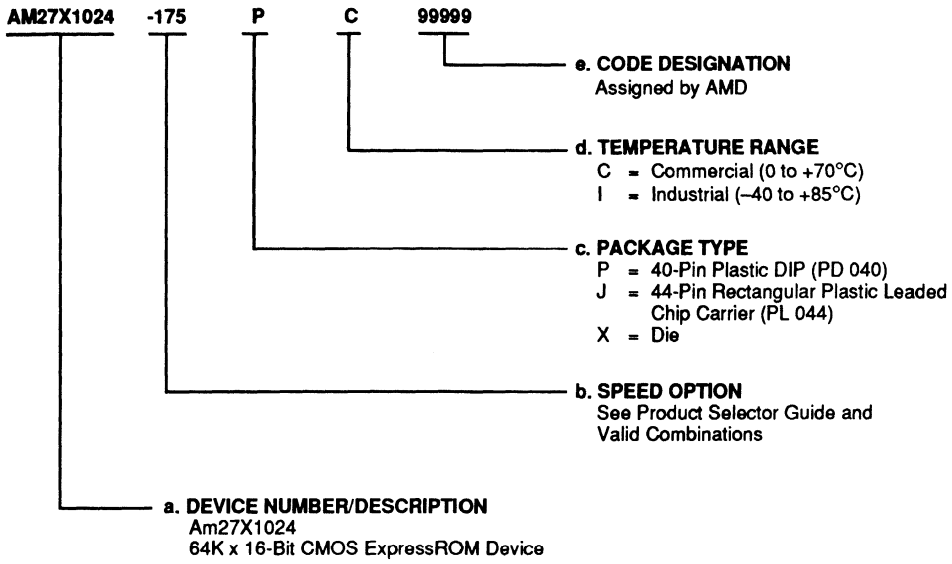
PIN DESCRIPTION

A0 – A15	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0 – DQ15	=	Data Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Enable Input
VPP	=	Vcc Supply Voltage
Vcc	=	Vcc Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation



Valid Combinations	
AM27X1024-175 AM27X1024-200 AM27X1024-205 AM27X1024-250	PC, JC, XC, PI, JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X1024 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X1024 has a CMOS standby mode which reduces the maximum V_{CC} current to 200 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X1024 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM Device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	High Z
Standby (TTL)	V_{IH}	X	X	X	High Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC}	–0.6 to V_{CC} + 0.6 V
V_{CC}	–0.6 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note:
During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to +70°C

Industrial (I) Devices

Case Temperature (T_C)	–40 to +85°C

Supply Read Voltages:

V_{CC} for Am27X1024–XX5	+4.75 to +5.25 V
V_{CC} for Am27X1024–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
TTL and NMOS					
V_{OH}	Output HIGH Voltage	I_{OH} = – 400 µA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		– 0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}		5	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)		50	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}		1	mA
I_{PP}	V_{CC} Supply Current (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}		100	µA
CMOS					
V_{OH}	Output HIGH Voltage	I_{OH} = – 400 µA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA		0.45	V
V_{IH}	Input HIGH Voltage		V_{CC} – 0.3	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		– 0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}		5	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)		50	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V		200	µA
I_{PP}	V_{CC} Supply Current (Note 6)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}		100	µA

CAPACITANCE (Notes 2, 3 & 7)

Parameter Symbol	Parameter Description	Test Conditions	PD040 Typ.	PD040 Max.	PL044 Typ.	PL044 Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0 V	6	10	6	9	pF
C_{IN2}	$\overline{OE}$ Input Capacitance	V_{IN} = 0 V	10	12	7	9	pF
C_{IN3}	$\overline{CE}$ Input Capacitance	V_{IN} = 0 V	10	12	7	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	14	6	9	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27X1024 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns.
   Maximum DC voltage on input and output may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

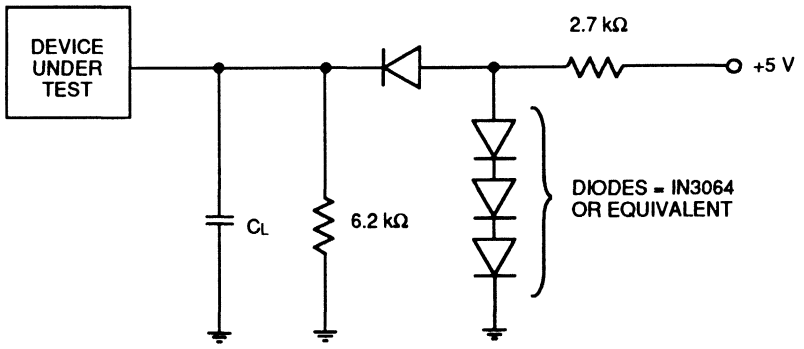
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 & 4)

Parameter Symbol JEDEC	Parameter Symbol Standard	Parameter Description	Test Conditions		-175	-205 -200	-250	Unit
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.				ns
				Max.	170	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.				ns
				Max.	170	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.				ns
				Max.	65	75	100	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.				ns
				Max.	55	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	ns
				Max.				

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X1024 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

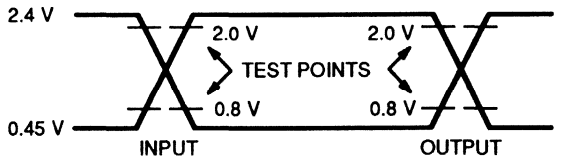
SWITCHING TEST CIRCUIT



10205-004A

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



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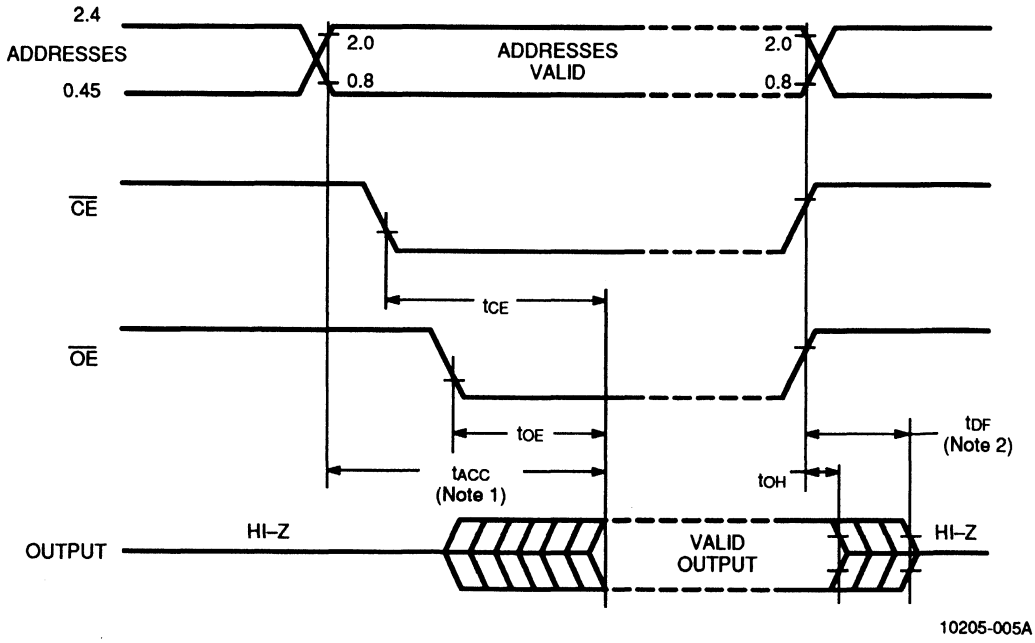
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



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Note:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Am27X020

2 Megabit (262,144 x 8-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - Factory optimized programming
  - Fully tested and guaranteed
  - Lower cost
- **As a Mask ROM alternative:**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High noise immunity**
- **High performance CMOS technology**
  - Fast access time—150 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier (PLCC), and in DIE form**
- **Latch-up protected to 100mA from –1 V to Vcc + 1 V**

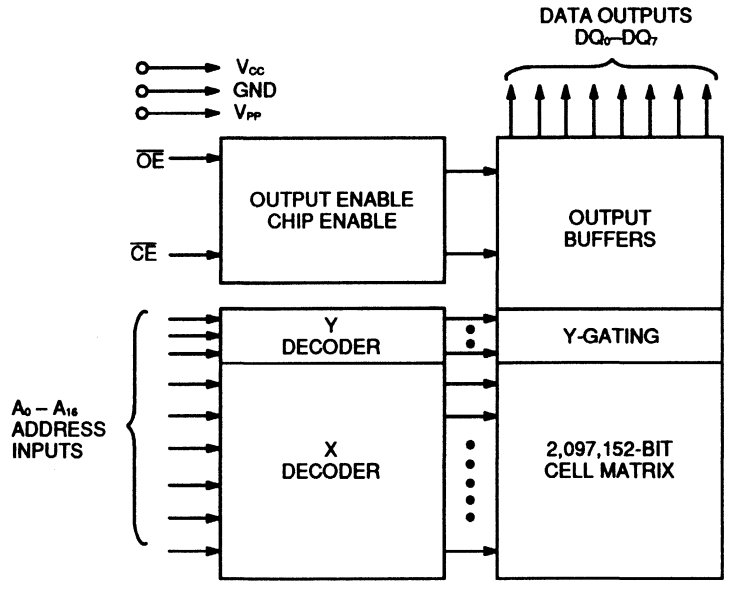
GENERAL DESCRIPTION

The Am27X020 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 262,144 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM Devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 150 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X020 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



12081B-001

Publication # 15652 Rev. A Amendment/0
Issue Date: March 1991

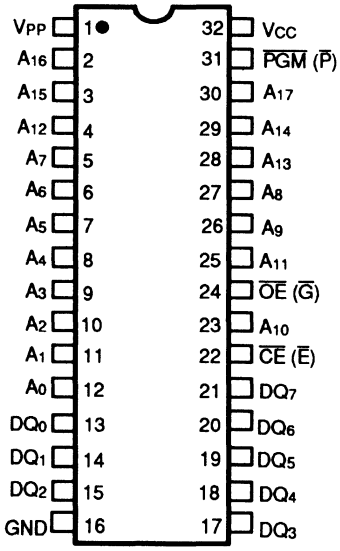
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X020		
Ordering part No:			
±5% VCC Tolerance	-155	-205	
±10% VCC Tolerance	—	-200	-250
Max Access Time (ns)	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	65	75	100

CONNECTION DIAGRAMS

Top View

PLASTIC DIP



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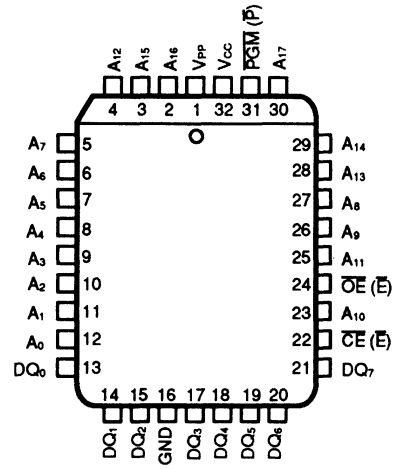
PLCC



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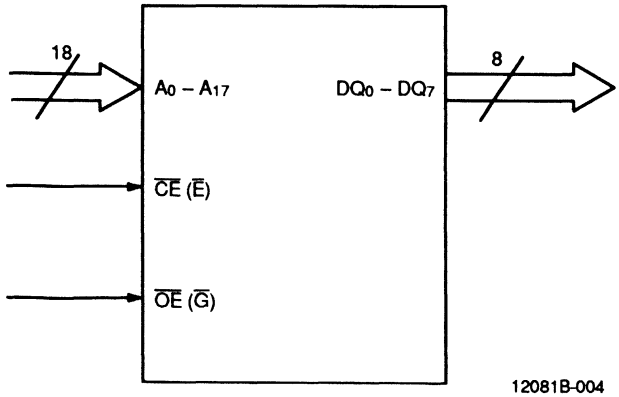
Note: 1. JEDEC nomenclature is in parentheses.
2. The 32-Pin DIP to 32-Pin PLCC configuration varies from the JEDEC 28-Pin DIP to 32-Pin PLCC configuration.

LOGIC SYMBOL



12081B-004

PIN DESCRIPTION

A0 – A17	= Address Inputs
$\overline{CE}$ ($\overline{E}$)	= Chip Enable Input
DQ0 – DQ7	= Data Outputs
$\overline{OE}$ ($\overline{G}$)	= Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	= Enable Input
VPP	= Vcc Supply Voltage
Vcc	= Vcc Supply Voltage
GND	= Ground
NC	= No Internal Connection
DU	= No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation

AM27X020 -155 P C 99999

e. CODE DESIGNATION
Assigned by AMD

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
I = Industrial (–40 to +85°C)

c. PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
X = Die

b. SPEED OPTION
See Product Selector Guide and Valid Combinations

a. DEVICE NUMBER/DESCRIPTION
Am27X020
256K x 8-Bit CMOS ExpressROM Device

Valid Combinations	
AM27X020-155 AM27X020-200 AM27X020-205 AM27X020-250	PC, JC, XC, PI, JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X020 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X020 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X020 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM Device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	High Z
Standby (TTL)	V_{IH}	X	X	X	High Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	X	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC}	–0.6 to V_{CC} + 0.6 V
V_{CC}	–0.6 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note:
During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to +70°C

Industrial (I) Devices

Case Temperature (T_C)	–40 to +85°C

Supply Read Voltages:

V_{CC} for Am27X020–XX5	+4.75 to +5.25 V
V_{CC} for Am27X020–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
TTL and NMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	Vcc Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	Vcc Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{PP}	Vcc Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA
CMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	$V_{CC} - 0.8$		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		0.7 V_{CC}	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	Vcc Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		30	mA
I_{CC2}	Vcc Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA
I_{PP}	Vcc Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 2, 3 & 7)

Parameter Symbol	Parameter Description	Test Conditions	PD032		PL032		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27X020 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns.
   Maximum DC voltage on input and output may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

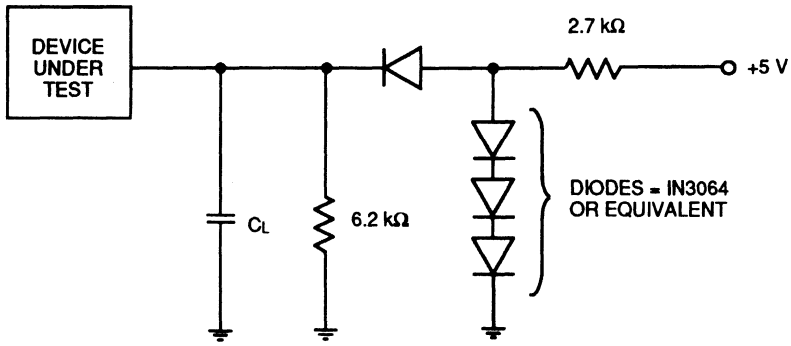
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 & 4)

Parameter Symbol		Parameter Description	Test Conditions		-155	-205 -200	-250	Unit
JEDEC	Standard							
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.				ns
				Max.	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.				ns
				Max.	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.				ns
				Max.	65	75	100	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.				ns
				Max.	50	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	ns
				Max.				

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X020 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

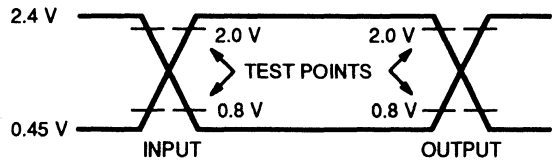
SWITCHING TEST CIRCUIT



10205-004A

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



10205-009A

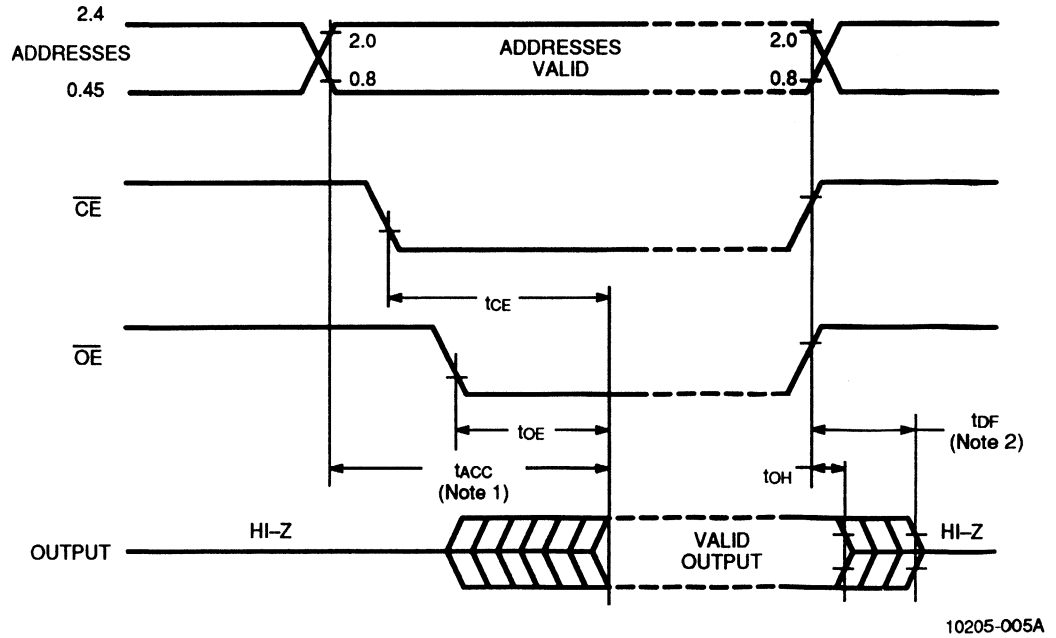
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



10205-005A

Note:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Am27X2048

2 Megabit (131,072 x 16-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - Factory optimized programming
  - Fully tested and guaranteed
  - Lower cost
- **As a Mask ROM alternative:**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High noise immunity**
- **High performance CMOS technology**
  - Fast access time — 150 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier (PLCC), and in DIE form**
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**

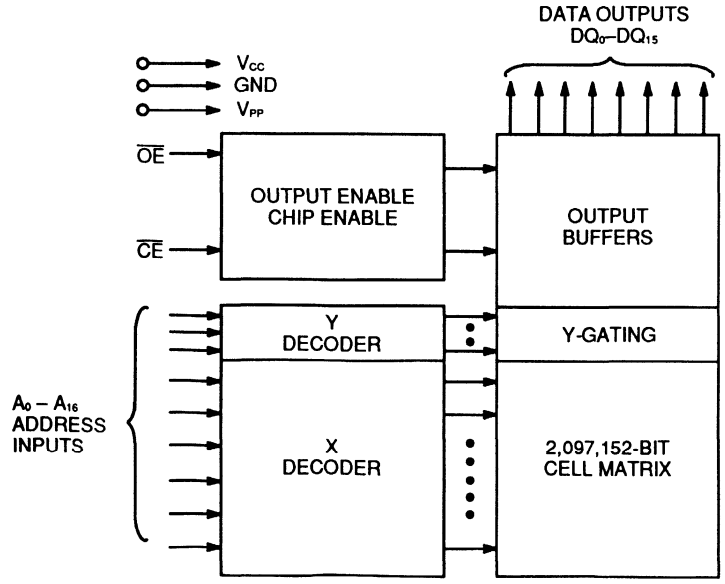
GENERAL DESCRIPTION

The Am27X2048 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 131,072 by 16 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM Devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 150 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X2048 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 125 µW in standby mode.

BLOCK DIAGRAM



12081B-001

Publication # 15653 Rev. A Amendment/0
Issue Date: March 1991

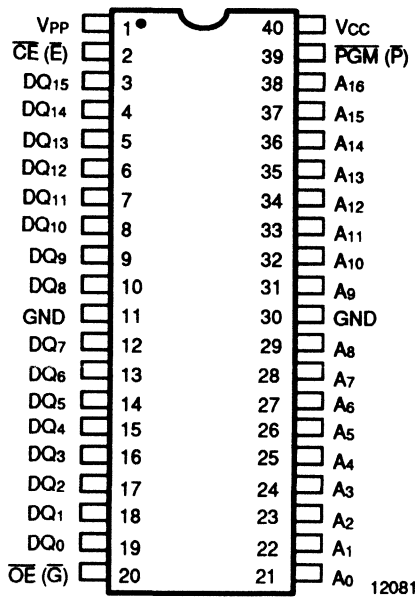
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X2048		
Ordering part No: ±5% VCC Tolerance	-155	-205	
±10% VCC Tolerance	—	-200	-250
Max Access Time (ns)	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	65	75	100

CONNECTION DIAGRAMS

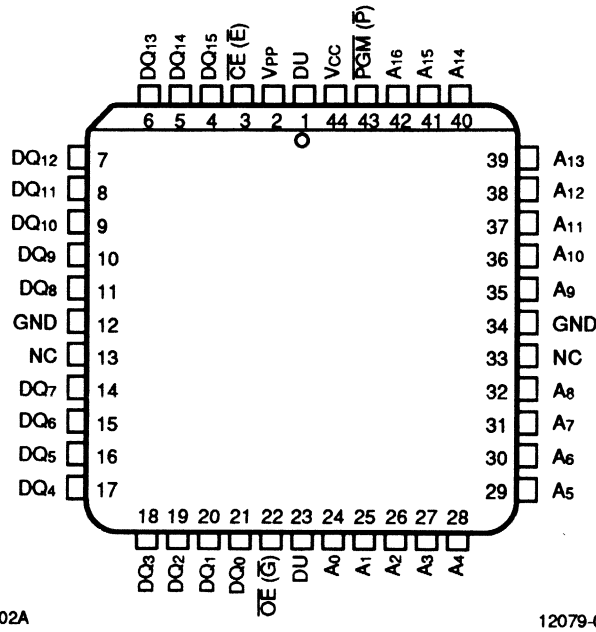
Top View

PLASTIC DIP



12081-002A

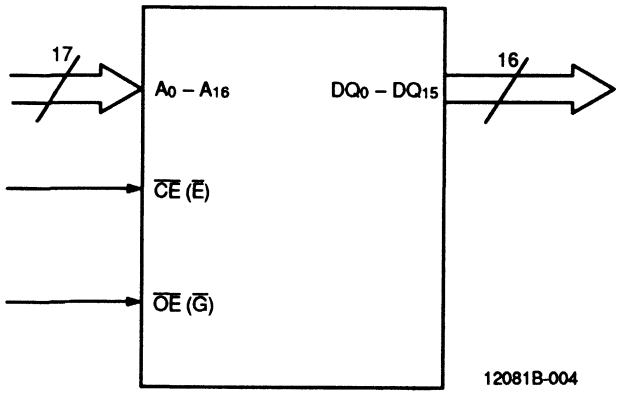
PLCC



12079-009A

Note: JEDEC nomenclature is in parentheses.

LOGIC SYMBOL



12081B-004

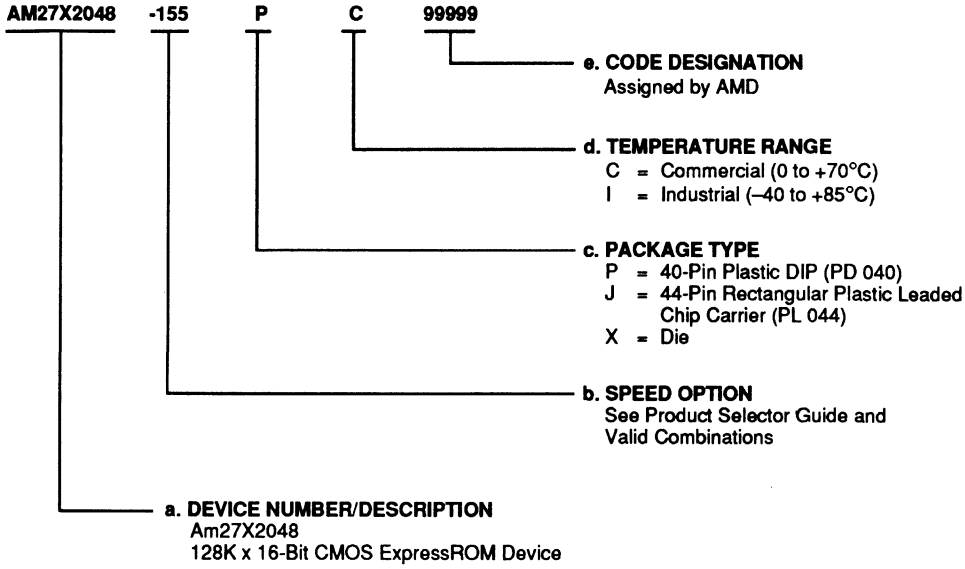
PIN DESCRIPTION

$A_0 - A_{16}$	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
$DQ_0 - DQ_{15}$	=	Data Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
$\overline{PGM}$ ($\overline{P}$)	=	Enable Input
V_{PP}	=	Vcc Supply Voltage
Vcc	=	Vcc Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation



Valid Combinations	
AM27X2048-155 AM27X2048-200 AM27X2048-205 AM27X2048-250	PC, JC, XC, PI, JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X2048 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X2048 has a CMOS standby mode which reduces the maximum V_{CC} current to 200 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27X2048 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM Device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	High Z
Standby (TTL)	V_{IH}	X	X	X	High Z
Standby (CMOS)	V_{CC} ± 0.3 V	X	X	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC}	–0.6 to V_{CC} + 0.6 V
V_{CC}	–0.6 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note:
During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to +70°C

Industrial (I) Devices

Case Temperature (T_C)	–40 to +85°C

Supply Read Voltages:

V_{CC} for Am27X2048–XX5	+4.75 to +5.25 V
V_{CC} for Am27X2048–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
TTL and NMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		50	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{PP}	V_{CC} Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA
CMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	$V_{CC} - 0.8$		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		0.7 V_{CC}	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		50	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA
I_{PP}	V_{CC} Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 2, 3 & 7)

Parameter Symbol	Parameter Description	Test Conditions	PD040		PL044		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27X2048 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns.
   Maximum DC voltage on input and output may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

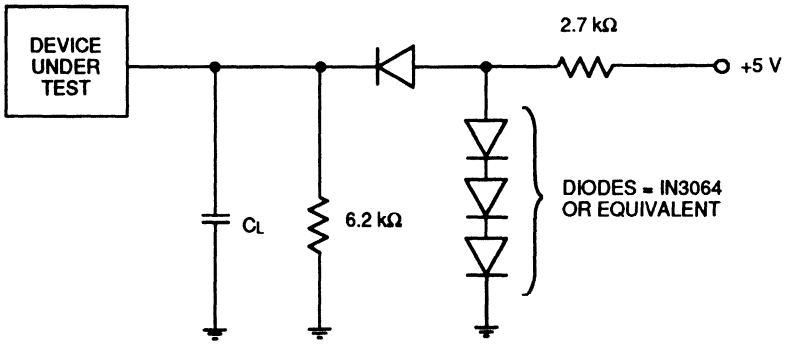
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 & 4)

Parameter Symbol		Parameter Description	Test Conditions		-155	-205 -200	-250	Unit
JEDEC	Standard							
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.				ns
				Max.	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.				ns
				Max.	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.				ns
				Max.	65	75	100	
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.				ns
				Max.	50	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	ns
				Max.				

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X2048 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

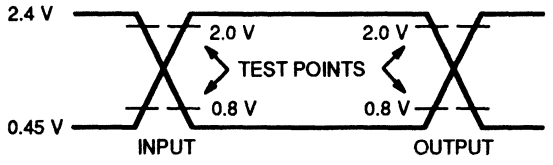
SWITCHING TEST CIRCUIT



10205-004A

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



10205-009A

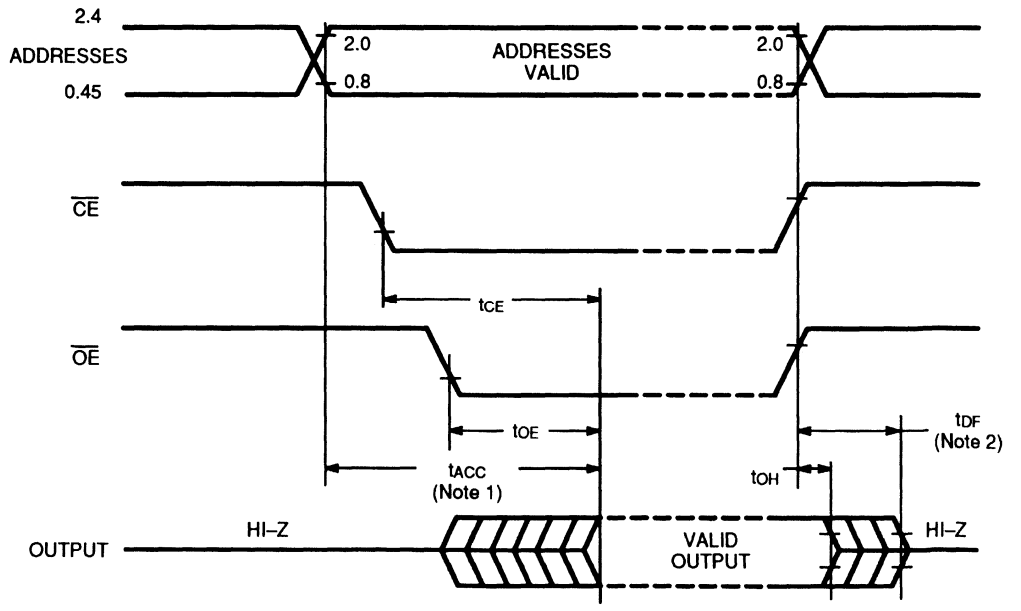
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



10205-005A

Note:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Am27X040

4 Megabit (524,288 x 8-Bit) CMOS ExpressROM™ Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - Factory optimized programming
  - Fully tested and guaranteed
  - Lower cost
- **As a Mask ROM alternative:**
  - Shorter leadtime
  - Lower volume per code
- **Compatible with JEDEC-approved EPROM pinout**
- **High noise immunity**
- **High performance CMOS technology**
  - Fast access time—120 ns
  - Low power dissipation
    100 µA maximum standby current
- **Available in plastic DIP and plastic leaded chip carrier (PLCC), and in DIE form**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**

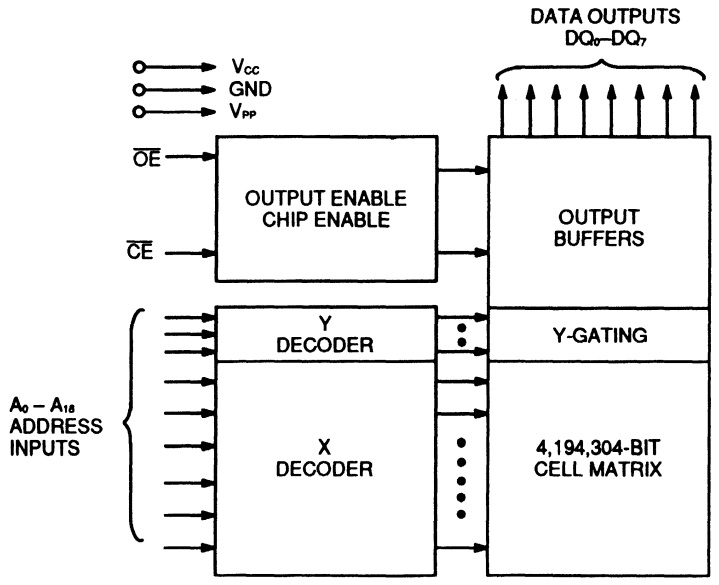
GENERAL DESCRIPTION

The Am27X040 is a wafer-level programmed EPROM with a standard topside for plastic packaging. It is organized as 524,288 by 8 bits and is available in plastic DIP as well as plastic leaded chip carrier (PLCC) packages. ExpressROM Devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Access times as fast as 120 ns allow operation with high-performance microprocessors with reduced WAIT states. The Am27X040 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



12081B-001

Publication # 15654 Rev. A Amendment/0
Issue Date: March 1991

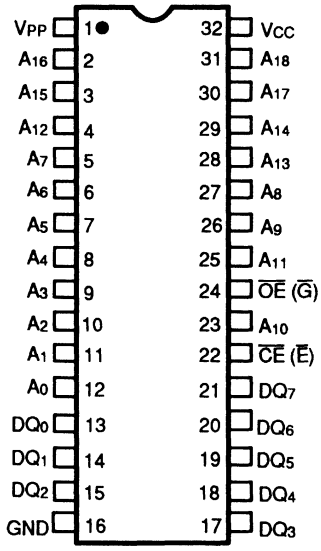
PRODUCT SELECTOR GUIDE

Family Part No.	Am27X040			
Ordering part No:				
±5% VCC Tolerance	-125	-155		
±10% VCC Tolerance	—	-150	-200	-250
Max Access Time (ns)	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	50	65	75	100

CONNECTION DIAGRAMS

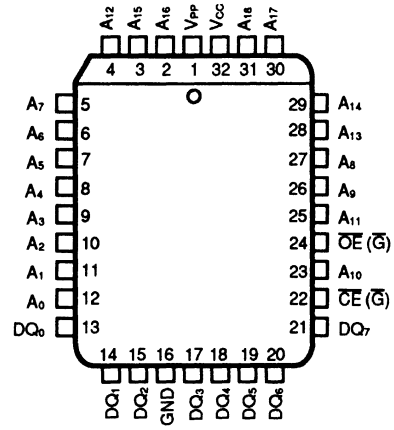
Top View

PLASTIC DIP



12081-002A

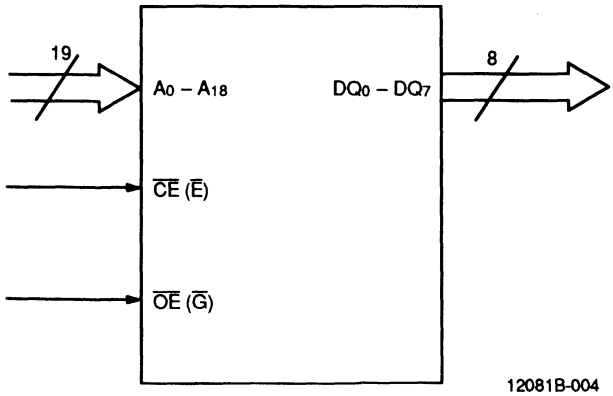
PLCC



12080-009A

Note: 1. JEDEC nomenclature is in parentheses.
2. The 32-Pin DIP to 32-Pin PLCC configuration varies from the JEDEC 28-Pin DIP to 32-Pin PLCC configuration.

LOGIC SYMBOL



12081B-004

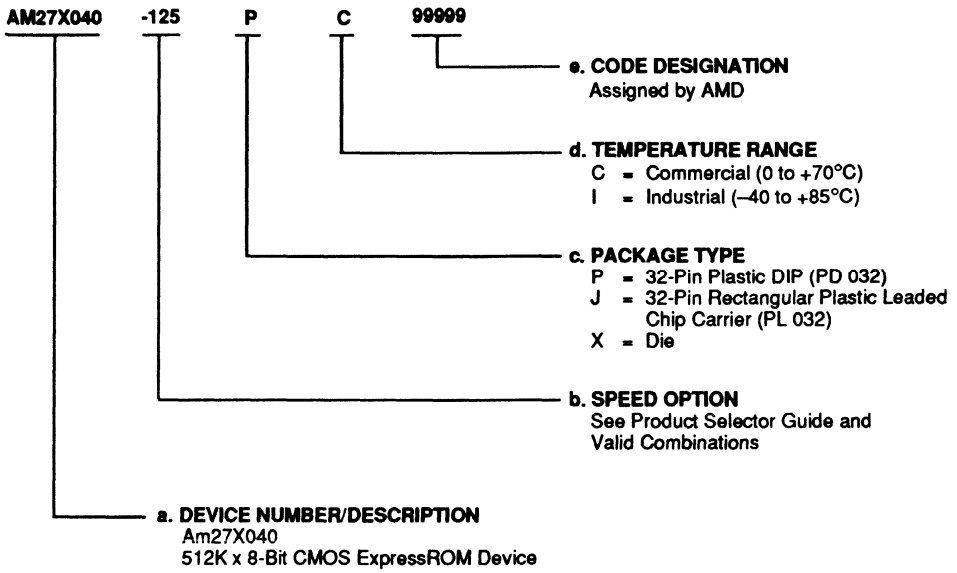
PIN DESCRIPTION

A0 – A18	=	Address Inputs
$\overline{CE}$ ($\overline{E}$)	=	Chip Enable Input
DQ0 – DQ7	=	Data Outputs
$\overline{OE}$ ($\overline{G}$)	=	Output Enable Input
VPP	=	Vcc Supply Voltage
Vcc	=	Vcc Supply Voltage
GND	=	Ground
NC	=	No Internal Connection
DU	=	No External Connection (Do Not Use)

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Code Designation



Valid Combinations	
AM27X040-125 AM27X040-150 AM27X040-155 AM27X040-200 AM27X040-250	PC, JC, XC, PI, JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

The Am27X040 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27X040 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE}$ is at $V_{CC} \pm 0.3$ V. The Am27X040 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on ExpressROM Device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Mode Select Table

Pins / Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	High Z
Standby (TTL)	V_{IH}	X	X	High Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	High Z

Note: X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +125°C
Ambient Temperature with Power Applied	–55 to +125°C
Voltage with Respect to Ground:	
All pins except V_{CC}	–0.6 to V_{CC} + 0.6 V
V_{CC}	–0.6 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note:
During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and output may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to +70°C

Industrial (I) Devices

Case Temperature (T_C)	–40 to +85°C

Supply Read Voltages:

V_{CC} for Am27X040–XX5	+4.75 to +5.25 V
V_{CC} for Am27X040–XX0	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 4, 5 & 8)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
TTL and NMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		40	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1.0	mA
I_{PP}	V_{CC} Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA
CMOS					
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\ \mu A$	$V_{CC} - 0.8$		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA		0.45	V
V_{IH}	Input HIGH Voltage		0.7 V_{CC}	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage		−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to $+V_{CC}$		1.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to $+V_{CC}$		5	µA
I_{CC1}	V_{CC} Active Current (Note 5)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA (Open Outputs)		40	mA
I_{CC2}	V_{CC} Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V		100	µA
I_{PP}	V_{CC} Supply Current (Note 6)	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$		100	µA

CAPACITANCE (Notes 2, 3 & 7)

Parameter Symbol	Parameter Description	Test Conditions	PD032		PL032		Unit
			Typ.	Max.	Typ.	Max.	
C_{IN}	Input Capacitance	V_{IN} = 0 V	10	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	12	15	9	12	pF

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. **Caution:** The Am27X040 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
5. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
6. Maximum active power usage is the sum of I_{CC} and I_{PP}.
7. T_A = 25°C, f = 1 MHz.
8. During transitions, the input may overshoot GND to –2.0 V for periods of up to 20 ns.
   Maximum DC voltage on input and output may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.

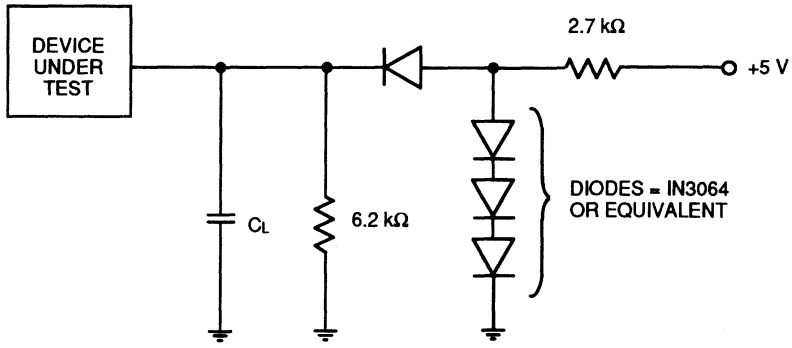
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 & 4)

Parameter Symbol		Parameter Description	Test Conditions		-125	-155 -150	-200	-250	Unit
JEDEC	Standard								
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Min.					ns
				Max.	120	150	200	250	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Min.					ns
				Max.	120	150	200	250	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}	Min.					ns
				Max.	50	65	75	100	
t_{EHQZ}, t_{GHQZ}	t_{DF} (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min.					ns
				Max.	40	50	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min.	0	0	0	0	ns
				Max.					

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. **Caution:** The Am27X040 must not be removed from, or inserted into, a socket or board when V_{CC} is applied.
4. Output Load: 1 TTL gate and C_L = 100 pF
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.45 to 2.4 V
   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V

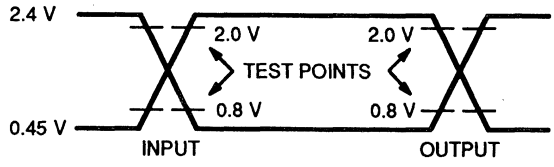
SWITCHING TEST CIRCUIT



10205-004A

C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



10205-009A

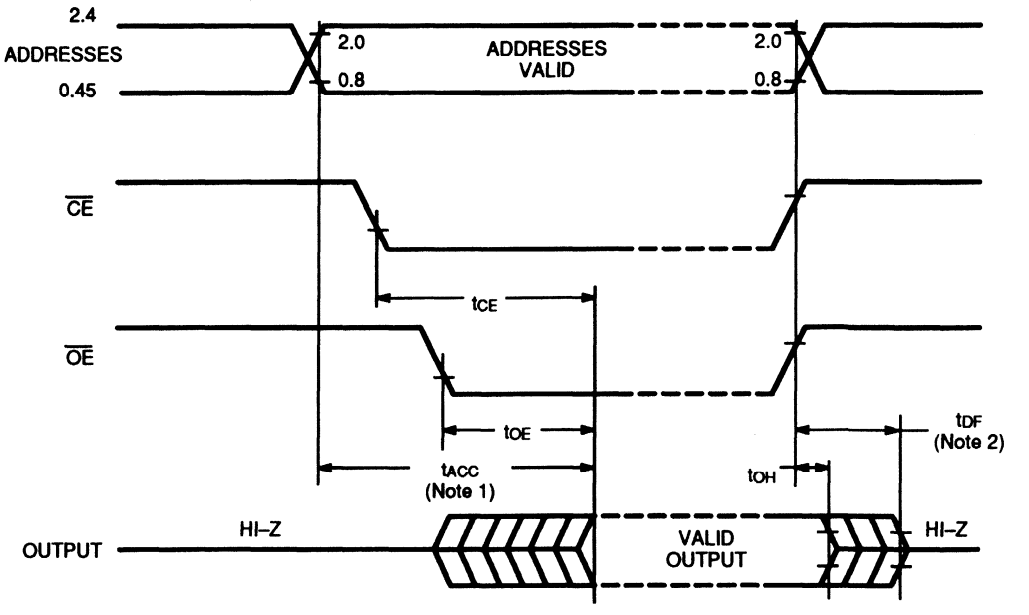
AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0". Input pulse rise and fall times are ≤ 20ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS



10205-005A

Note:

1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

SECTION 4
Flash Memories

An Introduction to Flash Memory

WHAT IS FLASH MEMORY?

Flash memories are the most cost effective non-volatile alternative for high density memory applications that require in-system reprogramming.

Flash memory is born out of a marriage of EPROM and E²PROM technology. Accordingly, Flash memories incorporate the best characteristics of both devices. Flash memories are erased electrically just like E²PROMs. However, Flash memories erase the entire chip at once. This is similar to UV EPROM. Unlike E²PROM, Flash memories do not allow data to be changed on a byte by byte basis. In addition, the Am28Fxxx family of Flash memories uses a separate 12.0 V ±5% programming power supply for both program and erase operations. Absolute write protection is provided when the 12.0 V supply is disabled.

The Am28F010 one Megabit Flash memory can be completely reprogrammed in less than five seconds. Reprogramming includes both the erase and programming operations. This is even faster than a standard E²PROM. In addition, Flash devices eliminate the need for expensive windowed packages, unplugging devices from sockets during code changes, and the 15–20 minutes required for EPROM erasure using ultraviolet light. Since Flash memories are available in plastic packages they are ideal for todays automatic manufacturing lines.

Table One compares the basic features of U.V. EPROM, Flash memories, and E²PROMs.

Table 1

Parameter	UV EPROM	Flash	E²PROM
Erase	UV Chip Erase	Electrical Chip Erase	Electricl Byte Erase
Program	Per Byte	Per Byte	Per Byte
Program Voltage	12.5 V	12.0 V	5.0 V
Programming Method	External Programmer	In-system	In-system
Reprogramming Time (1 Megabit)	15 – 20 Minutes	5 Seconds	10 Seconds

Where Will Flash Memories Be Used?

Flash memories can be used in a wide variety of applications that today are implemented with EPROM, E²PROM, SRAM & Battery, or DRAM & Disk memory systems.

Why Is Flash Memory Cost Effective?

In order to answer this question, the total cost of reprogramming a non-volatile memory system must be considered. There are two components of the cost structure associated

with in-system reprogramming. They are the device cost and the cost of updating memory contents in-system.

The following sections illustrate the advantage of AMD's Flash memory family versus today's alternative non-volatile memories.

12.0 V Flash vs. UV EPROM

Although the current device cost of Flash memories is greater than UV EPROM, soon they will be priced at only a multiple of 1.2 times UV EPROM. The cost savings of performing in-system reprogramming with Flash memories greatly outweighs any device level cost advantage of UV EPROM. The cost savings of a Flash memory system is greatly magnified if in-system updates are repeatedly performed. The key difference as shown in table 2 is in the cost of updating memory contents.

When the code of a UV EPROM is updated the device must be removed from a socket and either erased for 15–20 minutes, reprogrammed, and then replaced, or just replaced with an entirely new device containing the updated code. This method of updating memory contents is extremely labor intensive wherever it is performed, at the prototype stage, on the manufacturing line, or especially if it is required when a system is in the field. The reoccuring cost of a service call today exceeds $150. Logistics of implementing manual code changes are complicated if they are to be transparent to the system user. The down time associated with replacing EPROMs is reflected in the end user's loss of productivity.

In addition, when system disassembly occurs in the field to replace EPROM based code storage it impacts the overall system in two ways. First, system design may compromise the most efficient use of board layout space. The placement of the EPROM device and its socket is dictated by ease of access and replacement when the system is disassembled. Second, whenever systems are disassembled the integrity of its reliability as shipped from the factory shipped may be jeopardized. Frequently, system disassembly causes damage to boards and components. In addition, system recalibration may be required after reassembly.

Flash memories offer a superior solution. Reprogramming memory contents can be conveniently accomplished electrically in the resident system. Typically it takes only one second to erase an entire Flash memory device and only seconds to program the entire array. Memory contents may be updated in a number of ways. Reprogramming can be accomplished remotely via the communication abilities of the target system such as modem, Integrated Services Digital Networks (ISDN), or if it is part of a networked system. Updates may also be performed using existing disk drive capability. The updated code may also be distributed via floppy disks and downloaded with just a few simple strokes on the keypad.

12.0 V Flash vs. E^2PROM, 5.0 V – only Flash, and SRAM & Battery

The cost of updating memory contents for each of these alternatives is essentially equivalent. Again, existing communication links can be used. A nominal cost is assigned for this procedure as listed in table 2. In this comparison the primary advantage of AMD's Flash solution is in the device cost. AMD's Flash memories will continue to parallel the density of UV EPROMs while costing only slightly more than them. This is due to the use of our EPROM-like single transistor memory cell. Because these other devices use multiple transistor memory cells, they will be hard pressed to match the future increases in device density and the inherent cost-per-bit advantage of 12.0 V Flash memories.

Since at least 60% of a memory chip is comprised of the actual memory array, any alternative to the single transistor memory cell will suffer from limits of increasing chip density, incur a 2-4x increase in silicon real estate, and have a higher manufacturing cost structure. Today's 5.0 V-only Flash memories are really only watered down versions of standard E^2PROMs. They use complex, multiple transistor memory cells similar to E^2PROMs. This approach to Flash memories still uses charge pumps to raise internal voltages up to

18 volts and greater. This severely stresses the memory's tunnel oxide. In part, this explains the lower endurance capability of these types of devices. 5.0 V only Flash devices have at least an order of magnitude lower cycling endurance than 12.0 V Flash memory.

In addition, non-volatile 12.0 V Flash memories are not burdened by the reliability concern of battery backed SRAMs. Why try and predict battery failure? Flash memories exhibit the time tested data retention characteristics of EPROM memory devices. There is no need for battery holders or system design compromises that permit access to the battery for replacement. Batteries are also susceptible to environmental effects of temperature and mechanical shock and vibration.

12.0 V Flash vs. DRAM & Disk Drive

The new explosive growth markets of miniature portable equipment and computers along with the associated need for transportable non-volatile memory will be another driving factor for Flash memories. This will establish Flash memories as the new memory of choice. Flash offers immediate access (instant-on) to application programs without the download time associated with transfering application code from hard disk to system memory; code is executable directly from the memory. Data files may be written and altered using the Flash memory as a rewritable storage medium. A much smaller form fit and weight factor is achieved with solid state memory versus a mechanical disk drive. Power consumption is substantially reduced and reliability increased due to the greater lifetime achieved in environmentally extreme conditions.

Table Two summarizes these issues.

Table 2

Device	Device Cost (256 K Density)	Update Cost	Total Cost
EPROM	$2.00	$150.00	$152.00
E^2PROM	$20.00	$8.00	$28.00
SRAM & Battery	$12.00	$8.00	$20.00
5.0 V Flash	$10.00 – 20.00	$8.00	$18.00 – 28.00
Flash & V_{PP} Circuitry	$5.00 $3.00	$8.00	$16.00

HOW DO FLASH MEMORIES LOWER MY TOTAL SYSTEM COST?

In-System Updates

Flash memories provide immediate dividends as soon as they are reprogrammed. Code prototype time is significantly reduced because Flash memories can be updated with new code in a manner of seconds. Updates can occur on the prototype board without any disassembly. This eliminates the time required to unplug, UV erase, reprogram, and replace EPROMs.

Manufacturing Efficiency

Manufacturing processes are simplified by using Flash memories. Board level diagnostics, final system test, and customer specific configuration code can all be downloaded into the Flash memory electrically on the assembly line. Devices may be soldered directly to the system board. This eliminates the need to disassemble the system and replace socketed devices.

Time To Market

Today being first to market often separates the winners from the also rans. Since Flash memories are reprogrammable in-system, final system code is not absolutely a necessary requirement prior to shipment. As refinements and updates are made, each previously shipped system can be updated conveniently and cost effectively. Thus your entire product line can always be as up-to-date as your newest systems rolling out the factory door.

Efficient Inventory Control

Accurate product mix forecasting is an elusive capability. Changing market conditions that deviate from even the best forecasts have real world impact on a business unit's ability to be responsive to customer demands and meet quarterly goals. Flash memories offer an innovative solution to this issue. Generic hardware systems can be planned and built without exact knowledge of final product mix. Various models of one hardware platform may be configured with customer specific code prior to shipment.

This allows you to create a more flexible and cost effective finished goods inventory. You can now respond immediately to changing market demand as soon as marketing information is available.

Field Service Savings

The prohibitive costs associated with a field service call are now a thing of the past. When updates to system code or system reconfiguration is necessary, these costly service calls may be replaced with remote updates or by distributing floppy disks with new data. In this way, systems can also be reprogrammed when usage is at a minimum. The procedures required to keep all systems up to date now become transparent to the actual end user. In addition, system reliability is not compromised when remote updates are performed. System disassembly is not required. This also eliminates handling, ESD, and component damage issues.

Advantages of AMD's 12.0 V Flash Memory Family

AMD's Flash Memories Create a Defacto Industry Standard

AMD is the first company to address the issue of device compatibility. In the world of Flash memories today, no two device offerings can be used as 100% compatible alternate sources of supply. While 32-pin pinouts are assigned for Flash E^2PROMs, programming software standards do not exist. This is one of the major issues that must be addressed in order to fuel the widespread use of Flash memories.

AMD is leading the way to promote a defacto industry standard pinout and software for Flash memories. AMD's approach allows our device to be used as a 100% alternate source with the Intel Flash memories. Our devices are 100% compatible with the Intel type of software commands while providing us the flexibility to enhance our device features. These enhancements are a natural extension of our years of experience in the E^2PROM business.

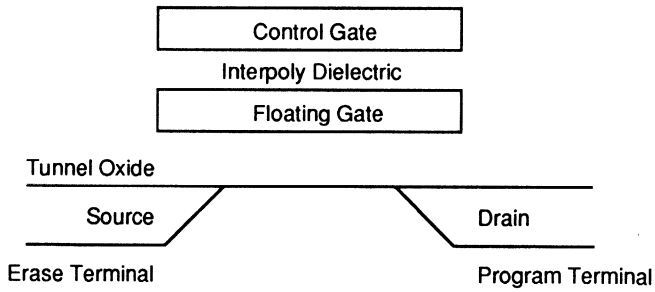
The market acceptance of Flash memories is now accelerated by the availability of 100% software and pinout compatible devices from the two largest U.S. suppliers of non-volatile memories.

Flash Memory Technology is Evolutionary

AMD is the only Flash memory supplier that is also a major manufacturer of both EPROM and E^2PROM technologies. We have transferred this experience base directly to our Flash memory technology and manufacturing process. This synergy is important because Flash memories were actually born out of a marriage of these two technologies.

We build our Flash memories on our state of the art 1.0 µM CMOS technology on the same high volume manufacturing line used for our current EPROM and E^2PROM devices. This provides the basis for our steep learning curve that will bring the cost of our 12.0 V Flash memories to within just a slight premium over UV EPROM devices.

Our many years of experience in E^2PROM design and our understanding of the issues relating to in-system write operations are incorporated into our Flash memory family. In addition, the many years of manufacturing experience and constant refinements to our thin film tunnel oxide provide immediate benefits to our Flash family.



The AMD Single Transistor Memory Cell

Figure 1. The AMD Flash Memory Cell

AMD's Flash Memory Technology

This section illustrates the fundamentals of AMD's Flash memory technology. AMD's Flash memory technology is very similar to that of our UV EPROM. The main difference is associated with the erase mechanism of Fowler-Nordheim tunneling.

Program Operations

AMD's Flash memories transfer and store charge on a floating gate in a manner similar to EPROM. This provides data retention that is equivalent to that of EPROM devices. The device is programed by raising the control gate and drain terminal to a high voltage. The source terminal is grounded.

The voltage potential across the channel attracts channel electrons from the source area toward the drain. At the drain region, some of these channel electrons become "hot." The high voltage on the control gate attracts the "hot" electrons from drain area across the thin oxide where they are trapped on the floating gate.

The Programmed State

The electrons stored on the floating gate creates an electric field which turns off the memory transistor and represents a logic zero.

Erase Operations

The Flash memory cell removes charge from the floating gate like an E^2PROM. The Fowler-Nordheim tuneling mechanism is used for erase operations. High voltage is applied to the source terminal while the control gate is grounded. This voltage potential causes the stored charge on the floating gate to tunnel through the thin oxide and into the source terminal. During the erase operation high voltage is applied to the source terminals of every memory cell at once. This produces the bulk erase characteristics of Flash memory.

The Erased State

Without the presence of electrons on the floating gate, the transistor is conductive and represents a logic one.

Programming Endurance

AMD's Flash memory technology incorporates the traditional EPROM programming mechanism of hot electron injection and the standard E^2PROM erase mechanism of Fowler-Nordheim tunneling. AMD achieves the highest level of endurance capability by performing each of the program and erase operations on separate terminals of the memory cell. This is because programming and erase methods employ different charge transfer mechanisms. This way the memory cell can be optimized for each separate mechanism. In addition, the V_{PP} voltage used for program and erase operations is lower than the voltages used by traditional E^2PROMs. This significantly lowers the stress on the tunnel oxide during erase operations and hence extends the cycling capability of the tunnel oxide by orders of magnitude.

Manufacturing Efficiency

AMD also leads the industry as the most cost efficient manufacturer of non-volatile memories. Our EPROM experience base again offers immediate benefits to our Flash family. We continue to the lead the competition with the smallest Flash memory chips. Thus, we are positioned to be the lowest cost Flash memory supplier in the industry. This not only ensures our viability as a long term supplier but also ensures you of a ready supply of product.

Zero Wait State Systems

AMD's Flash memories let you take full advantage of your high performance microprocessor systems. Our devices lead the industry with the fastest access times available. AMD's Am28F256 and Am28F512 devices are available at 70ns and our Am28F010 one Megabit device is available at 90ns. These devices operate at typically twice the performance of our competitors. Again, this advantage is a direct result of AMD's high performance EPROM leadership.

Inadvertant Write Protection

The AMD Flash memory incorporates an on-chip state machine to determine the operating mode of the device. The state machine is accessed only via the on chip command register. In turn, the command register is only enabled when the 12.0 V V_{PP} voltage is active. Without the V_{PP} voltage, memory contents can not be altered.

The command register is manipulated by a combination of three control pins. The only condition valid for a write operation is when $\overline{OE}$ is high and both $\overline{CE}$ and $\overline{WE}$ are low. Any other state is considered a non-write state. Data can not be transferred from the command register to the state machine if a non-write state condition exists.

The state machine requires a sequence of two-cycle bus commands to change the "state" of the Flash memory device. Should an improper sequence of commands be issued to the device it will interpret these as "illegal" commands and safely reset to the read only mode and terminate any current operation. The two-cycle bus commands tend to eliminate the potential for inadvertent writes should system glitches occur. It is unlikely that the proper sequence and timing of these glitches would resemble actual valid commands. This is an advantage over other approaches to Flash memories that simply use control pins to initiate write operations.

In addition, during system power transitions the Flash memory device automatically resets to the read mode. The command register may also be effectively locked out of transfering any commands to the state machine by tying the $\overline{WE}$ pin to the device V_{CC} pin. Thus, $\overline{WE}$ will always be in a non-write configuration until driven low by the system write control line.

Please refer to application note AN–101 for details regarding this issue.

Efficient Programming Algorithms Also Guarantee Data Retention

AMD's Flash memory programming algorithms use an interactive approach to adequately program and erase the device with a minimal number of pulses.

We guarantee data retention by using a similar margin verify concept employed by EPROM programming algorithms. During the verify mode an internally generated margin verify voltage is applied to each addressed memory location. The verify voltage is generated internally on chip from the static 12.0 V V_{PP} supply. In this way, data retention is guaranteed to equal that of EPROM memories.

Generating V_{PP} Programming Voltages

In many of today's systems a regulated 12.0 V supply is available. If this is not the case, there are many alternatives for generating this voltage. They vary from DC/DC or analog convertors that can pump up 5.0 V from the system V_{CC} to the regulated 12.0 V V_{PP} supply. In addition, there are many DC/DC convertors that take higher incoming voltages and step them down to the regulated V_{PP} output voltage.

The cost of implementing the voltage generation typically costs less than a fraction of the Flash memory itself and best of all it can be amortized over the entire Flash memory array. Many of these solutions offer enough programming current to program and erase four (4) devices in parallel. This would be sufficient for many of today's 32-bit word systems.

Please refer to application note AN–102 for details regarding this issue.

Preliminary

Am28F256

32,768 x 8-Bit CMOS Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
- **Compatible with JEDEC-standard byte-wide pinouts**
  - 32-pin DIP
  - 32-pin PLCC
- **10,000 erase/program cycles**
- **Program and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Flasherase™ Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite™ Programming**
  - 10 µs typical byte-program
  - Less than 0.5 second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell

GENERAL DESCRIPTION

The Am28F256 is a 256K "Flash" electrically erasable, electrically programmable read only memory organized as 32K bytes of 8 bits each. The Am28F256 is packaged in 32-Pin PDIP and PLCC versions which allow for upgrades to the 2 Megabit density. The device is also offered in ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F256 offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F256 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F256 uses a command register to manage this functionality, while maintaining a standard 32-Pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F256 uses a 12.0 V ±5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to V_{CC}+1 V.

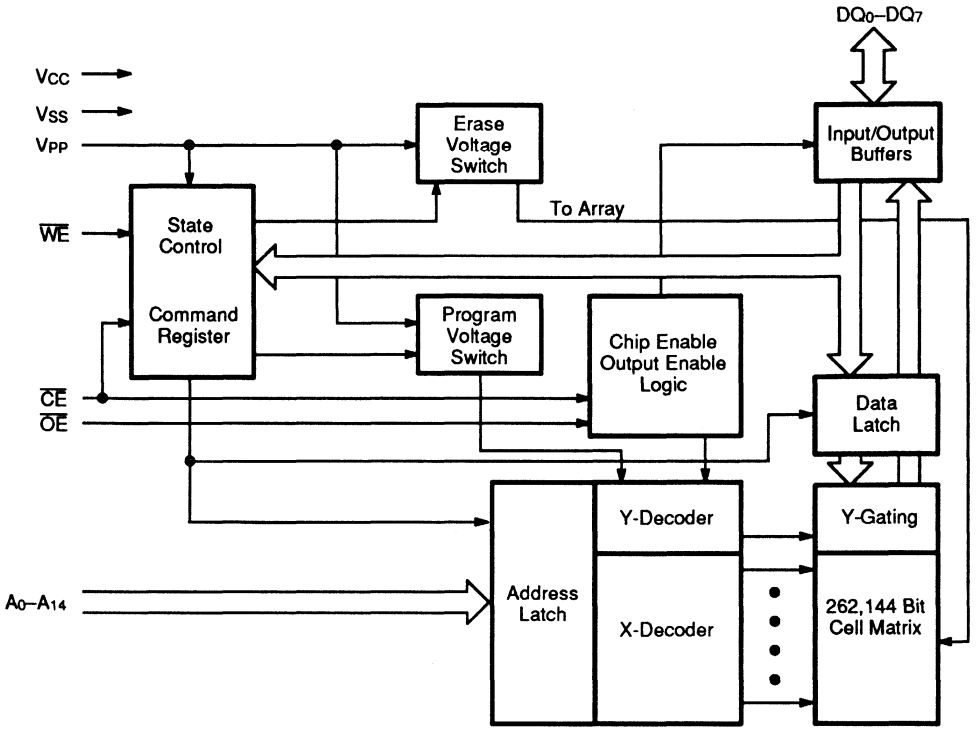
The Am28F256 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F256 is less than one half a second. The entire chip is bulk erased using 10ms erase pulses according to AMD's Flasherase algorithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM erasure using ultraviolet light are eliminated.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F256 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F256 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Publication# 11560 Rev. C Amendment/0
Issue Date: March 1991

BLOCK DIAGRAM



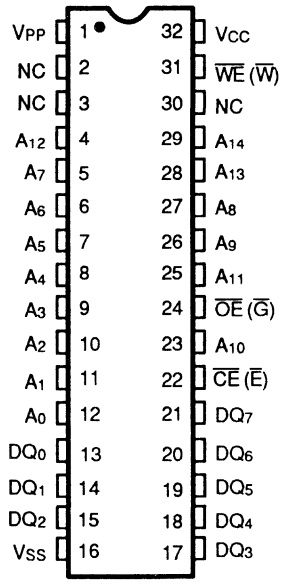
11561-001B

PRODUCT SELECTOR GUIDE

Family Part No.	Am28F256			
Ordering part No:				
± 10% VCC Tolerance	-90	-120	-150	-200
± 5% VCC Tolerance	-95	—	—	—
Max Access Time (ns)	90	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	75	75

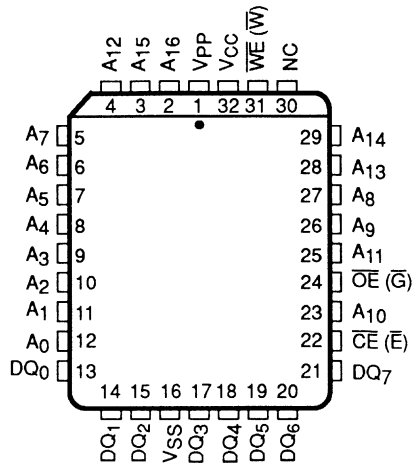
CONNECTION DIAGRAMS

DIP



11560-002A

PLCC*

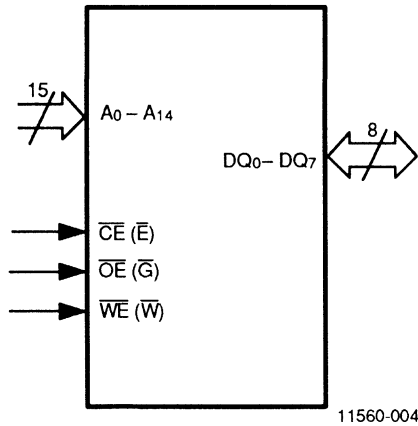


11560-003A

Note: Pin 1 is marked for orientation.

* Also available in LCC.

LOGIC SYMBOL

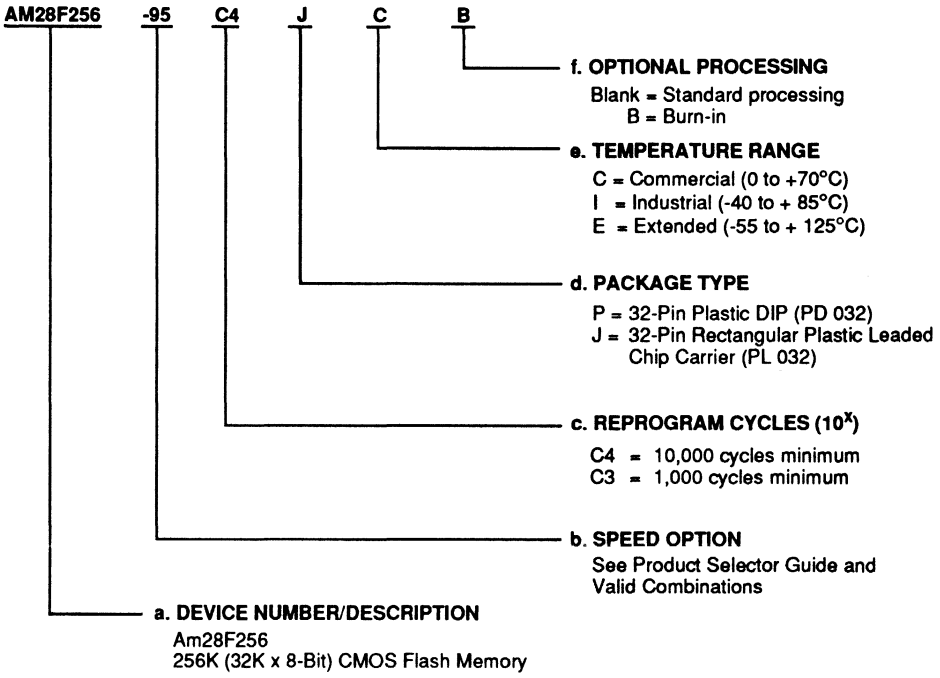


11560-004A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram Cycles
d. Package Type
e. Temperature Range
f. Optional Processing



Valid Combinations	
AM28F256-90 AM28F256-95	C4PC, C4JC, C4PCB, C4JCB, C3PC, C3JC, C3PCB, C3JCB
AM28F256-120 AM28F256-150 AM28F256-200	C4PC, C4PI, C4JC, C4JI, C4PCB, C4PIB, C4JCB, C4JIB, C4PE, C4PEB, C4JE, C4JEB C4JI, C3PC, C3PI, C3JC, C3JI, C3PCB, C3PIB, C3JCB, C3JIB, C3PE, C3PEB, C3JE, C3JEB

Valid Combinations

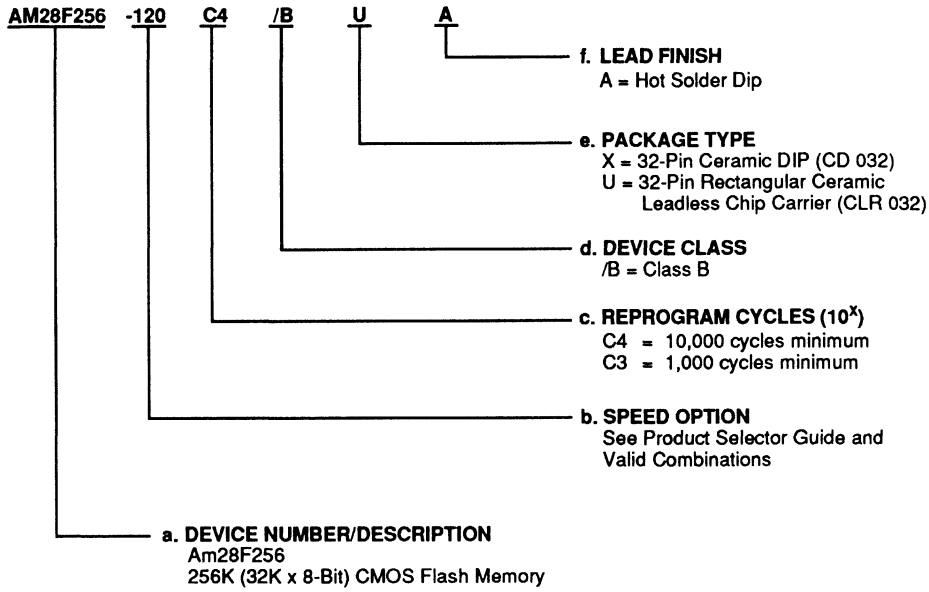
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram cycles
d. Device Class
e. Package Type
f. Lead Finish



Valid Combinations	
AM28F256-120 AM28F256-150 AM28F256-200	C4/BXA, C4/BUA C3/BXA, C3/BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$A_0 - A_{14}$

Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$DQ_0 - DQ_7$

Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

$\overline{CE}$ ($\overline{E}$)

The Chip Enable active low input activates the chip'scontrol logic and input buffers. Chip Enable high deselects the device and operates the chip in stand-by mode.

$\overline{OE}$ ($\overline{G}$)

The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

$\overline{WE}$ ($\overline{W}$)

The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

V_{PP}

Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2V$.

V_{CC}

Power supply for device operation. (5.0V ± 5% or 10%)

V_{SS}

Ground

NC

No Connect-corresponding pin is not connected internally to the die.

BASIC PRINCIPLES

The Am28F256 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F256 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F256's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F256 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Erase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase Algorithm.

1. **Set-up Erase:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command.
3. **Erase-verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Set-up Program:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command.
3. **Program-verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

FUNCTIONAL DESCRIPTION
Description Of User Modes

Table 1. Am28F256 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (A1H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:
X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2V$, See DC Characteristics for voltage levels of V_{PPH}, $0V < An < V_{CC} + 2V$, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC} + 2.0V$. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0V$
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2V$

Command Register Inactive

Read

The Am28F256 functions as a read only memory when $V_{PP} < V_{CC} + 2V$. The Am28F256 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F256 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5V$), consumes less than 100µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A Prom Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5V to 13.0V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0V$ while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F256 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F256 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	A1	1	0	1	0	0	0	0	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits $R_7 - R_0$ correspond to the data inputs $DQ_7 - DQ_0$ (Refer to Table 3). Register bits $R_7 - R_5$ store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H or 80H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands (Notes 1, 2)	X	X	X	X	X	X	X	X

Notes:

1. See Table 4 Am28F256 Command Definitions
2. X = Appropriate Data or Register Commands

Table 4. Am28F256 Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Notes 6, 7)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/A1H
Set-up Erase/Erase (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 7)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Wait 6 µs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.
7. Please refer to Reset Command section on page 5–18.

Erase Sequence

Set-up Erase/Erase Commands

Set-up Erase

Set-up Erase is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Set-up Erase operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{pp} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.

Erase-verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F256 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte in

the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Set-up Erase/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:

The erase-verify command must be written to the register in order to terminate the erase operation. During the erase operations, the local microprocessor must be dedicated to run software timing routines (erase in 10ms) as specified in AMD's Flasherase algorithm.

Should a system interrupt occur during an erase operation, always write the Erase-verify command prior to executing an interrupt sequence.

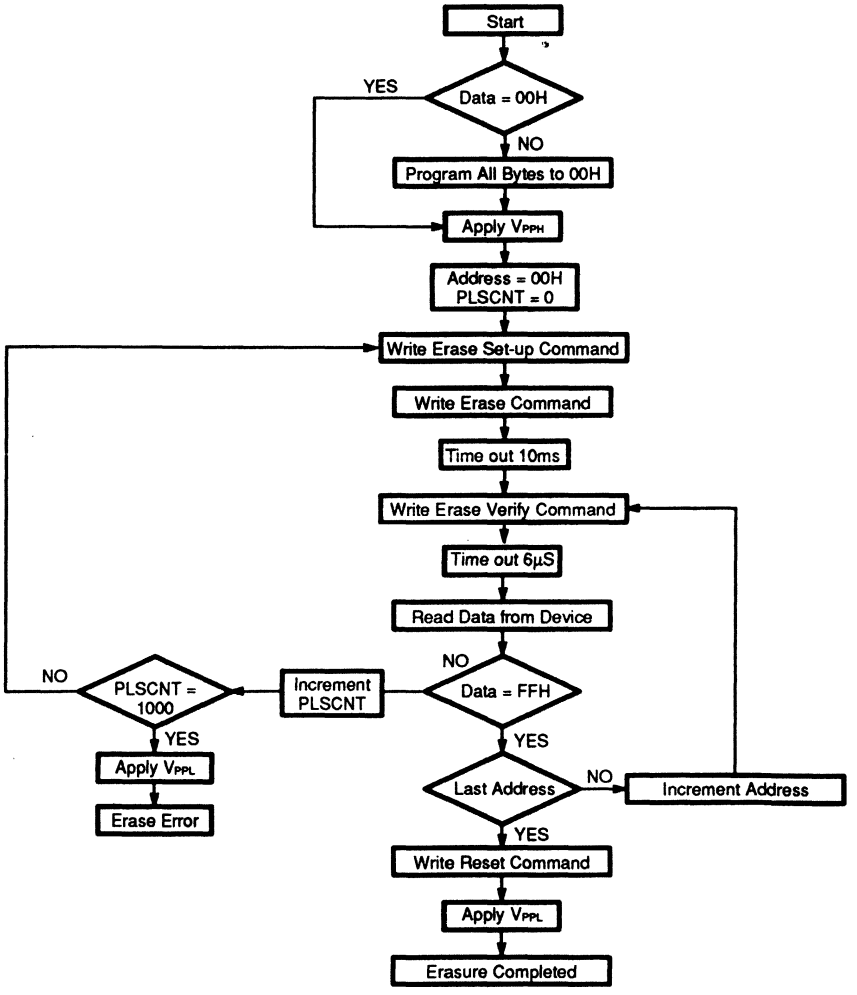


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Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F256 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

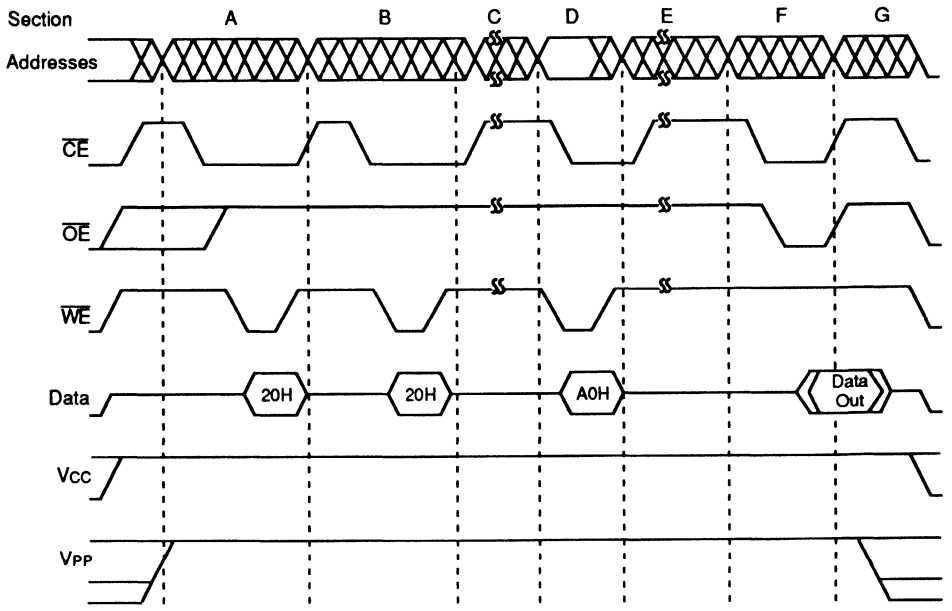
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (1 second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase operations are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. Erasure typically occurs in one second. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 2) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Set-Up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Set-up Erase	Erase	Erase (10ms)	Erase-verify	Transition (6μs)	Erase verification	Stand by & Vcc Power down

Figure 2. A.C. Waveforms For Erase Operations

Analysis Of Erase Timing Waveform

Note:
This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flasherase algorithm.

Set-up Erase/Erase

This analysis illustrates the use of two-cycle erase commands (section A&B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-out

A software timing routine (10ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Erase-verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6μs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Notes:

1. All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.

2. The erase verify command must be written to terminate the erase operation. Should a system interrupt occur during an erase operation, always write the erase-verify command prior to executing an interrupt sequence.

Programming Sequence

Set-up Program/Program Command

Set-up Program

The Am28F256 is programmed byte by byte. Bytes may be programmed sequentially or at random. Set-up Program is the first of a two-cycle program command. It stages the device for byte programming. The Set-up Program operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F256 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Set-up Program/Program). Figure 3 and Table 6 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F256 Flashrite programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the programming algorithm.

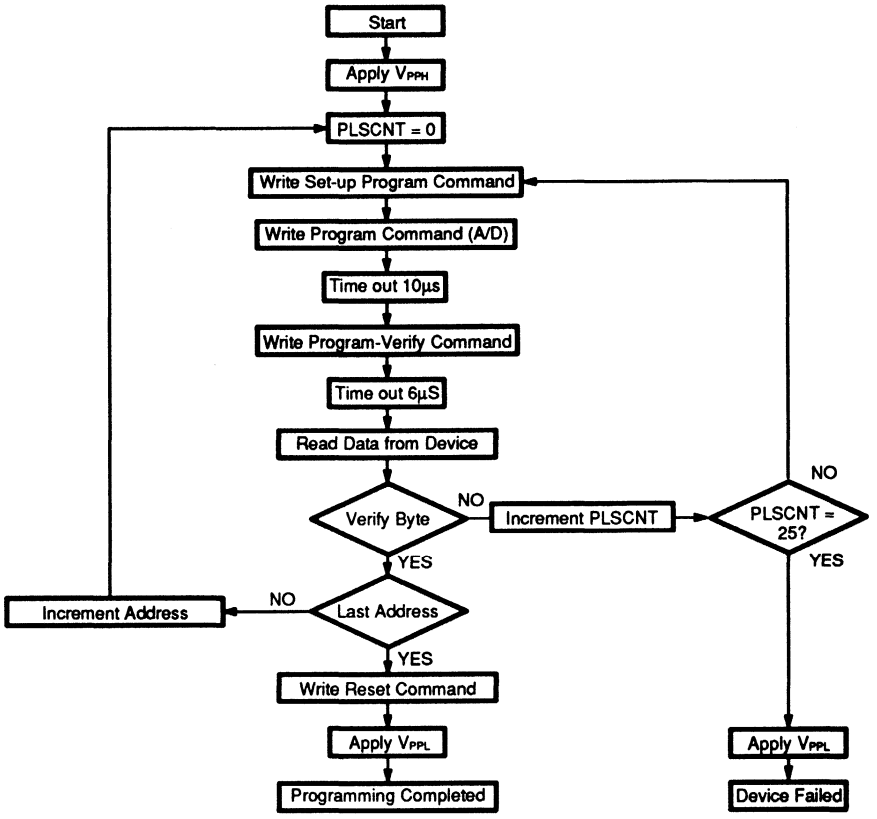


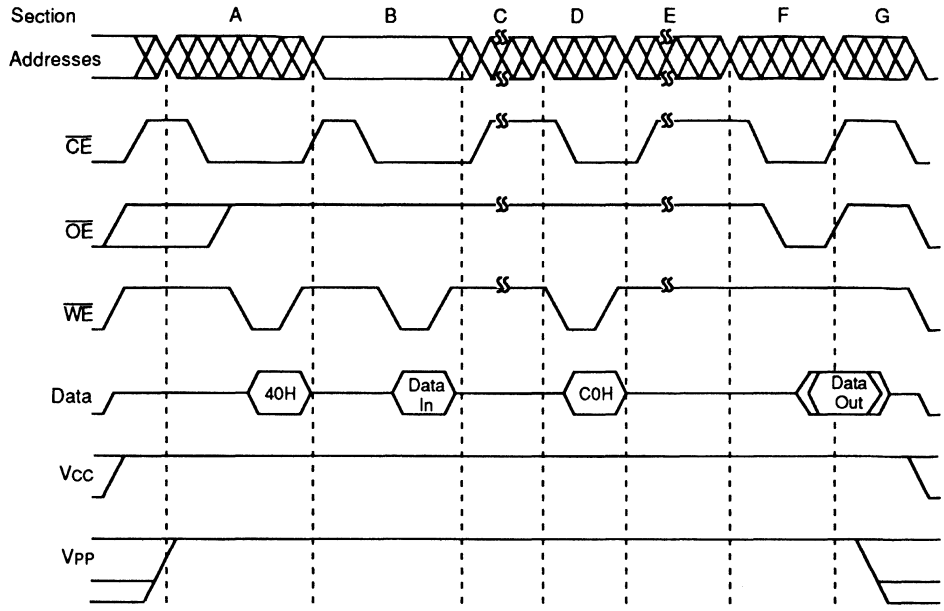
Figure 3. Flashrite Programming Algorithm

Table 6. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Set-up Program	Program Command Latch Address & Data	Program (10µs)	Program verify	Transition (6µs)	Program verification	Stand by & Vcc Power down

Figure 4. A.C. Waveforms for Programming Operations

Analysis Of Program Timing Waveforms

Set-up Program/Program

Two-cycle write commands are required for program operations (section A&B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-out

A software timing routine (10µs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Program-verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Note:
The program-verify operation must be written to terminate the programming operation. Should a system interrupt occur during a programming operation, always write the program-verify command prior to executing an interrupt sequence.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1µF/device. V_{PP} must reach its final value 100ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse, or the device may continue to erase until the memory cells are driven into depletion (over-erasure). Should this happen the internal circuitry will no longer select unique addresses. A symptom of over-erasure is an error attempting to program the next time. Occasionally it is possible to recover over-erased devices by programming all of the locations with 00H data.
3. A third delay time is required for each programming pulse width (10 µs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 µs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:
Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified seperately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-up Sequence

V_{CC} Prior to V_{PP}

The Am28F256 powers-up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two step command sequence.

V_{PP} Prior to V_{CC}

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. With V_{PP} = 12 V, the Flash device resets to the Read mode when V_{CC} rises above 2 V.

Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the set-up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The set-up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the set-up Program state or not.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-system

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F256 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code A1H (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
Ceramic Packages	– 65°C to +150°C
Plastic Packages	– 65°C to +125°C
Ambient Temperature with Power Applied	– 55°C to + 125°C
Voltage with Respect To Ground	
All pins except A_9 and V_{PP} (Note 1)	– 2.0V to 7.0V
V_{CC} (Note 1)	– 2.0V to 7.0V
A_9 (Note 2)	– 2.0V to 14.0V
V_{PP} (Note 2)	– 2.0V to 14.0V
Output Short Circuit Current (Note 3)	200mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A_9 and V_{PP} pins is –0.5V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) – 40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) – 55°C to +125°C

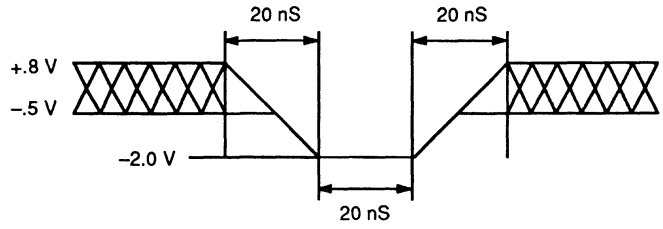
Military (M) Devices
Case Temperature (T_C) – 55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am28F256–X5 + 4.75V to +5.25V
V_{CC} for Am28F256–XX0 + 4.50V to +5.50V

V_{PP} Supply Voltages
Read – 0.5V to +12.6V
Program, Erase, and Verify + 11.4V to +12.6V

MAXIMUM OVERSHOOT

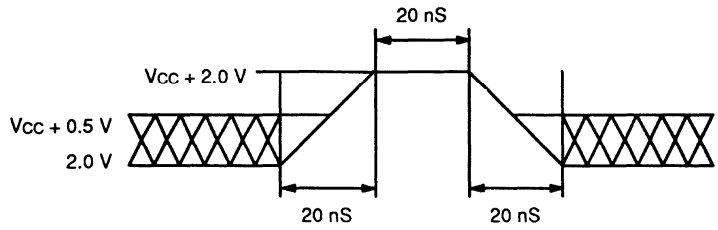
Maximum Negative Input Overshoot



11561-009A

Maximum Negative Overshoot Waveform

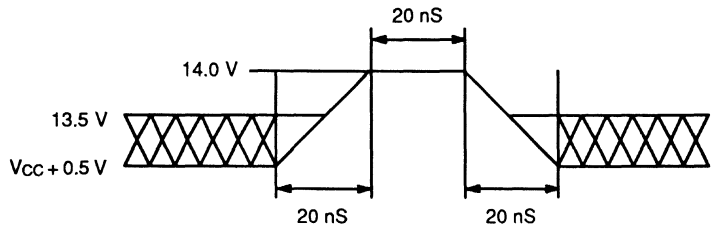
Maximum Positive Input Overshoot



11561-010A

Maximum Positive Overshoot Waveform

Maximum V_{PP} Overshoot



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Maximum V_{PP} Overshoot Waveform

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted). (Notes 1–3)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

PRELIMINARY					
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min.**	**Max.**	**Unit**
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or Vss		± 1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or Vss		± 1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{IH}		1.0	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}		± 1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH} V_{PP} = V_{PPL}		200 ± 1.0	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA V_{CC} = V_{CC} Min.	2.4		V
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

DC CHARACTERISTICS-CMOS COMPATIBLE

PRELIMINARY					
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min.**	**Max.**	**Unit**
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ± 0.5 V		100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}		±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85 V_{CC}		V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC} –0.4		
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/ Program are inhibited when V_{PP} = V_{PPL}	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

Notes:

1. **Caution:** the Am28F256 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified.

AC CHARACTERISTICS-Read Only Operation (Notes 1– 2)

PRELIMINARY								
Parameter Symbols				Am28F256				
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	Unit
t_{AVAV}	t_{RC}	Read Cycle Time	Min. Max.	90	120	150	200	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	90	120	150	200	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	90	120	150	200	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min. Max.	35	50	75	75	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	Min. Max.	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z	Min. Max.	25	30	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	Min. Max.	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z	Min. Max.	25	30	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	Min. Max.	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min. Max.	6	6	6	6	µs
t_{VCS}		V_{CC} Set-up Time to Valid Read	Min. Max.	50	50	50	50	µs

Notes:

1. Output Load (except Am28F256-95): 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: ≤ 10 ns, Input Pulse levels: 0.45 to 2.4 V, Timing Measurement Reference Level - Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F256-95 Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. t_{VCS} is guaranteed by design not tested.

AC CHARACTERISTICS-Write/Erase/Program Operations (Notes 1– 4)

PRELIMINARY								
Parameter Symbols				Am28F256				
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	Min. Max.	90	120	150	200	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min. Max.	45	50	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation	Min. Max.	10 25	10 25	10 25	10 25	µs
t_{WHWH2}		Duration of Erase Operation	Min. Max.	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	ms
t_{EHVP}		Chip Enable Set-Up Time to V_{PP} Ramp	Min. Max.	100	100	100	100	ns
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	Min. Max.	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable Low	Min. Max.	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH}	Min. Max.	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL}	Min. Max.	500	500	500	500	ns

Notes:

1. Read timing characteristics during read/write operations are the same as durng read-only operations. Refer to AC Characteristics for Read Only operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines theWrite PulseWidth (within a longer Write-Enable timing waveform) all set-up, hold and inactiveWrite-Enable times should be measured relative to the Chip-Enable waveform.
3. All devices except Am28F256-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
4. Am28F256-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V

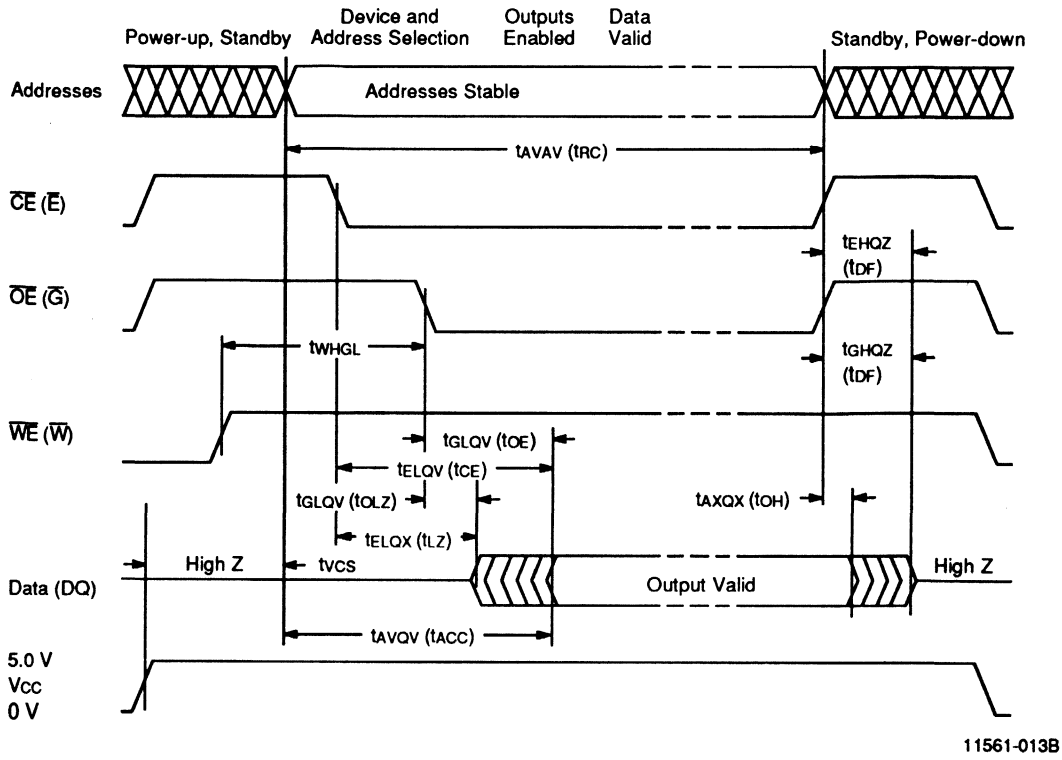


Figure 5. AC Waveforms for Read Operations

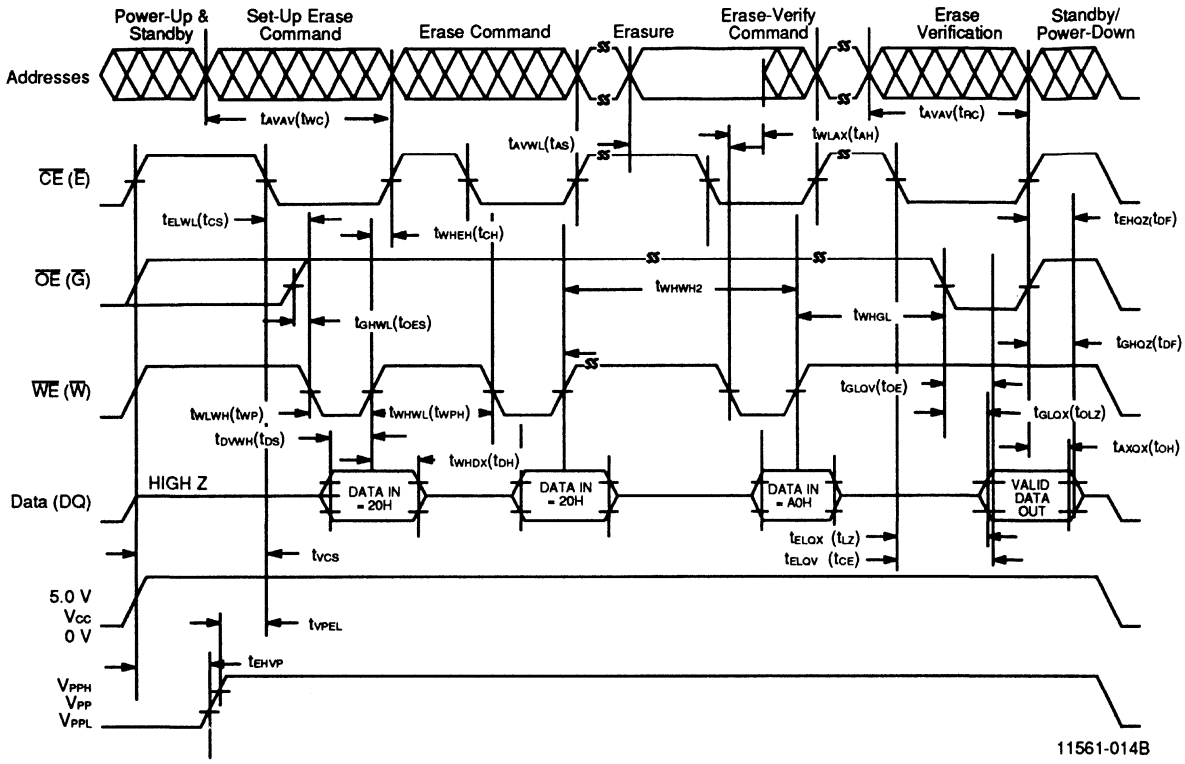


Figure 6. A.C. Waveforms for Erase Operations

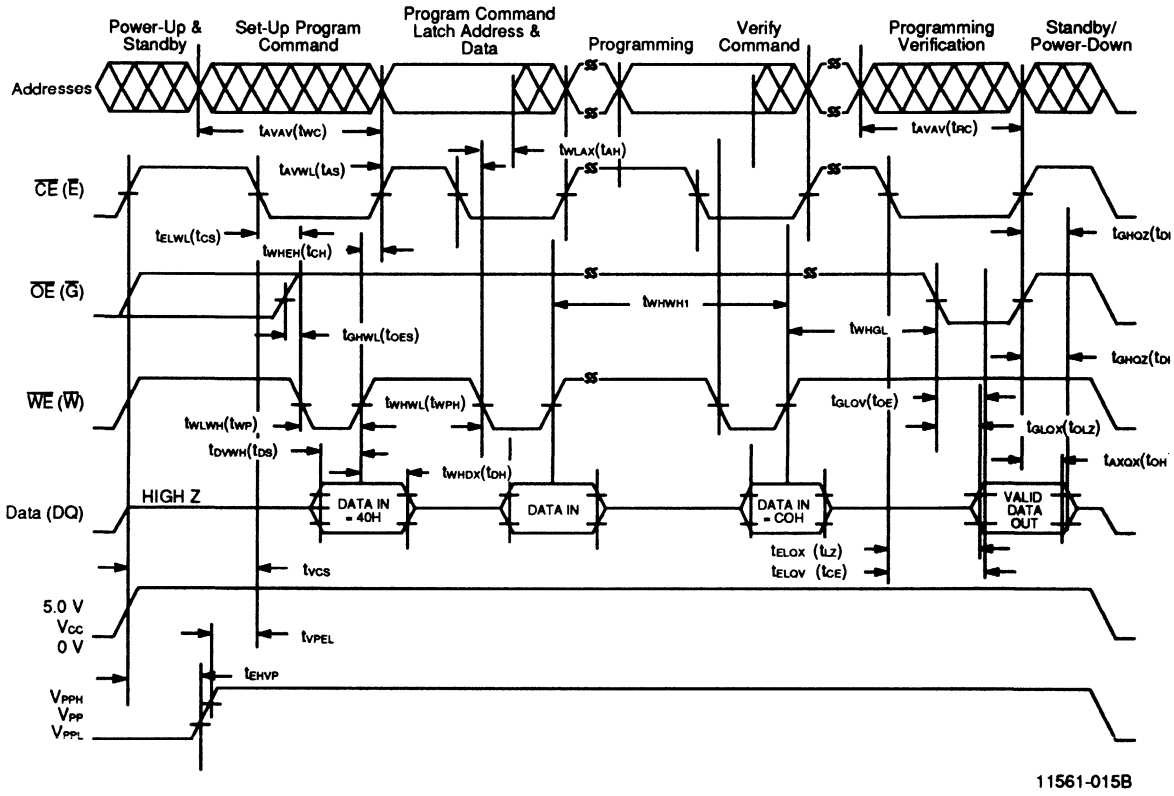
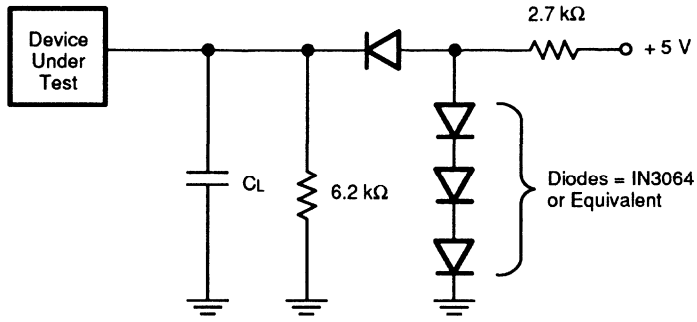


Figure 7. A.C. Waveforms for Programming Operations

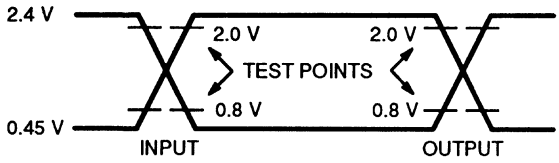
SWITCHING TEST CIRCUIT



11561-012A

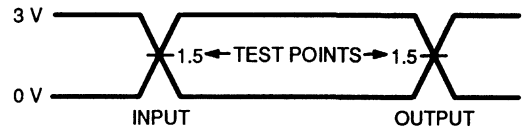
C_L = 100 pF including jig capacitance (30 pF for Am28F256-95)

SWITCHING TEST WAVEFORMS



All Devices Except Am28F256-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.



For Am28F256-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

08007-003A

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Chip Erase Time		0.5 (Note 1)	10	S	Excludes 00H programming prior to erasure
Chip Programming Time		0.5 (Note 1)	6	S	Excludes system-level overhead
Erase/Program Cycles					
Am28F256-95C4JC	10,000			Cycles	
Am28F256-95C3JC	1,000			Cycles	

Note:

1. 25°C, 12V V_{PP}

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	– 1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	– 1.0 V	V_{CC} + 1.0 V
Current	– 100 mA	+ 100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

Preliminary

Am28F512

65,536 x 8-Bit CMOS Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
- **Compatible with JEDEC-standard byte-wide pinouts**
  - 32-pin DIP
  - 32-pin PLCC
- **10,000 erase/program cycles**
- **Program and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from −1 V to V_{CC} +1 V**
- **Flasherase™ Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite™ Programming**
  - 10 µs typical byte-program
  - Less than 1 second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell

GENERAL DESCRIPTION

The Am28F512 is a 512K "Flash" electrically erasable, electrically programmable read only memory organized as 64K bytes of 8 bits each. The Am28F512 is packaged in 32-pin PDIP and PLCC versions which allow for upgrades to the 2 Megabit density. The device is also offered in ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F512 offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F512 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F512 uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F512 uses a 12.0 V ±5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from −1 V to V_{CC}+1 V.

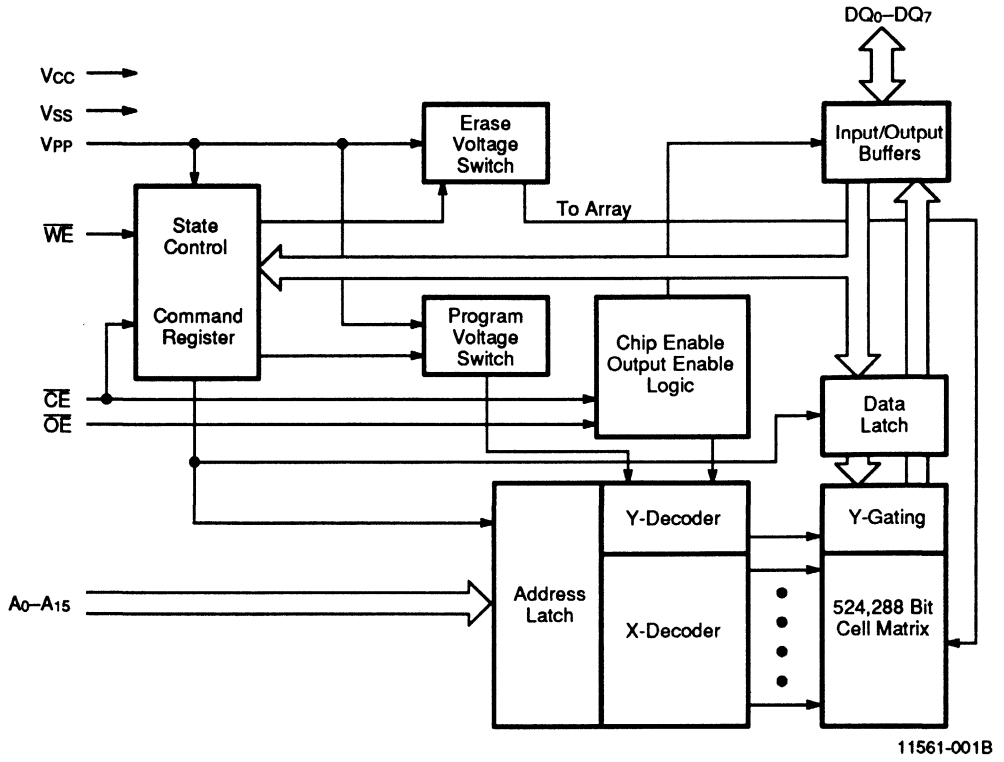
The Am28F512 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F512 is less than one second. The entire chip is bulk erased using 10ms erase pulses according to AMD's Flasherase algorithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM erasure using ultraviolet light are eliminated.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F512 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F512 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Publication# 11561 Rev. C Amendment/0
Issue Date: March 1991

BLOCK DIAGRAM

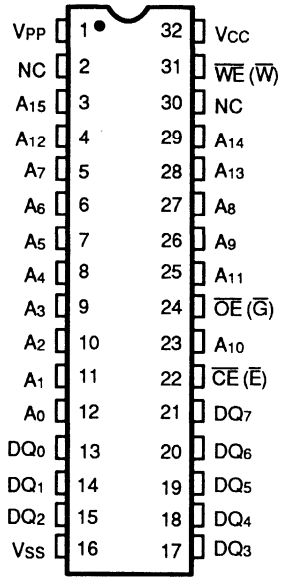


PRODUCT SELECTOR GUIDE

Family Part No.	Am28F512			
Ordering part No:				
± 10% V_{CC} Tolerance	-90	-120	-150	-200
± 5% V_{CC} Tolerance	-95	—	—	—
Max Access Time (ns)	90	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	75	75

CONNECTION DIAGRAMS

DIP



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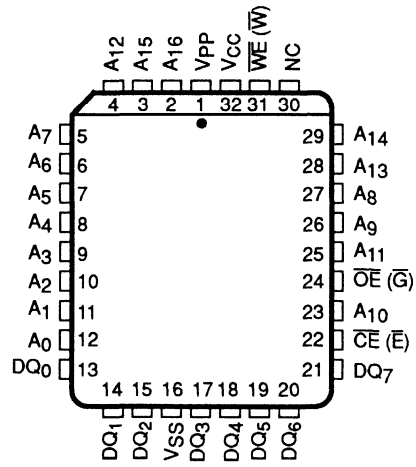
PLCC*

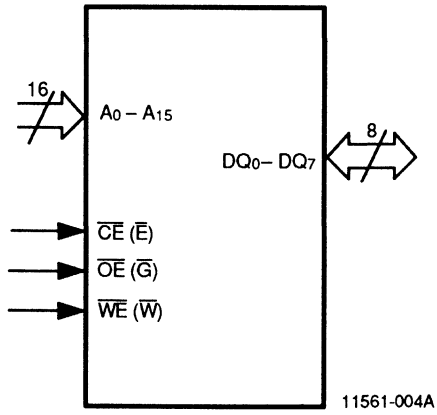


11561-003B

Note: Pin 1 is marked for orientation.

* Also available in LCC.

LOGIC SYMBOL



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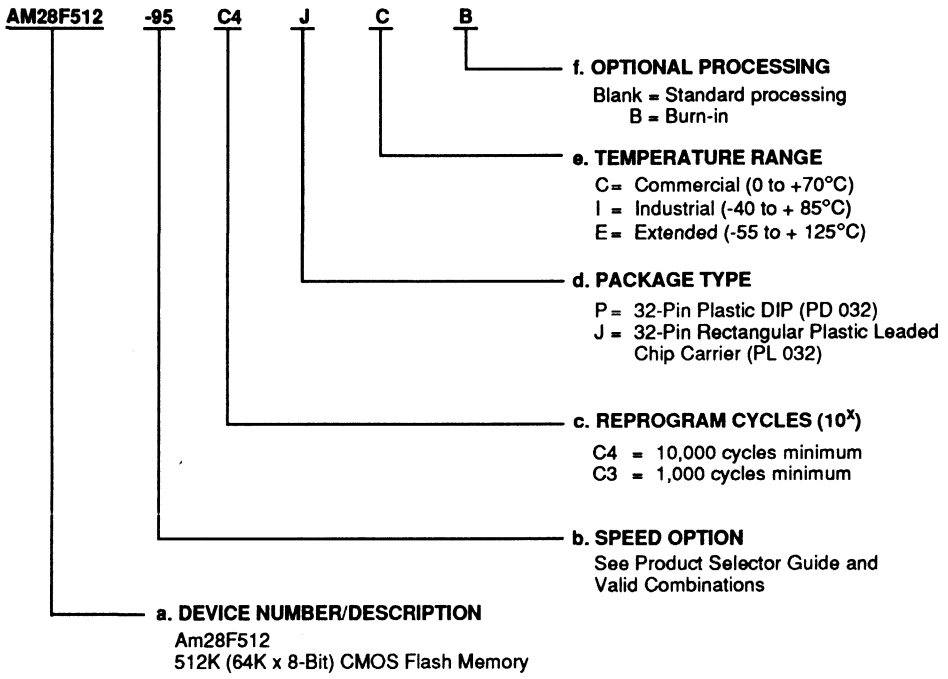
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram Cycles
d. Package Type
e. Temperature Range
f. Optional Processing



Valid Combinations	
AM28F512-95 AM28F512-90	C4PCB, C4JCB, C4PC, C4JC, C3PC, C3JC, C3PCB, C3JCB
AM28F512-120 AM28F512-150 AM28F512-200	C4PC, C4PI, C4JC, C4PCB, C4PIB, C4JCB, C4JIB, C4PE, C4PEB, C4JE, C4JEB, C4JI, C3PC, C3PI, C3PCB, C3PIB, C3JCB, C3JIB, C3PE, C3PEB, C3JE, C3JEB, C3JC, C3JI

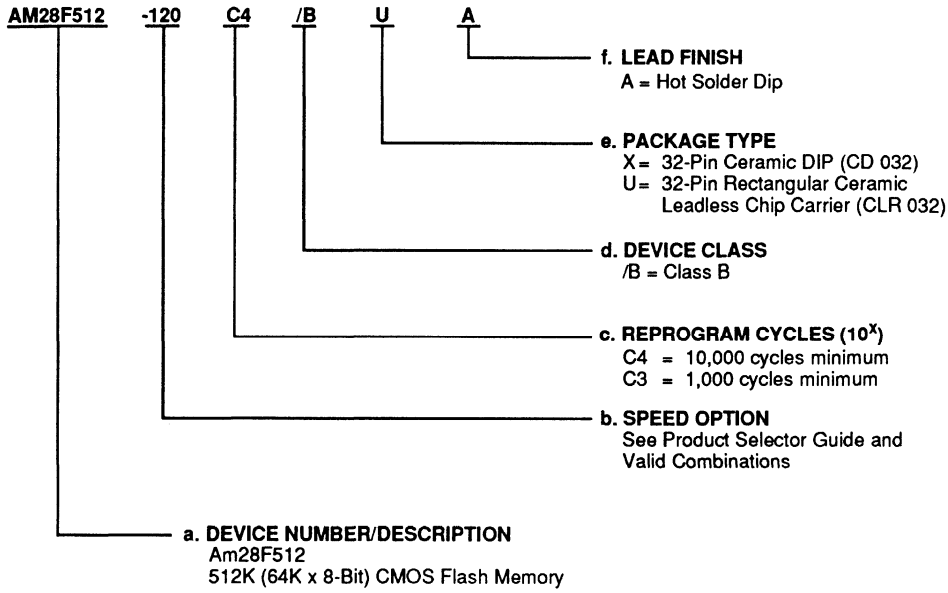
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram cycles
d. Device Class
e. Package Type
f. Lead Finish



Valid Combinations	
AM28F512-120 AM28F512-150 AM28F512-200	C4/BXA, C4/BUA C3/BXA, C3/BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$A_0 - A_{15}$

Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$DQ_0 - DQ_7$

Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

$\overline{CE}$ ($\overline{E}$)

The Chip Enable active low input activates the chip'scontrol logic and input buffers. Chip Enable high will deselect the device and operates the chip in standby mode.

$\overline{OE}$ ($\overline{G}$)

The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

$\overline{WE}$ ($\overline{W}$)

The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

V_{PP}

Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2V$.

V_{CC}

Power supply for device operation. (5.0V ± 5% or 10%)

V_{SS}

Ground

NC

No Connect-corresponding pin is not connected internally to the die.

BASIC PRINCIPLES

The Am28F512 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F512 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F512's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F512 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Erase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase Algorithm.

1. **Set-up Erase:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command.
3. **Erase-verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Set-up Program:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command.
3. **Program-verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am28F512 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (25H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:
X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2V$, See DC Characteristics for voltage levels of V_{PPH}, $0V < An < V_{CC} + 2V$, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC} + 2.0V$. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0V$
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V

Command Register Inactive

Read

The Am28F512 functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F512 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F512 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1 mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A Prom Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0$ V while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F512 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F512 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	25	0	0	1	0	0	1	0	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits $R_7 - R_0$ correspond to the data inputs $DQ_7 - DQ_0$ (Refer to Table 3). Register bits $R_7 - R_5$ store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H or 80H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6 µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands*	X	X	X	X	X	X	X	X

*** Notes:**

1. See Table 4 Am28F512 Command Definitions
2. X = Appropriate Data or Register Commands

Table 4. Am28F512 Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Notes 6, 7)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/25H
Set-up Erase/Erase (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 7)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Wait 6 µs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.
7. Please refer to Reset Command section on page 5–47.

Erase Sequence

Set-up Erase/Erase Commands

Set-up Erase

Set-up Erase is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Set-up Erase operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{pp} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.

Erase-verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F512 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte in

the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Set-up Erase/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The erase-verify command must be written to the register in order to terminate the erase operation. During the erase operations, the local microprocessor must be dedicated to run software timing routines (erase in 10ms) as specified in AMD's Flasherase algorithm.

Should a system interrupt occur during an erase operation, always write the Erase-verify command prior to executing an interrupt sequence.

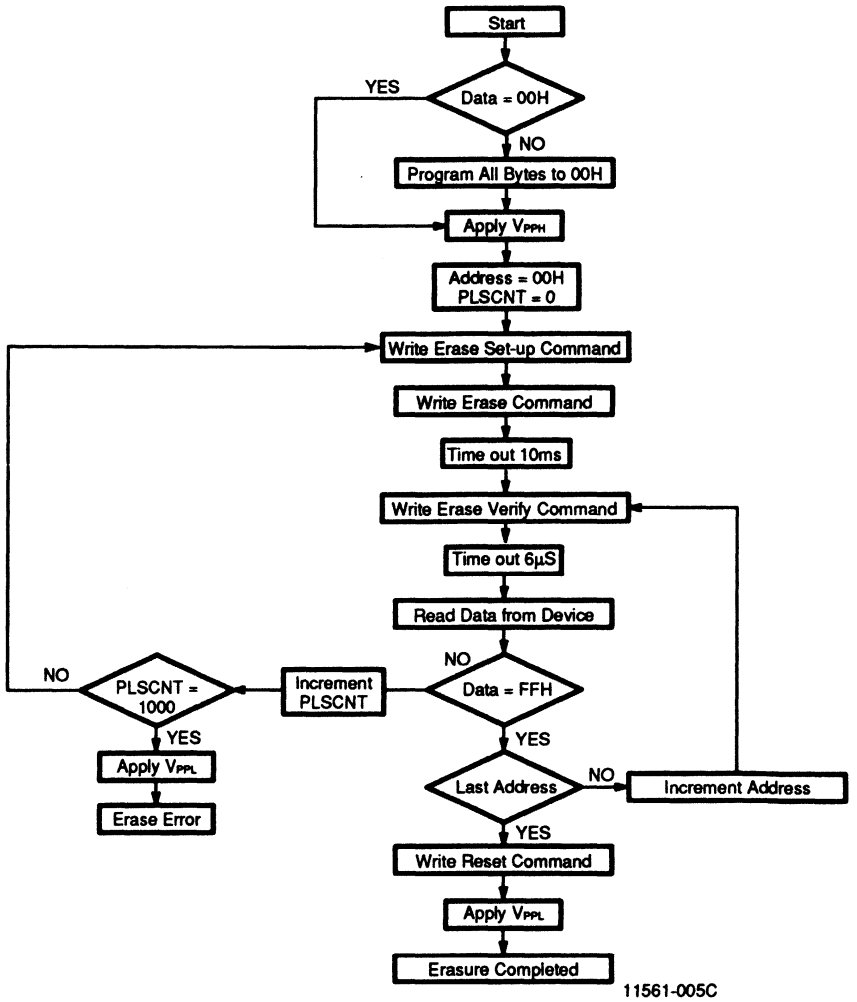


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F512 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

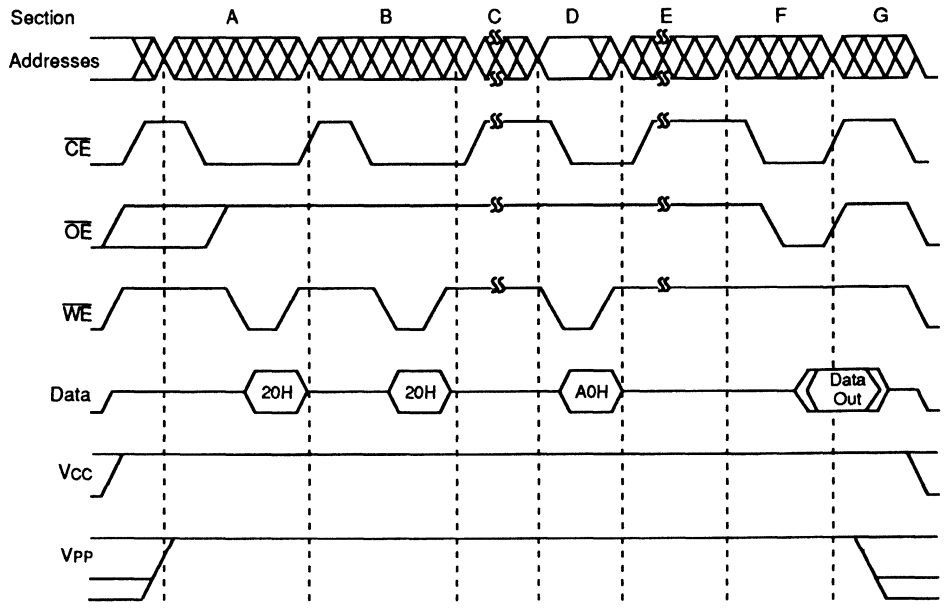
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (1 second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase operations are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. Erasure typically occurs in one second. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 2) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Set-Up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Set-up Erase	Erase	Erase (10ms)	Erase-verify	Transition (6µs)	Erase verification	Stand by & Vcc Power down

Figure 2. A.C. Waveforms For Erase Operations

Analysis Of Erase Timing Waveform

Note:
This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flasherase algorithm.

Set-up Erase/Erase

This analysis illustrates the use of two-cycle erase commands (section A&B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-out

A software timing routine (10 ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Erase-verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Notes:

1. All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.

2. The erase verify command must be written to terminate the erase operation. Should a system interrupt occur during an erase operation, always write the erase-verify command prior to executing an interrupt sequence.

Programming Sequence

Set-up Program/Program Command

Set-up Program

The Am28F512 is programmed byte by byte. Bytes may be programmed sequentially or at random. Set-up Program is the first of a two-cycle program command. It stages the device for byte programming. The Set-up Program operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F512 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Set-up Program/Program). Figure 3 and Table 6 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F512 Flashrite programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the programming algorithm.

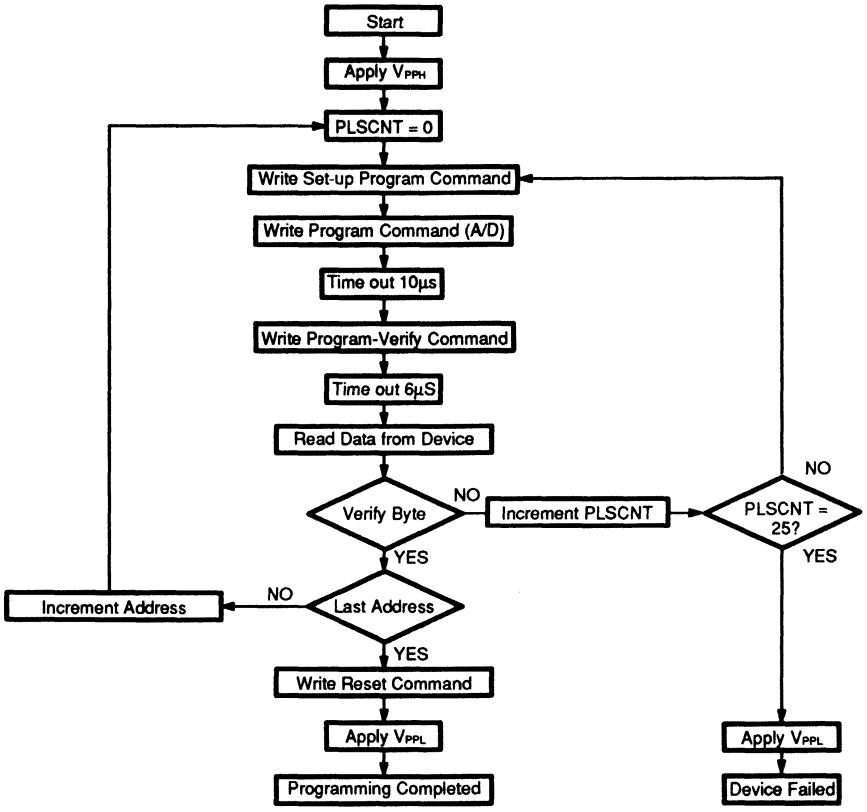


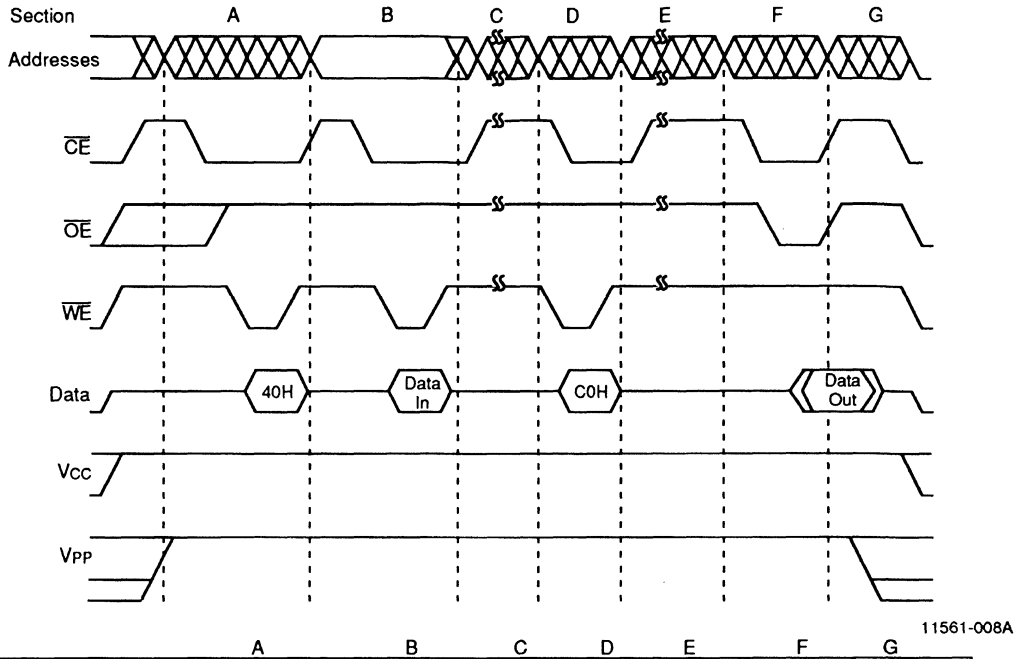
Figure 3. Flashrite Programming Algorithm

Table 6. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Set-up Program	Program Command Latch Address & Data	Program (10 µs)	Program verify	Transition (6 µs)	Program verification	Stand by & Vcc Power down

Figure 4. A.C. Waveforms for Programming Operations

Analysis Of Program Timing Waveforms

Set-up Program/Program

Two-cycle write commands are required for program operations (section A&B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-out

A software timing routine (10 µs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Program-verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Note:
The program-verify operation must be written to terminate the programming operation. Should a system interrupt occur during a programming operation, always write the program-verify command prior to executing an interrupt sequence.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1 µF/device. V_{PP} must reach its final value 100ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse, or the device may continue to erase until the memory cells are driven into depletion (over-erasure). Should this happen the internal circuitry will no longer select unique addresses. A symptom of over-erasure is an error attempting to program the next time. Occasionally it is possible to recover over-erased devices by programming all of the locations with 00H data.
3. A third delay time is required for each programming pulse width (10 µs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 µs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:
Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified seperately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-up Sequence

V_{CC} Prior to V_{PP}

The Am28F512 powers-up in the Read only mode. In addition, memory contents may only be altered after successful completion of a two step command sequence.

V_{PP} Prior to V_{CC}

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. With V_{PP} = 12 V, the Flash device resets to the Read mode when V_{CC} rises above 2 V.

Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the set-up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The set-up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the set-up Program state or not.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-system

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F512 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code 25H (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
Ceramic Packages	– 65°C to +150°C
Plastic Packages	– 65°C to +125°C
Ambient Temperature with Power Applied	– 55°C to + 125°C
Voltage with Respect To Ground	
All pins except A_9 and V_{PP} (Note 1)	– 2.0 V to 7.0 V
V_{CC} (Note 1)	– 2.0 V to 7.0 V
A_9 (Note 2)	– 2.0 V to 14.0 V
V_{PP} (Note 2)	– 2.0 V to 14.0 V
Output Short Circuit Current (Note 3)	200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A_9 and V_{PP} pins is –0.5V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

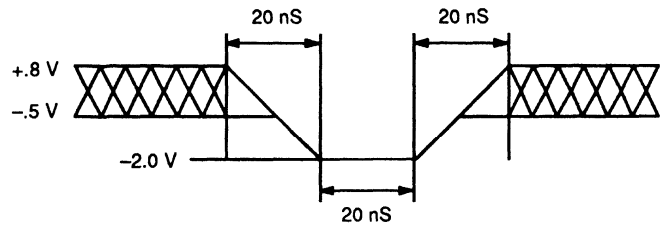
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (Tc)	0°C to +70°C
Industrial (I) Devices	
Case Temperature (Tc)	– 40°C to +85°C
Extended (E) Devices	
Case Temperature (Tc)	– 55°C to +125°C
Military (M) Devices	
Case Temperature (Tc)	– 55°C to +125°C
V_{CC} Supply Voltages	
V_{CC} for Am28F512–X5	+ 4.75 V to +5.25 V
V_{CC} for Am28F512–XX0	+ 4.50 V to +5.50 V
V_{PP} Supply Voltages	
Read	– 0.5 V to +12.6 V
Program, Erase, and Verify	+ 11.4 V to +12.6 V

MAXIMUM OVERSHOOT

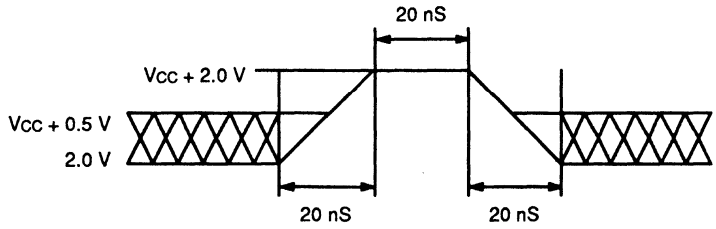
Maximum Negative Input Overshoot



11561-009A

Maximum Negative Overshoot Waveform

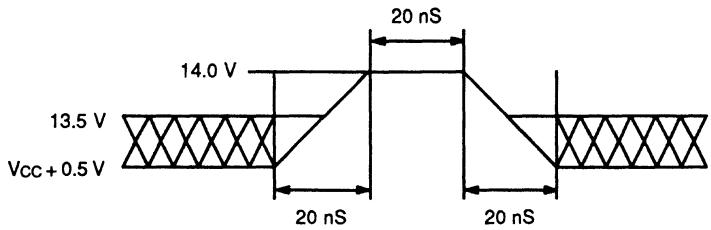
Maximum Positive Input Overshoot



11561-010A

Maximum Positive Overshoot Waveform

Maximum V_{PP} Overshoot



11561-011A

Maximum V_{PP} Overshoot Waveform

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted). (Notes 1–3)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

PRELIMINARY					
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min.**	**Max.**	**Unit**
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or Vss		± 1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or Vss		± 1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{IH}		1.0	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}		± 1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH} V_{PP} = V_{PPL}		200 ± 1.0	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA V_{CC} = V_{CC} Min.	2.4		V
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

DC CHARACTERISTICS-CMOS COMPATIBLE

PRELIMINARY					
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min.**	**Max.**	**Unit**
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ± 0.5 V		100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}		±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85 V_{CC}		V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC} –0.4		
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/ Program are inhibited when V_{PP} = V_{PPL}	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

Notes:

1. **Caution:** the Am28F512 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS-Read Only Operation (Notes 1– 2)

PRELIMINARY

Parameter Symbols				Am28F512				
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	Unit
t_{AVAV}	t_{RC}	Read Cycle Time	Min. Max.	90	120	150	200	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	90	120	150	200	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	90	120	150	200	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min. Max.	35	50	75	75	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	Min. Max.	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z	Min. Max.	25	30	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	Min. Max.	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z	Min. Max.	25	30	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	Min. Max.	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min. Max.	6	6	6	6	µs
t_{VCS}		Vcc Set-up Time to Valid Read	Min. Max.	50	50	50	50	µs

Notes:

1. Output Load (except Am28F512-95): 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: ≤ 10 ns, Input Pulse levels: 0.45 to 2.4 V, Timing Measurement Reference Level - Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F512-95 Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. t_{VCS} is guaranteed by design not tested.

AC CHARACTERISTICS-Write/Erase/Program Operations (Notes 1– 4)

PRELIMINARY								
Parameter Symbols				Am28F512				
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	Min. Max.	90	120	150	200	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min. Max.	45	50	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation	Min. Max.	10 25	10 25	10 25	10 25	µs
t_{WHWH2}		Duration of Erase Operation	Min. Max.	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	ms
t_{EHVP}		Chip Enable Set-Up Time to V_{PP} Ramp	Min. Max.	100	100	100	100	ns
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	Min. Max.	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable Low	Min. Max.	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH}	Min. Max.	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL}	Min. Max.	500	500	500	500	ns

Notes:

1. Read timing characteristics during read/write operations are the same as durng read-only operations. Refer to AC Characteristics for Read Only operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
3. All devices except Am28F512-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
4. Am28F512-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V

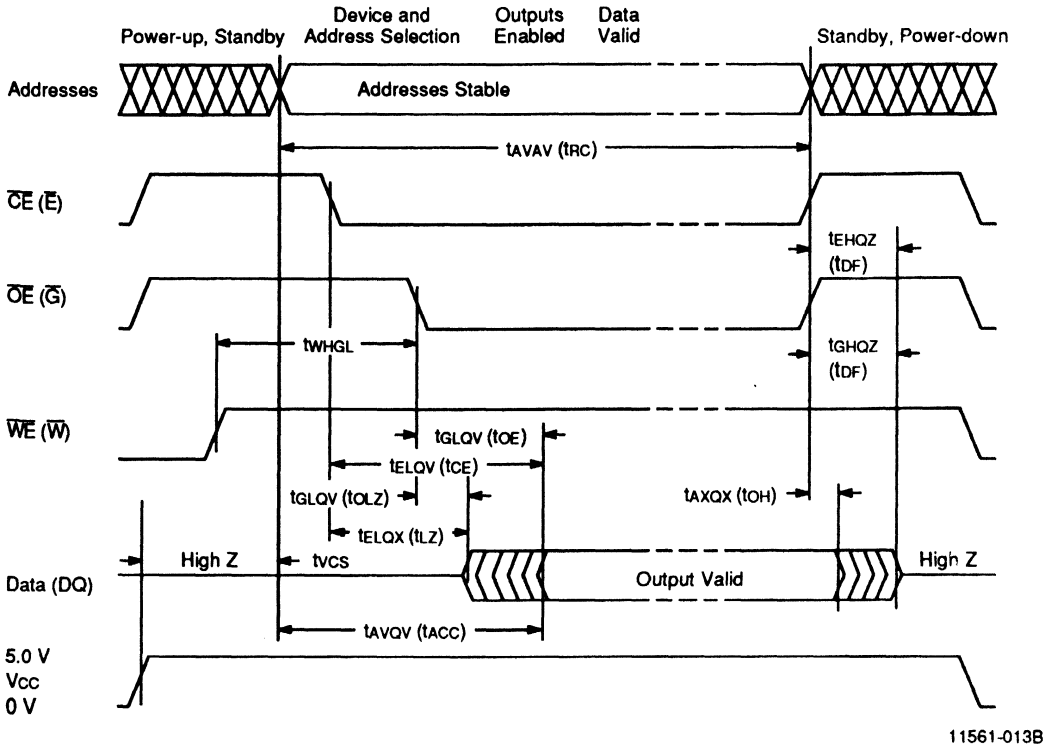


Figure 5. AC Waveforms for Read Operations

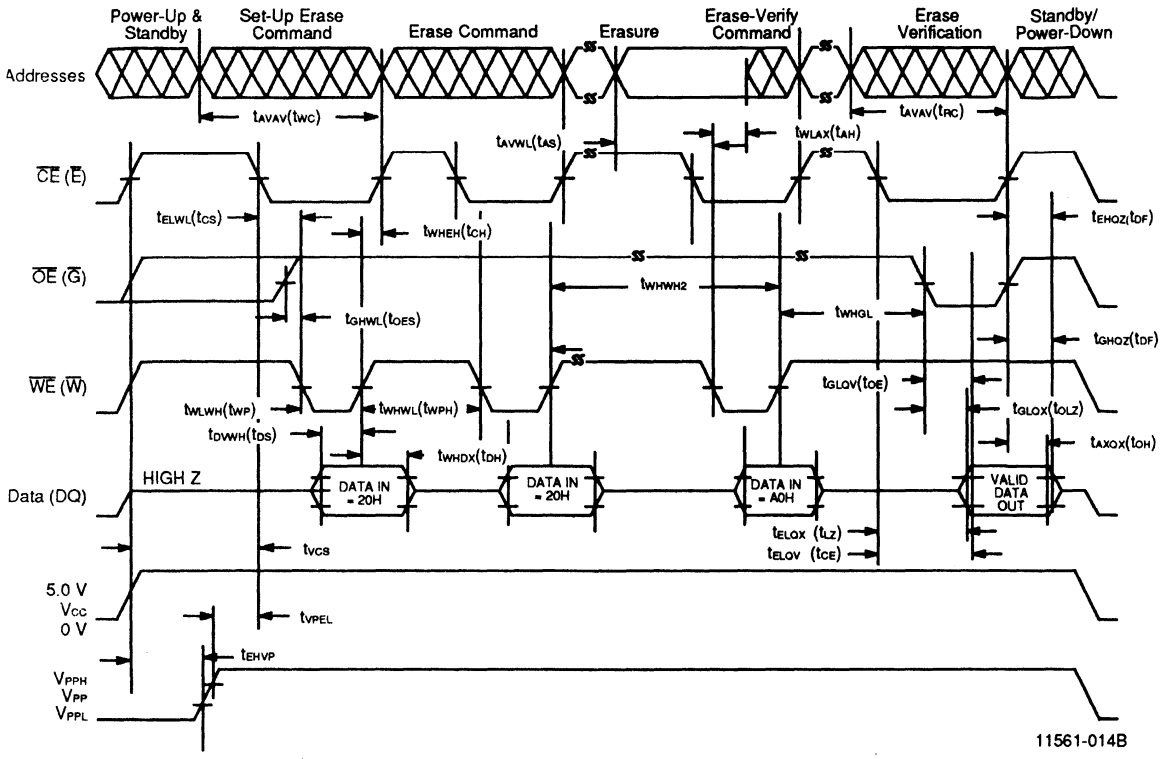


Figure 6. AC Waveforms for Erase Operations

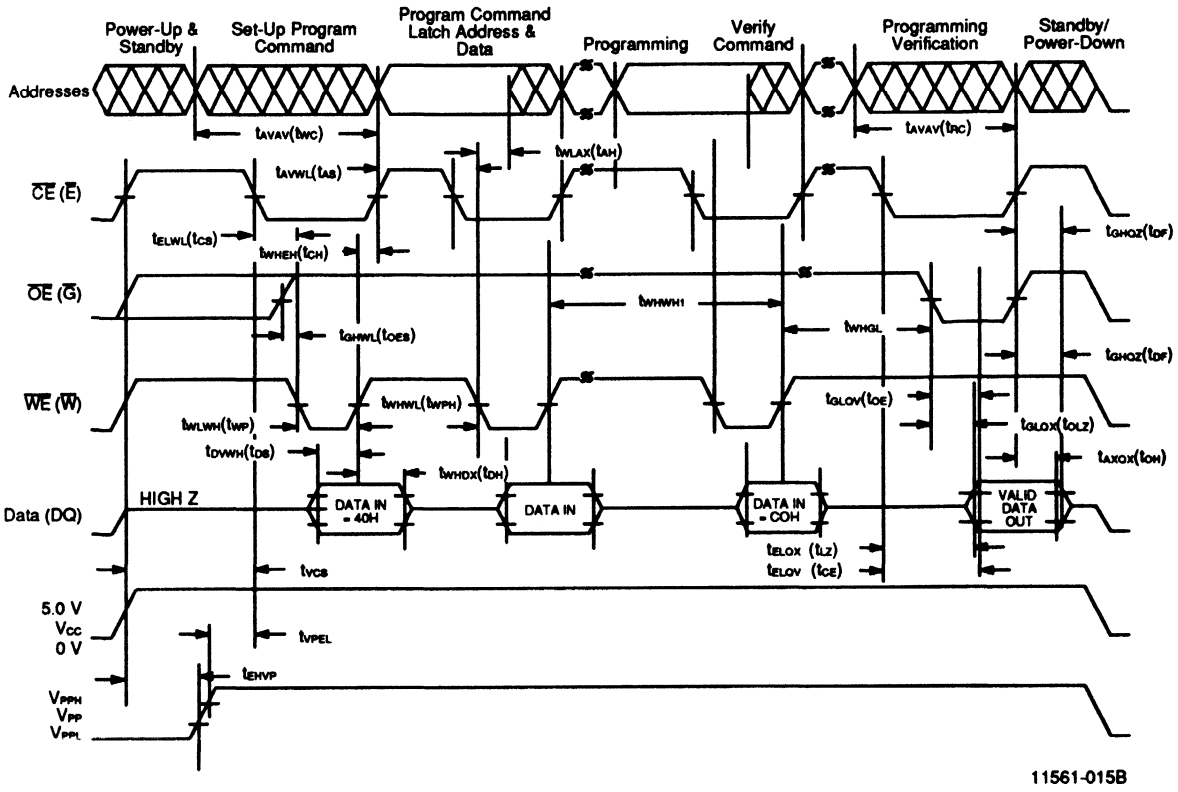
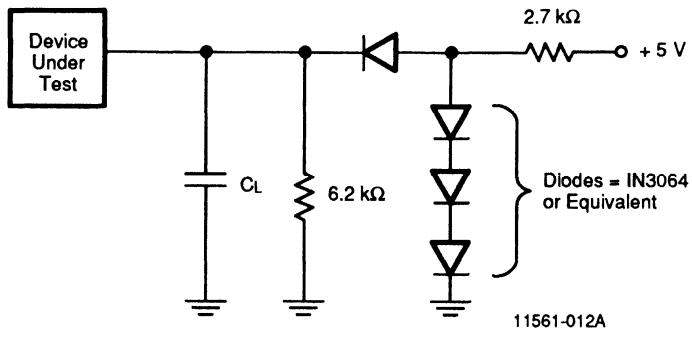


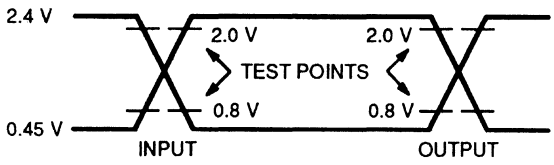
Figure 7. AC Waveforms for Programming Operations

SWITCHING TEST CIRCUIT



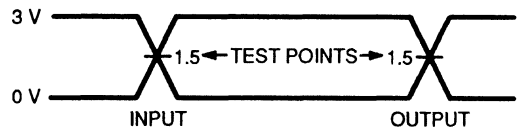
C_L = 100 pF including jig capacitance (30 pF for Am28F512-95)

SWITCHING TEST WAVEFORMS



All Devices Except Am28F512-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.



For Am28F512-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

08007-003A

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Chip Erase Time		0.5 (Note 1)	10	S	Excludes 00H programming prior to erasure
Chip Programming Time		1 (Note 1)	12	S	Excludes system-level overhead
Erase/Program Cycles					
Am28F512-95C4JC	10,000			Cycles	
Am28F512-95C3JC	1,000			Cycles	

Note:

1. 25°C, 12 V V_{PP}.

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	−1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	−1.0 V	V_{CC} + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

Preliminary

Am28F010

131,072 x 8-Bit CMOS Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
- **Compatible with JEDEC-standard byte-wide pinouts**
  - 32-Pin DIP
  - 32-Pin PLCC
  - 32-Pin TSOP
- **10,000 erase/program cycles**
- **Program and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Flasherase™ Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite™ Programming**
  - 10 µs typical byte-program
  - Less than 2 seconds typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell

GENERAL DESCRIPTION

The Am28F010 is a 1 Megabit "Flash" electrically erasable, electrically programmable read only memory organized as 128K bytes of 8 bits each. The Am28F010 is packaged in 32-Pin PDIP and PLCC versions which allow for upgrades to the 2 Megabit density. The device is also offered in ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F010 offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F010 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F010 uses a command register to manage this functionality, while maintaining a standard 32-Pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F010 uses a 12.0 V ±5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to Vcc+1 V.

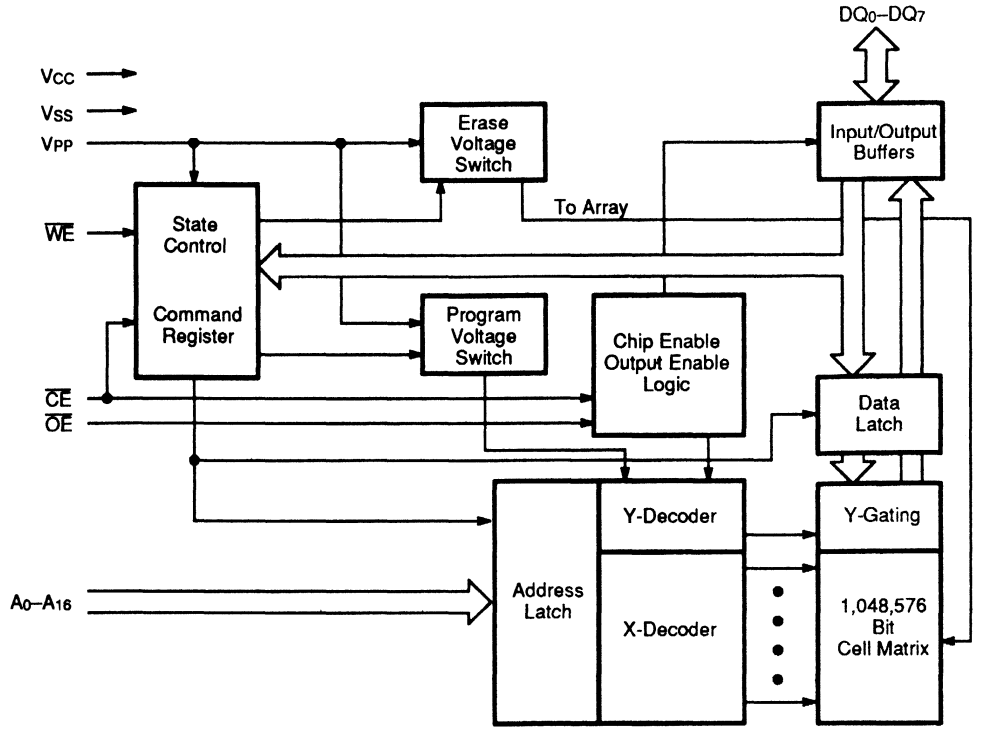
The Am28F010 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F010 is less than two seconds. The entire chip is bulk erased using 10ms erase pulses according to AMD's Flasherase algorithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM erasure using ultraviolet light are eliminated.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F010 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and E²PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F010 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Publication# 11559 Rev. C Amendment/0
Issue Date: March 1991

BLOCK DIAGRAM



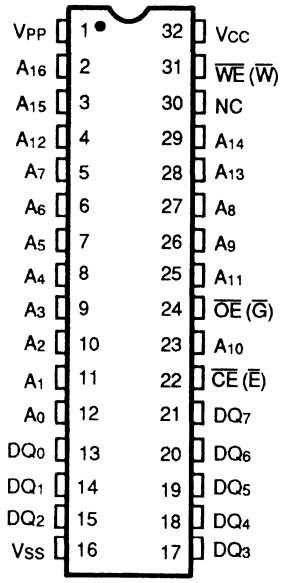
11561-001B

PRODUCT SELECTOR GUIDE

Family Part No.	Am28F010			
Ordering part No:				
± 10% Vcc Tolerance	-90	-120	-150	-200
± 5% Vcc Tolerance	-95	—	—	—
Max Access Time (ns)	90	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	75	75

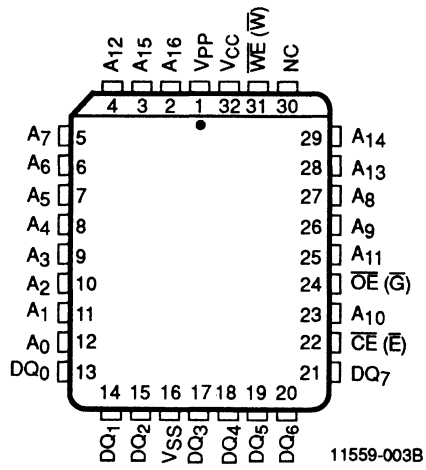
CONNECTION DIAGRAMS

DIP



11559-002B

PLCC*

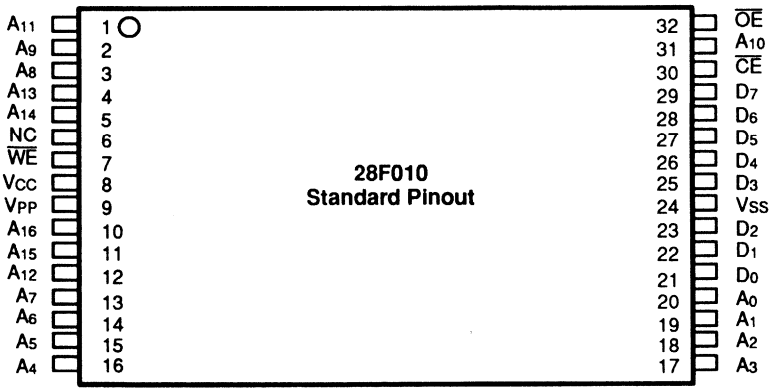


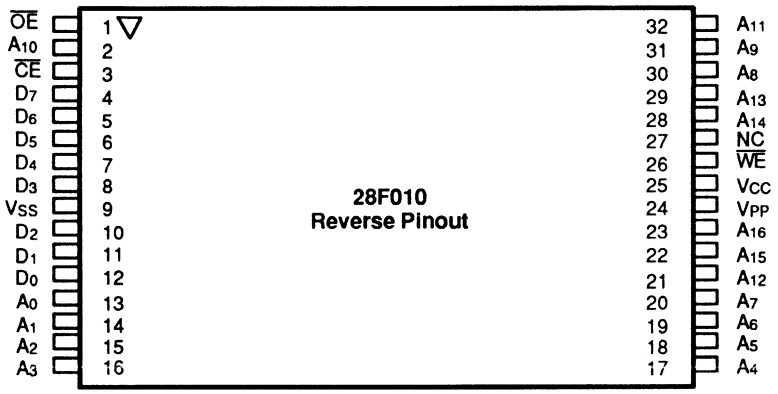
11559-003B

Note: Pin 1 is marked for orientation.

* Also available in LCC.

TSOP PACKAGES*

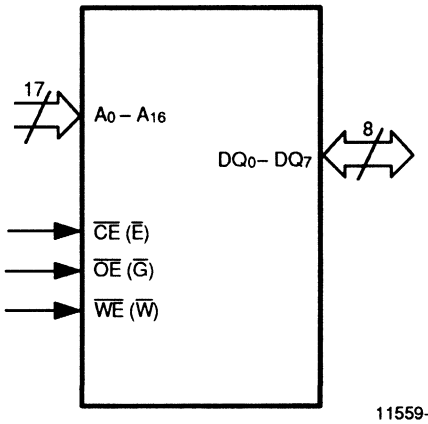




* In development

11559-005A

LOGIC SYMBOL

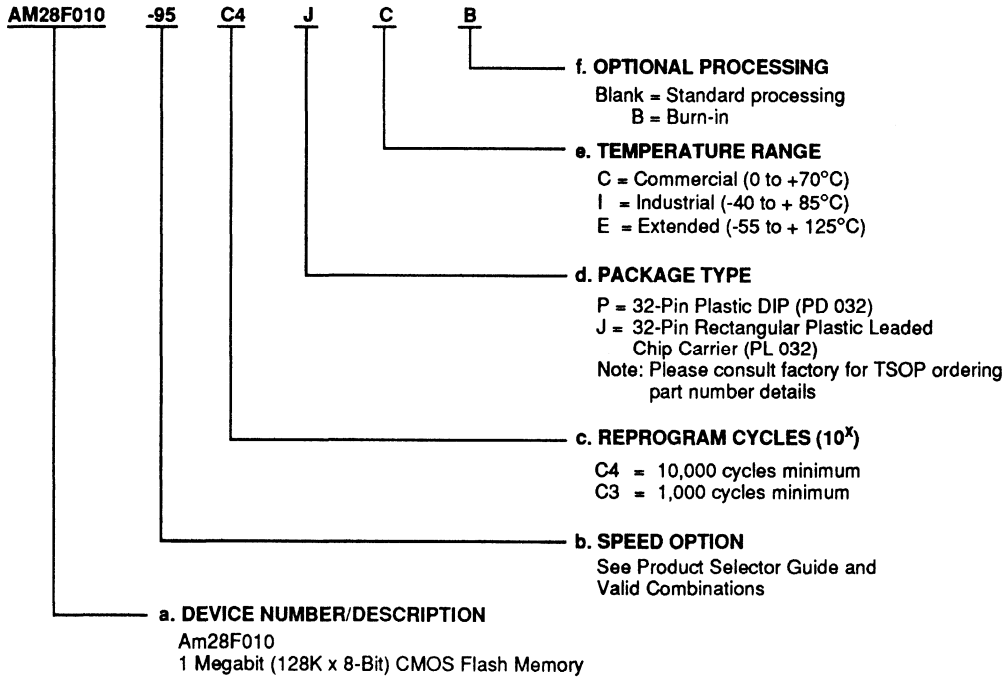


11559-004A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram Cycles
d. Package Type
e. Temperature Range
f. Optional Processing



Valid Combinations	
AM28F010-90 AM28F010-95	C4PC, C4PI, C4PCB, C4PIB, C4JC, C4JI, C4JCB, C4JIB, C3PC, C3PI, C3PCB, C3PIB, C3JC, C3JI, C3JCB, C3JIB
AM28F010-120 AM28F010-150 AM28F010-200	C4PC, C4PI, C4JC, C4JI, C4PCB, C4PIB, C4JCB, C4JIB, C4PE, C4PEB, C4JE, C4JEB, C3PC, C3PI, C3JC, C3JI, C3PCB, C3PIB, C3JCB, C3JIB, C3PE, C3PEB, C3JE, C3JEB

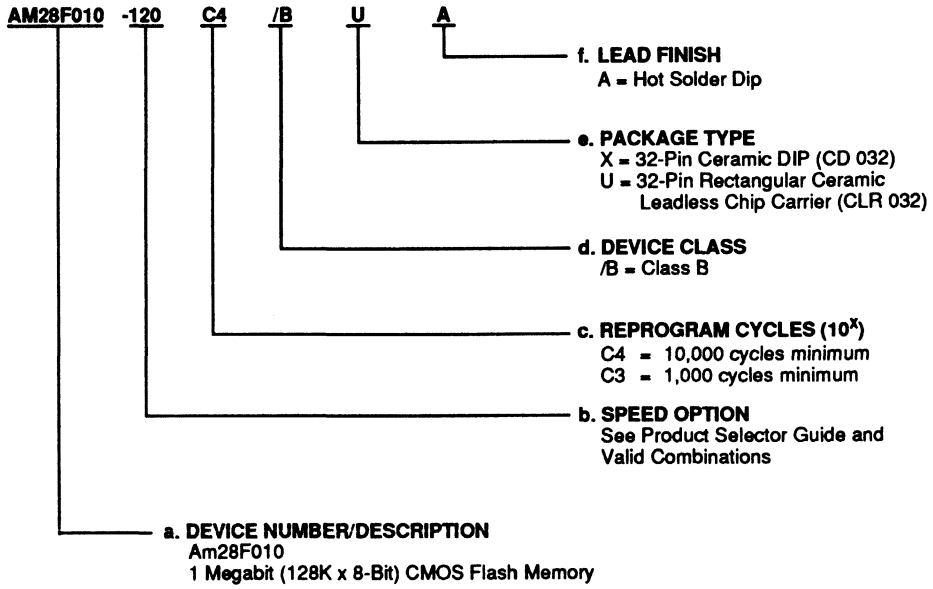
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram cycles
d. Device Class
e. Package Type
f. Lead Finish



Valid Combinations	
AM28F010-120	C4/BXA, C4/BUA C3/BXA, C3/BUA
AM28F010-150	
AM28F010-170	
AM28F010-200	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

$A_0 - A_{16}$

Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$DQ_0 - DQ_7$

Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

$\overline{CE}$ ($\overline{E}$)

The Chip Enable active low input activates the chip'scontrol logic and input buffers. Chip Enable high deselects the device and operates the chip in stand-by mode.

$\overline{OE}$ ($\overline{G}$)

The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

$\overline{WE}$ ($\overline{W}$)

The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

V_{PP}

Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2V$.

V_{CC}

Power supply for device operation. ($5.0V \pm 5\%$ or 10%)

V_{SS}

Ground

NC

No Connect-corresponding pin is not connected internally to the die.

BASIC PRINCIPLES

The Am28F010 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F010 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F010's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F010 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Erase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase Algorithm.

1. **Set-up Erase:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command.
3. **Erase-verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Set-up Program:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command.
3. **Program-verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

FUNCTIONAL DESCRIPTION
Description Of User Modes

Table 1. Am28F010 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (A7H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:
X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2V$, See DC Characteristics for voltage levels of V_{PPH}, $0V < An < V_{CC} + 2V$, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC} + 2.0V$. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0V$
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2V$

Command Register Inactive

Read

The Am28F010 functions as a read only memory when $V_{PP} < V_{CC} + 2V$. The Am28F010 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F010 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5V$), consumes less than 100µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A Prom Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5V to 13.0V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0V$ while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F010 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F010 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	A7	1	0	1	0	0	1	1	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits R_7 – R_0 correspond to the data inputs DQ_7 – DQ_0 (Refer to Table 3). Register bits R_7 – R_5 store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H or 80H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands (Notes 1, 2)	X	X	X	X	X	X	X	X

Notes:

1. See Table 4 Am28F010 Command Definitions
2. X = Appropriate Data or Register Commands

Table 4. Am28F010 Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Notes 6, 7)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/A7H
Set-up Erase/Erase (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 7)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Wait 6 µs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.
7. Please refer to Reset Command section on page 19.

Erase Sequence

Set-up Erase/Erase Commands

Set-up Erase

Set-up Erase is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Set-up Erase operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.

Erase-verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F010 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte in

the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Set-up Erase/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:

The erase-verify command must be written to the register in order to terminate the erase operation. During the erase operations, the local microprocessor must be dedicated to run software timing routines (erase in 10ms) as specified in AMD's Flasherase algorithm.

Should a system interrupt occur during an erase operation, always write the Erase-verify command prior to executing an interrupt sequence.

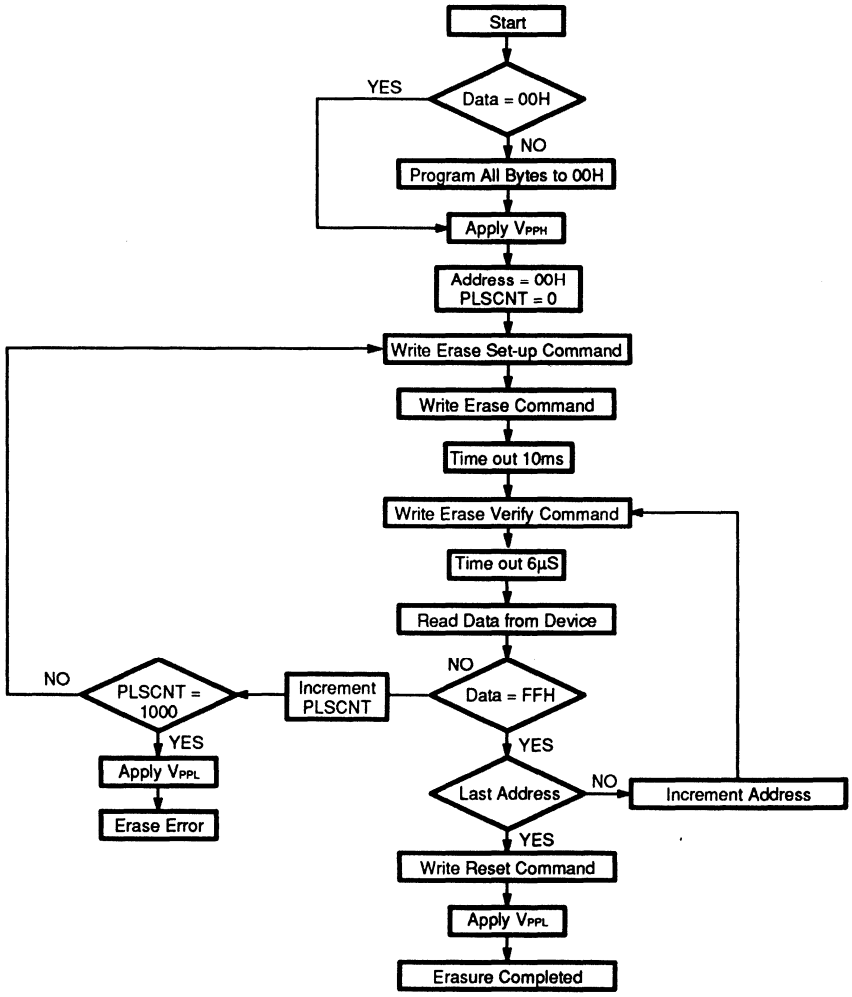


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Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F010 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

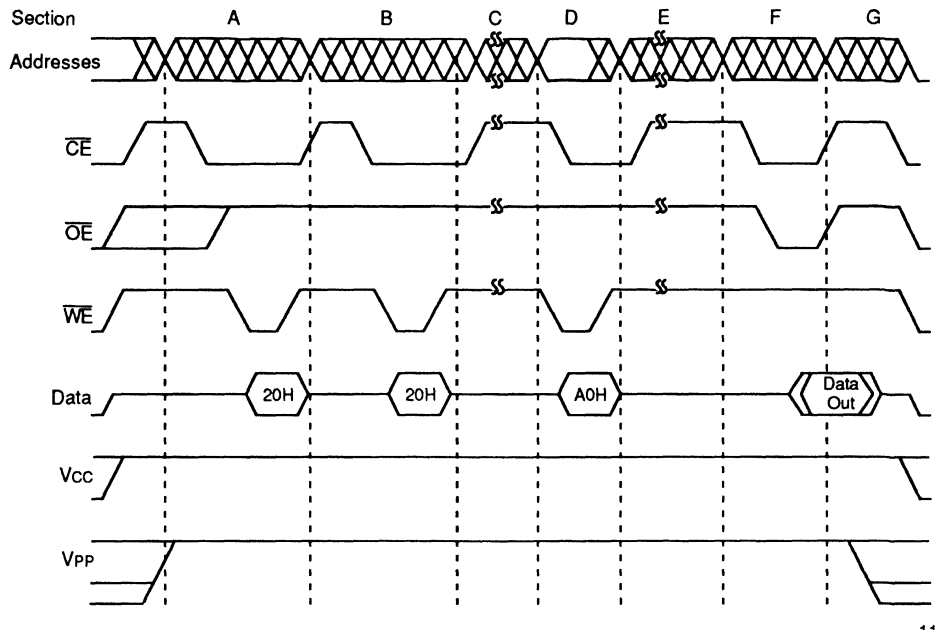
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (1 second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase operations are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. Erasure typically occurs in one second. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 2) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Set-Up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Set-up Erase	Erase	Erase (10ms)	Erase-verify	Transition (6µs)	Erase verification	Stand by & Vcc Power down

Figure 2. A.C. Waveforms For Erase Operations

Analysis Of Erase Timing Waveform

Note:
This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flasherase algorithm.

Set-up Erase/Erase

This analysis illustrates the use of two-cycle erase commands (section A&B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-out

A software timing routine (10ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Erase-verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Notes:

1. All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.

2. The erase verify command must be written to terminate the erase operation. Should a system interrupt occur during an erase operation, always write the erase-verify command prior to executing an interrupt sequence.

Programming Sequence

Set-up Program/Program Command

Set-up Program

The Am28F010 is programmed byte by byte. Bytes may be programmed sequentially or at random. Set-up Program is the first of a two-cycle program command. It stages the device for byte programming. The Set-up Program operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F010 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Set-up Program/Program). Figure 3 and Table 6 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F010 Flashrite programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the programming algorithm.

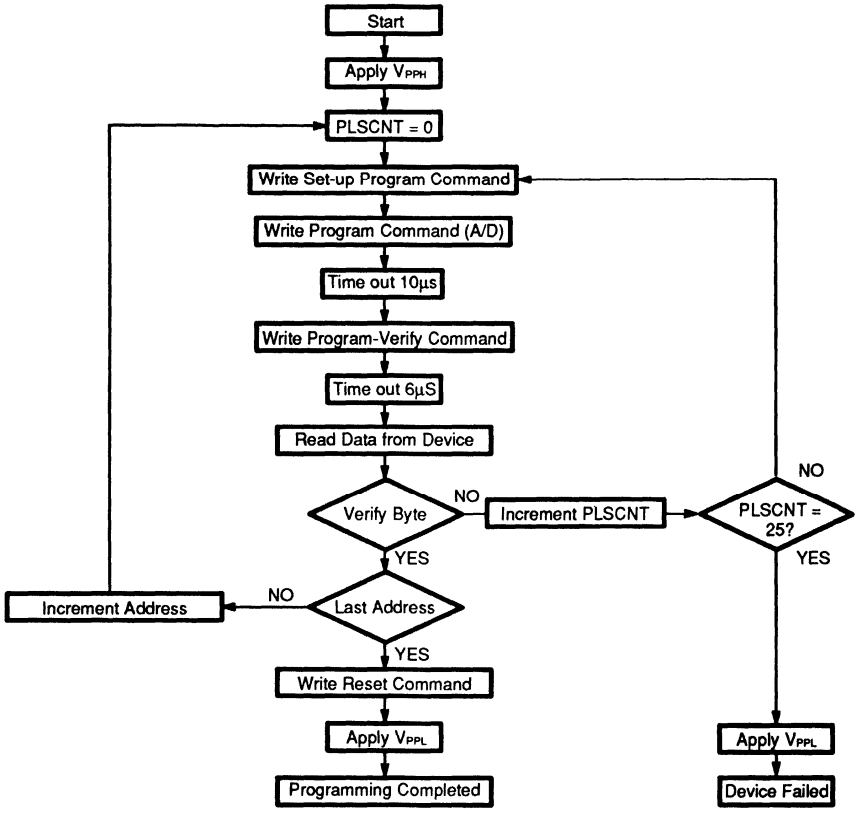


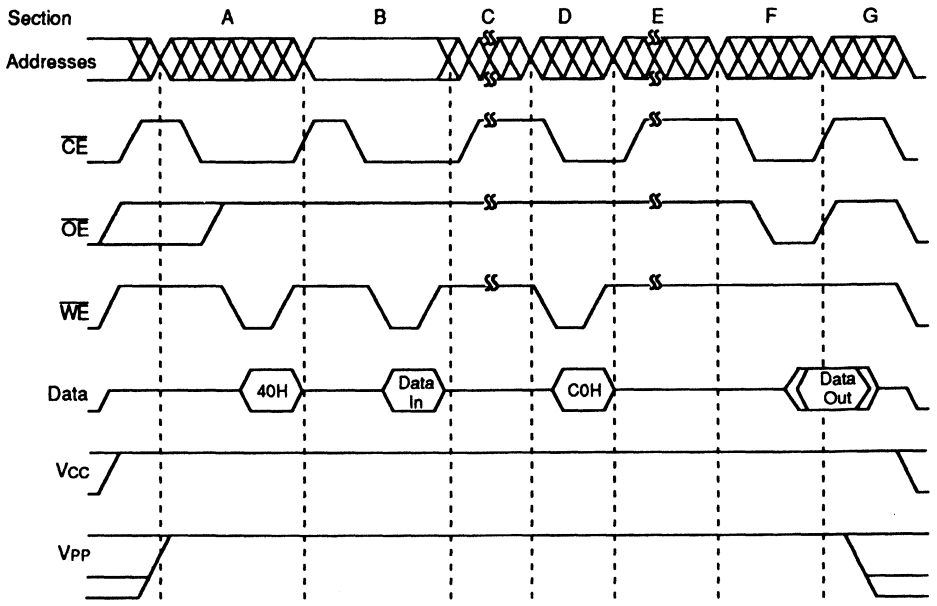
Figure 3. Flashrite Programming Algorithm

Table 6. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Set-up Program	Program Command Latch Address & Data	Program (10µs)	Program verify	Transition (6µs)	Program verification	Stand by & Vcc Power down

Figure 4. A.C. Waveforms for Programming Operations

Analysis Of Program Timing Waveforms

Set-up Program/Program

Two-cycle write commands are required for program operations (section A&B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-out

A software timing routine (10µs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Program-verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address js programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Note:
The program-verify operation must be written to terminate the programming operation. Should a system interrupt occur during a programming operation, always write the program-verify command prior to executing an interrupt sequence.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1µF/device. V_{PP} must reach its final value 100ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse, or the device may continue to erase until the memory cells are driven into depletion (over-erasure). Should this happen the internal circuitry will no longer select unique addresses. A symptom of over-erasure is an error attempting to program the next time. Occasionally it is possible to recover over-erased devices by programming all of the locations with 00H data.
3. A third delay time is required for each programming pulse width (10 µs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 µs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:
Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified seperately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-up Sequence

V_{CC} Prior to V_{PP}

The Am28F010 powers-up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two step command sequence.

V_{PP} Prior to V_{CC}

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. With V_{PP} = 12 V, the Flash device resets to the Read mode when V_{CC} rises above 2 V.

Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the set-up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The set-up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the set-up Program state or not.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-system

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F010 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code A7H (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
Ceramic Packages	– 65°C to +150°C
Plastic Packages	– 65°C to +125°C
Ambient Temperature with Power Applied	– 55°C to + 125°C
Voltage with Respect To Ground	
All pins except A_9 and V_{PP} (Note 1)	– 2.0V to 7.0V
V_{CC} (Note 1)	– 2.0V to 7.0V
A_9 (Note 2)	– 2.0V to 14.0V
V_{PP} (Note 2)	– 2.0V to 14.0V
Output Short Circuit Current (Note 3)	200mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A_9 and V_{PP} pins is –0.5V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

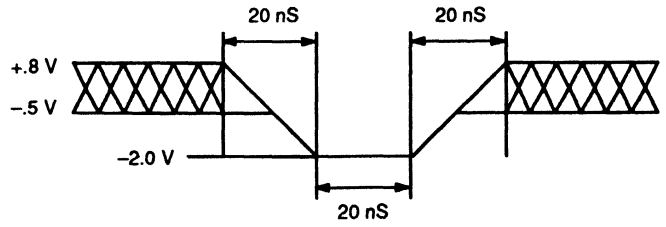
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (Tc)	0°C to +70°C
Industrial (I) Devices	
Case Temperature (Tc)	– 40°C to +85°C
Extended (E) Devices	
Case Temperature (Tc)	– 55°C to +125°C
Military (M) Devices	
Case Temperature (Tc)	– 55°C to +125°C
V_{CC} Supply Voltages	
V_{CC} for Am28F010–X5	+ 4.75V to +5.25V
V_{CC} for Am28F010–XX0	+ 4.50V to +5.50V
V_{PP} Supply Voltages	
Read	– 0.5V to +12.6V
Program, Erase, and Verify	+ 11.4V to +12.6V

MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



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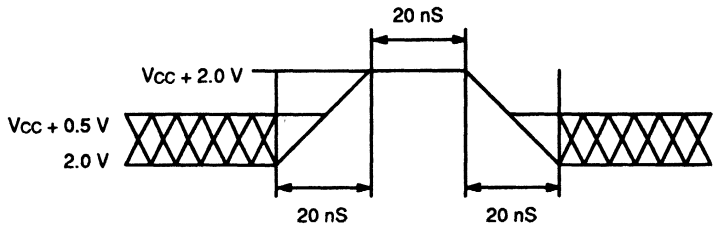
Maximum Negative Overshoot Waveform

Maximum Positive Input Overshoot



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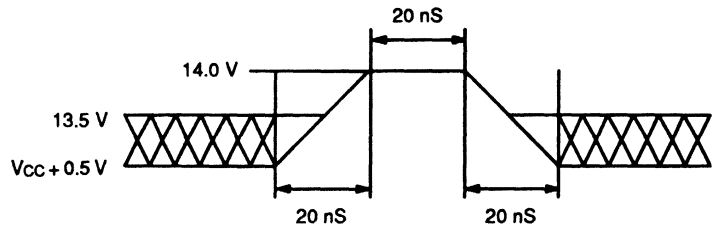
Maximum Positive Overshoot Waveform

Maximum V_{PP} Overshoot



11561-011A

Maximum V_{PP} Overshoot Waveform

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted). (Notes 1–3)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

PRELIMINARY					
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min.**	**Max.**	**Unit**
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		±1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		±1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{IH}		1.0	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}		±1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		200	µA
		V_{PP} = V_{PPL}		±1.0	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA V_{CC} = V_{CC} Min.	2.4		V
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

DC CHARACTERISTICS-CMOS COMPATIBLE

PRELIMINARY					
Parameter Symbol	**Parameter Description**	**Test Conditions**	**Min.**	**Max.**	**Unit**
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or Vss		± 1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or Vss		± 1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ± 0.5 V		100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}		± 1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85 V_{CC}		V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC} –0.4		
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/ Program are inhibited when V_{PP} = V_{PPL}	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

Notes:

1. **Caution:** the Am28F010 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	V_{PP} = 0	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions T_A = 25°C, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified.

AC CHARACTERISTICS-Read Only Operation (Notes 1– 2)

PRELIMINARY								
Parameter Symbols				Am28F010				
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	Unit
t_{AVAV}	t_{RC}	Read Cycle Time	Min. Max.	90	120	150	200	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	90	120	150	200	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	90	120	150	200	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min. Max.	35	50	75	75	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	Min. Max.	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z	Min. Max.	25	30	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	Min. Max.	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z	Min. Max.	25	30	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	Min. Max.	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min. Max.	6	6	6	6	µs
t_{VCS}		V_{CC} Set-up Time to Valid Read	Min. Max.	50	50	50	50	µs

Notes:

1. Output Load (except Am28F010-95): 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: ≤ 10 ns, Input Pulse levels: 0.45 to 2.4 V, Timing Measurement Reference Level - Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F010-95 Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. t_{VCS} is guaranteed by design not tested.

AC CHARACTERISTICS-Write/Erase/Program Operations (Notes 1– 4)

PRELIMINARY								
Parameter Symbols				Am28F010				
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	Min. Max.	90	120	150	200	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min. Max.	45	50	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation	Min. Max.	10 25	10 25	10 25	10 25	µs
t_{WHWH2}		Duration of Erase Operation	Min. Max.	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	ms
t_{EHVP}		Chip Enable Set-Up Time to V_{PP} Ramp	Min. Max.	100	100	100	100	ns
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	Min. Max.	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable Low	Min. Max.	2	2	2	2	µs
t_{VPPR}		V_{PP} Rise Time	Min. Max.	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time	Min. Max.	500	500	500	500	ns

Notes:

1. Read timing characteristics during read/write operations are the same as durng read-only operations. Refer to AC Characteristics for Read Only operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
3. All devices except Am28F010-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
4. Am28F010-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V
   Timing Measurement Reference Level: Inputs and Outputs: 1.5 V

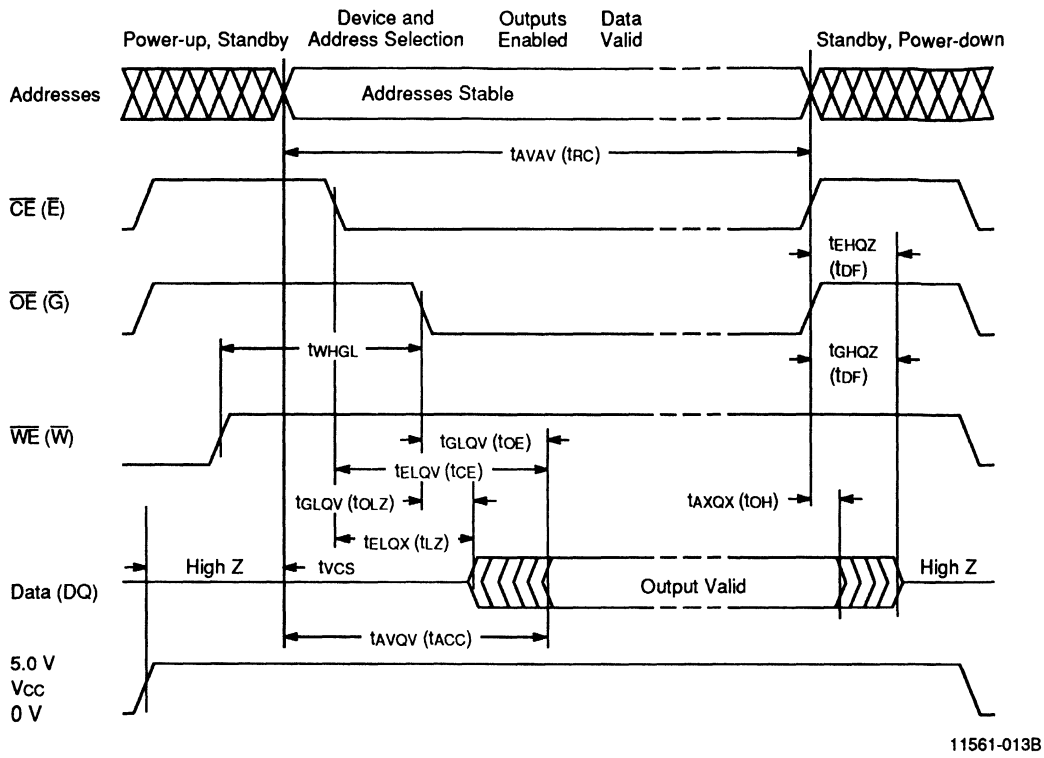


Figure 5. AC Waveforms for Read Operations

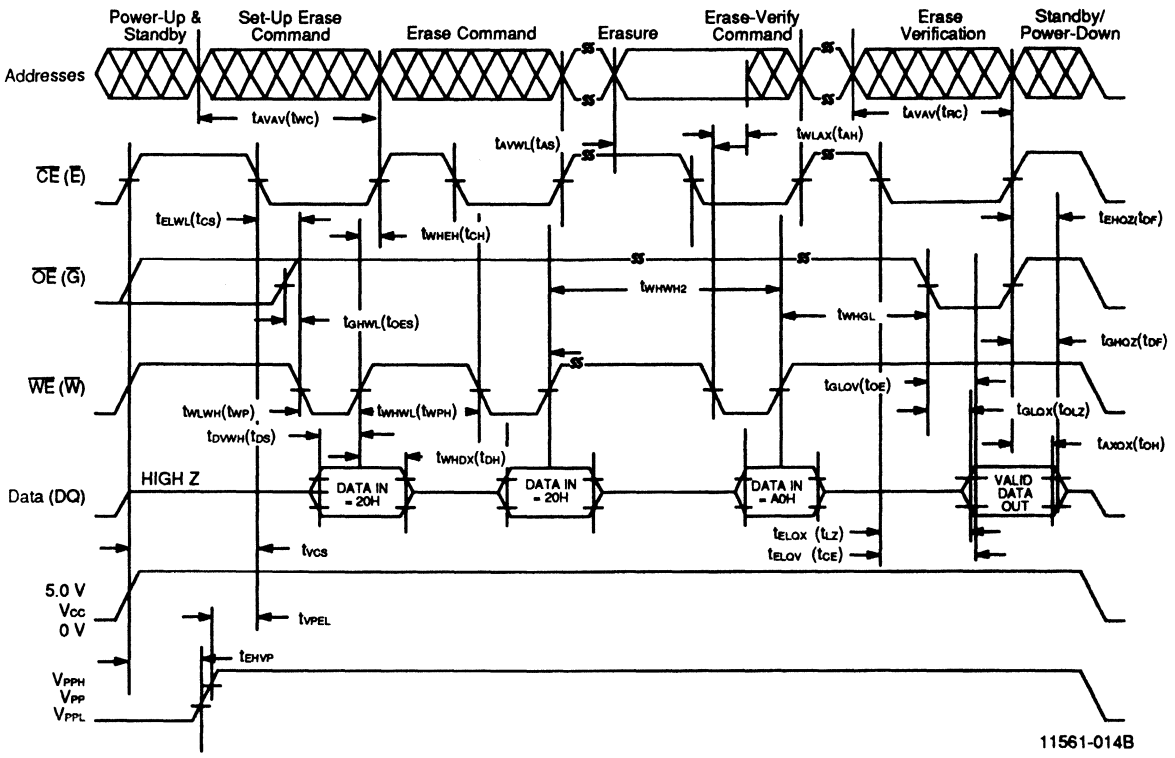


Figure 6. AC Waveforms for Erase Operations

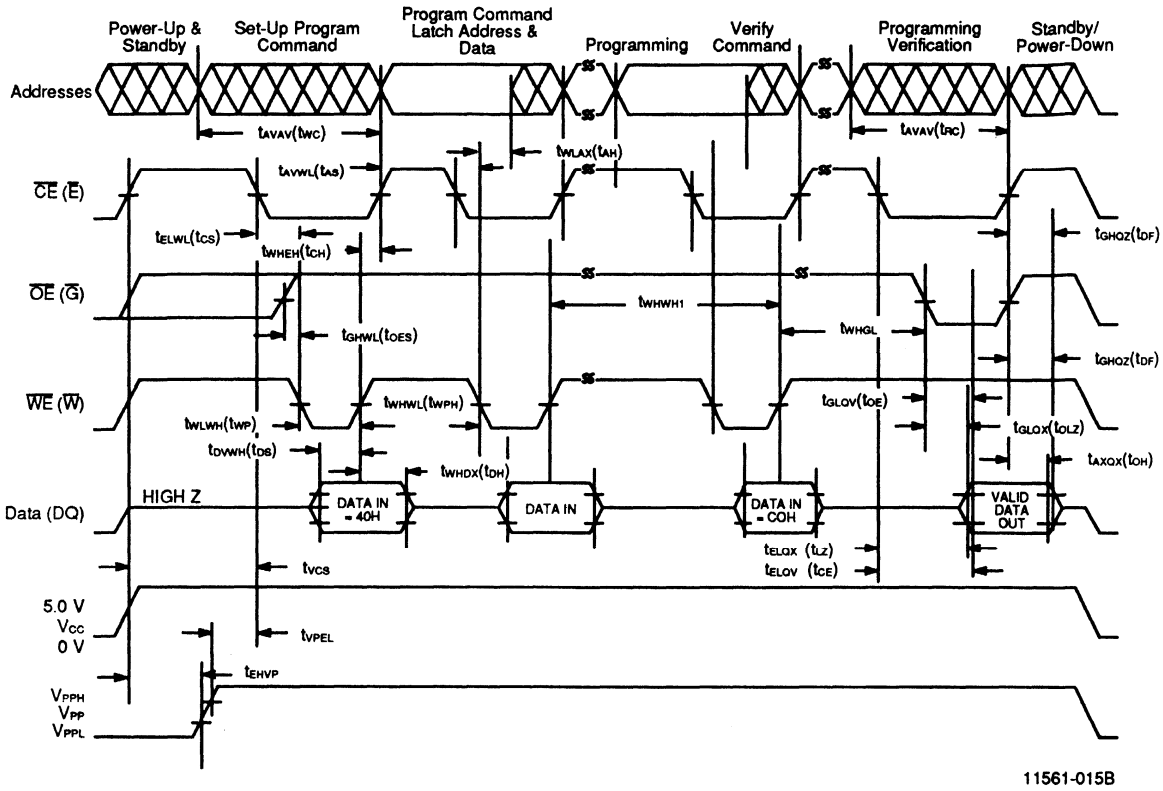
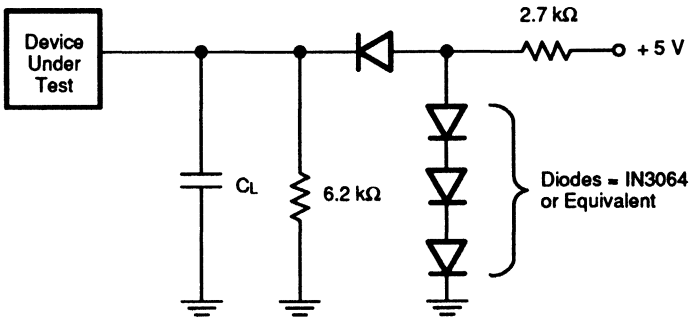


Figure 7. AC Waveforms for Programming Operations

SWITCHING TEST CIRCUIT



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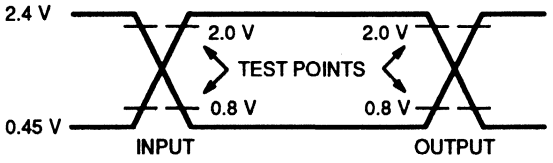
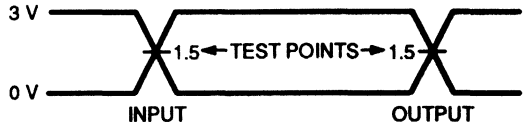
C_L = 100 pF including jig capacitance (30 pF for Am28F010-95)

SWITCHING TEST WAVEFORMS



All Devices Except Am28F010-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.



For Am28F010-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

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ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Chip Erase Time		0.5 (Note 1)	10	S	Excludes 00H programming prior to erasure
Chip Programming Time		2 (Note 1)	24	S	Excludes system-level overhead
Erase/Program Cycles					
Am28F010-95C4JC	10,000			Cycles	
Am28F010-95C3JC	1,000			Cycles	

Note:

1. 25°C, 12V V_{PP}

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	– 1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	– 1.0 V	V_{CC} + 1.0 V
Current	– 100 mA	+ 100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

Advance Information

Am28F020

262,144 x 8-Bit CMOS Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **CMOS Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
  - No Data Retention Power
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-Pin TSOP
- **10,000 erase/program cycles minimum**
- **Program and erase voltage 12.0 V +5%**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Flasherase™ or Embedded Erase™ Electrical Bulk Chip-Erase**
  - Two second typical chip-erase
- **Flashrite™ or Embedded Program™**
  - 10 µs typical byte-program
  - Less than 3 seconds typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell
- **Embedded algorithms for completely self-timed program/erase operations**
- **Automatic program/erase pulse stop timer**

GENERAL DESCRIPTION

The Am28F020 is a 2 Megabit Flash memory organized as 256K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The Am28F020 is packaged in 32-pin PDIP and PLCC versions. The device is also offered in the ceramic DIP package. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F020 offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F020 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F020 uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F020 uses a 12.0 V ± 5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to Vcc+1 V.

Embedded Program

The Am28F020 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The device may also be programmed using the Embedded Programming algorithm. The Embedded Programming algorithm does not require the system to time-out or verify the data programmed. The typical room temperature programming time of the Am28F020 is less than three seconds.

Embedded Erase

The entire chip is bulk erased using 10 ms erase pulses according to AMD's Flasherase algorithm. Typical erasure at room temperature is accomplished in less than two seconds. The device may also be erased using the Embedded Erase algorithm. The Embedded Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device.

AMD's Am28F020 is entirely pin and software compatible with existing AMD Flash memories. The availability of the Embedded Program and Erase algorithms does not preclude the use of standard Flashrite and Flasherase algorithms. Thus AMD's devices are always backwards compatible with existing designs.

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Issue Date: March 1991

Embedded Programming Algorithm vs. Flashrite Programming Algorithm

The Flashrite Programming algorithm requires the user to write a program set-up command, a program command (program data and address), and a program verify command followed by a read and compare operation. The user is required to time the programming pulse width in order to issue the program verify command. An integrated stop timer prevents any possibility of over-programming. Upon completion of this sequence the data is read back from the device and compared by the user with the data intended to be written; if there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 25 times.

AMD's Embedded Programming algorithm requires the user to only write a program set-up command and a program command (program data and address). The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, similar to data polling, provides feedback to the user as to the status of the programming operation.

Embedded Erase Algorithm vs. Flasherase Erase Algorithm

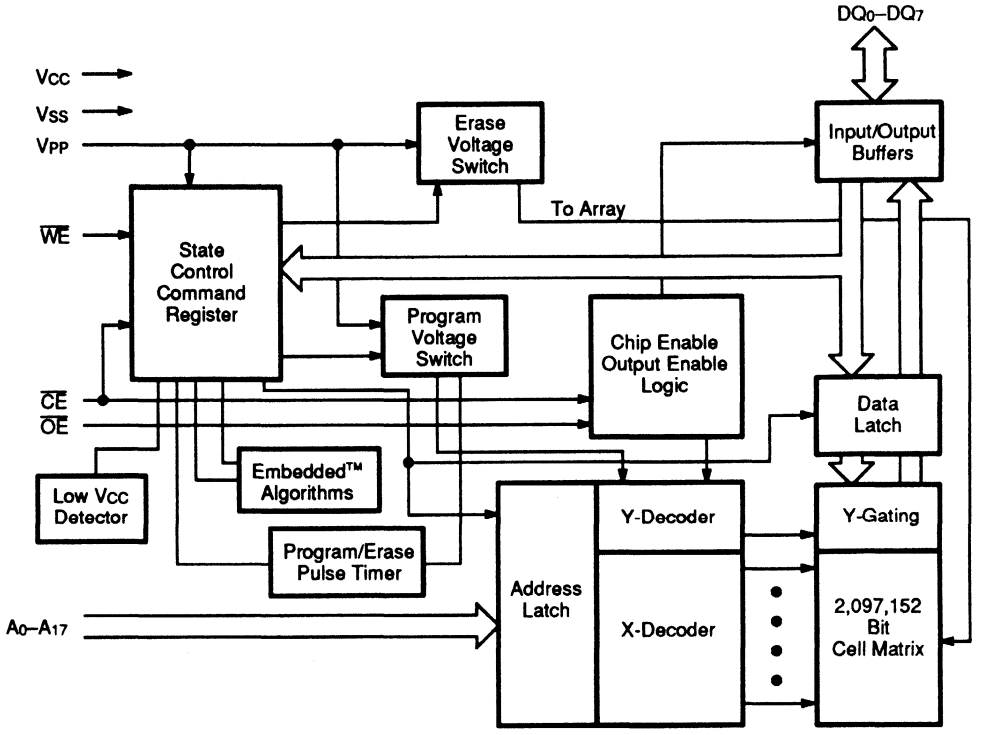
The Flasherase Erase algorithm requires the device to be completely programmed prior to executing an erase command. To invoke the erase operation the user writes an erase set-up command, an erase command, and an erase verify command. The user is required to time the erase pulse width in order to issue the erase verify command. An integrated stop timer prevents any possibility of overerasure. Upon completion of this sequence the data is read back from the device and compared by the user with erased data. If there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 1,000 times.

AMD's Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, similar to data polling, provides feedback to the user as to the status of the erase operation.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F020 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F020 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM



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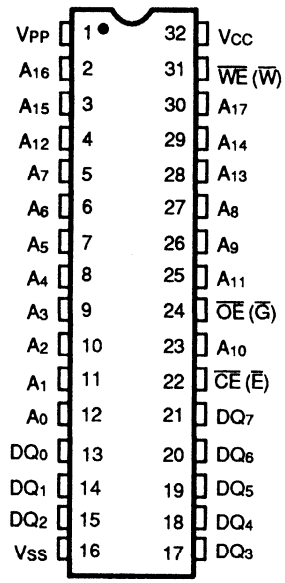
PRODUCT SELECTOR GUIDE

Family Part No.	Am28F020			
Ordering part No:				
+ 10% VCC Tolerance	-90	-120	-150	-200
+ 5% VCC Tolerance	-95			
Max Access Time (ns)	90	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	75	75

CONNECTION DIAGRAMS

DIP



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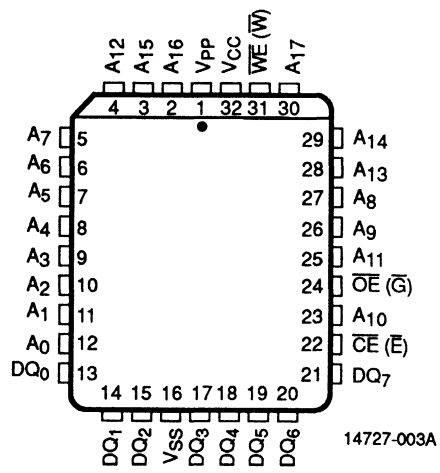
PLCC



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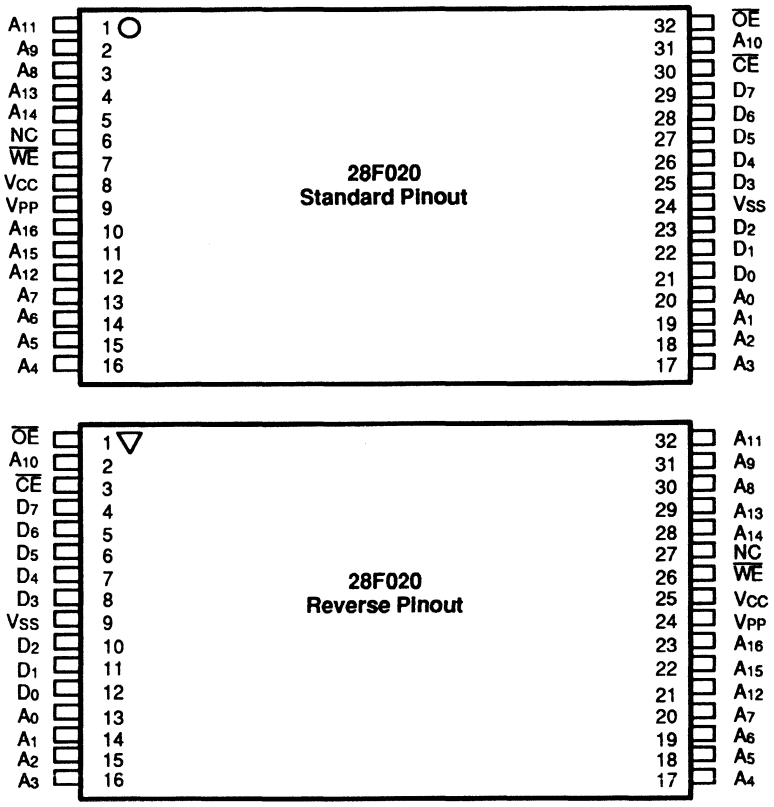
Note: Pin 1 is marked for orientation.

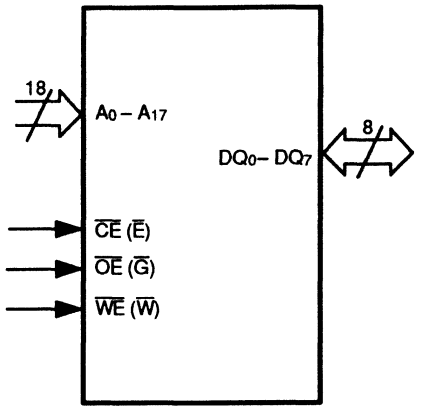
TSOP PACKAGES*



*In development

28F020 256K x 8 Flash Memory In 32 Lead TSOP

LOGIC SYMBOL

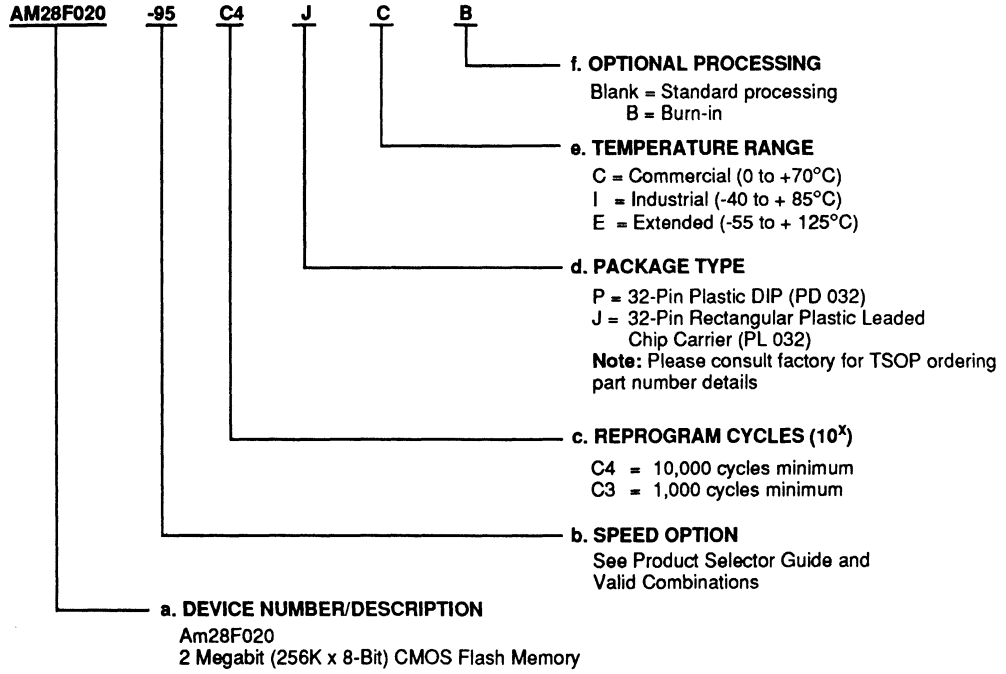


11559-004A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram Cycles
d. Package Type
e. Temperature Range
f. Optional Processing



Valid Combinations	
AM28F020-90 AM28F020-95	C4PC, C4JC, C3PC, C3JC,
AM28F020-120 AM28F020-150 AM28F020-200	C4PC, C4PI, C4JC, C4JI, C4PE, C4PEB, C4JE, C4JEB, C3PC, C3PI, C3JC, C3JI

Valid Combinations

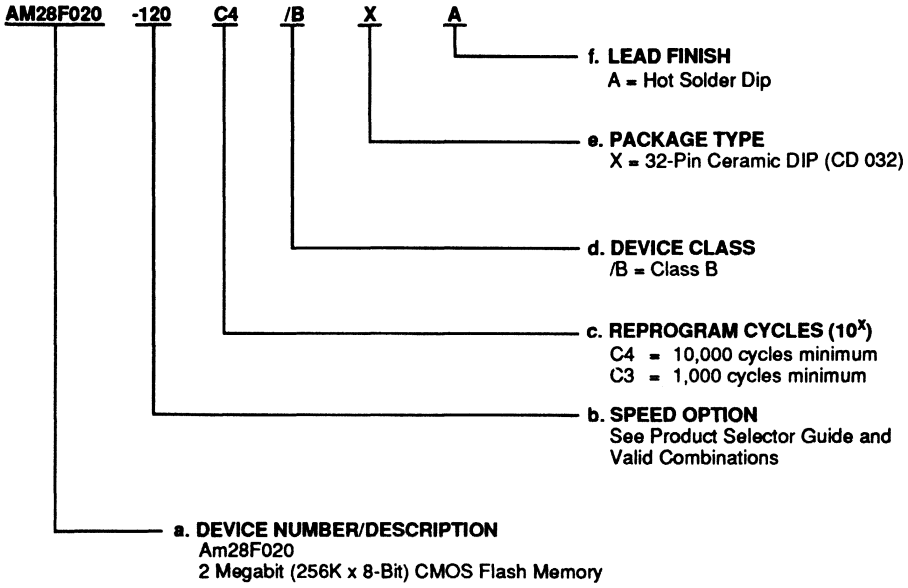
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram cycles
d. Device Class
e. Package Type
f. Lead Finish



Valid Combinations	
AM28F020-120	C4/BXA C3/BXA
AM28F020-150	
AM28F020-170	
AM28F020-200	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

V_{PP}

Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2V$.

V_{CC}

Power supply for device operation. (5.0 V + 5% or 10%)

V_{SS}

Ground

NC

No Connect-corresponding pin is not connected internally to the die.

$A_0 - A_{17}$

Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$DQ_0 - DQ_7$

Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

$\overline{CE}$ ($\overline{E}$)

The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

$\overline{OE}$ ($\overline{G}$)

The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

$\overline{WE}$ ($\overline{W}$)

The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F020 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0V + 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F020 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F020's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F020 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Flasherase™ Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase Algorithm.

1. **Set-up Erase:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command. An integrated stop timer prevents any possibility of overerasure.
3. **Erase-verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Embedded Programming Algorithm

AMD now makes programming extremely simple and reliable. The Embedded Programming algorithm requires the user to only write a program set-up command and a program command. The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, similar to $\overline{data}$ polling, provides feedback to the user as to the status of the programming operation.

Flashrite Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Set-up Program:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command. An integrated stop timer prevents any possibility of overprogramming.
3. **Program-verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

Embedded Erase Algorithm

AMD now makes erasure extremely simple and reliable. The Embedded Erase algorithm requires the user to only write and erase set-up command and erase command. The device will automatically pre-program and verify the entire array. The device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, similar to data polling, provides feedback to the user as to the status of the erase operation.

Data Write Protection

The Am28F020 is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F020 powers up in the read only state irregardless of the state of V_{PP}. If $V_{PP} = V_{PPL}$ then the device contents cannot be altered. If $V_{PP} = V_{PPH}$ the device still powers up in the read mode. In addition, the control register only allows alteration of the memory contents after successful completion of the two step write command sequence. Also, all register write commands are inhibited whenever V_{CC} is below the write lockout voltage V_{LKO}.

Noise Protection

All control pins ($\overline{CE}$, $\overline{WE}$ and $\overline{OE}$) ignore any pulse widths of less than 10 ns duration.

Power Up/Power Down Protection

To avoid initiation of an inadvertent write cycle during V_{CC} and V_{PP} power transitions, the device always powers up in the Read mode. Power supply sequencing is not required.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am28F020 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (2AH)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2V$, See DC Characteristics for voltage levels of V_{PPH}, $0V < An < V_{CC} + 2V$, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC} + 2.0V$. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0V$
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2V$

Command Register Inactive

Read

The Am28F020 functions as a read only memory when $V_{PP} < V_{CC} + 2V$. The Am28F020 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F020 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5V$), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5V to 13.0V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0V$ while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F020 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F020 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	2A	0	0	1	0	1	0	1	0

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits R_7 – R_0 correspond to the data inputs DQ_7 – DQ_0 (Refer to Table 3). Register bits R_7 – R_5 store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H or 80H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6 µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands (Notes 1, 2)	X	X	X	X	X	X	X	X

Notes:

1. See Table 4 Am28F020 Command Definitions
2. X = Appropriate Data or Register Commands

Table 4. Am28F020 Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Notes 6, 7)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/2AH
Set-up Erase/Erase (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Embedded Set-up Erase/ Embedded Erase	Write	X	30H	Write	X	30H
Embedded Set-up Program/ Embedded Program	Write	X	50H	Write	PA	PD
Reset (Note 7)	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Wait 6 µs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.
7. Please reference Reset Command section on page 5–110.

FLASH MEMORY PROGRAM/ERASE OPERATIONS

Section I: Details AMD's Flasherase and Flashrite Algorithms

Section II: Details AMD's Embedded Program and Erase Operations

Section I: Details AMD's Flasherase and Flashrite Algorithms

Flasherase Erase Sequence

Set-up Erase/Erase Commands

Set-up Erase

Set-up Erase is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Set-up Erase operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{pp} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:

The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.

Erase-verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F020 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte in the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Set-up Erase/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

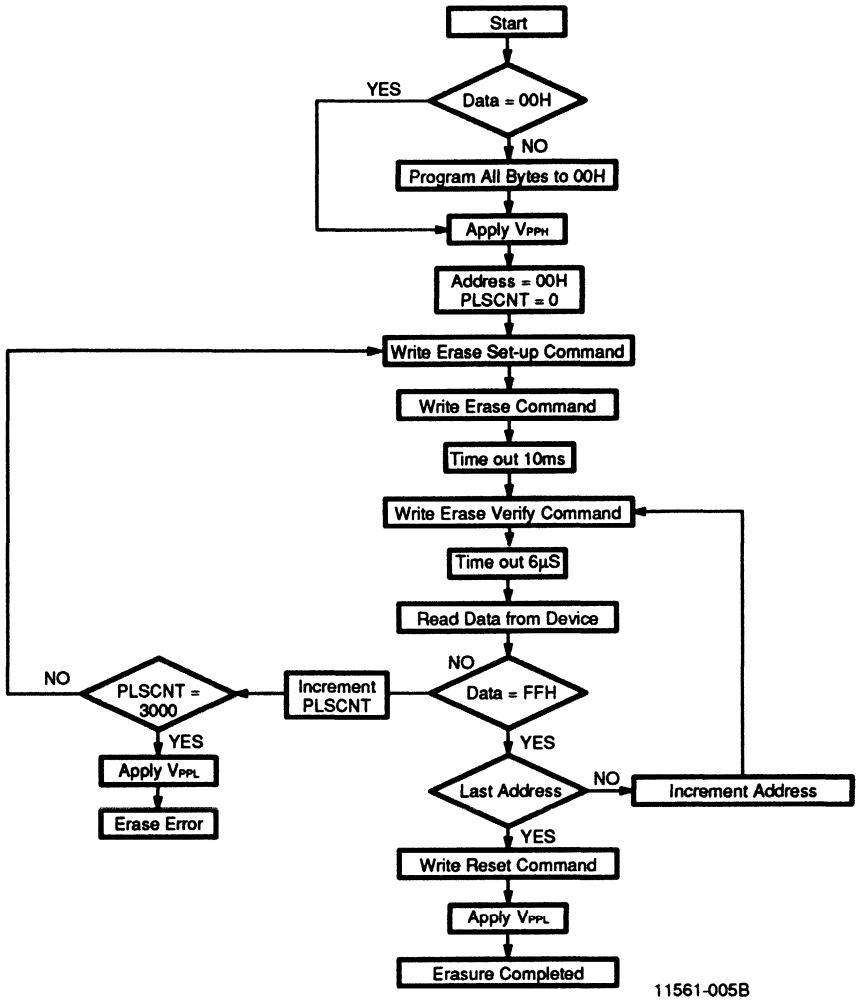


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F020 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

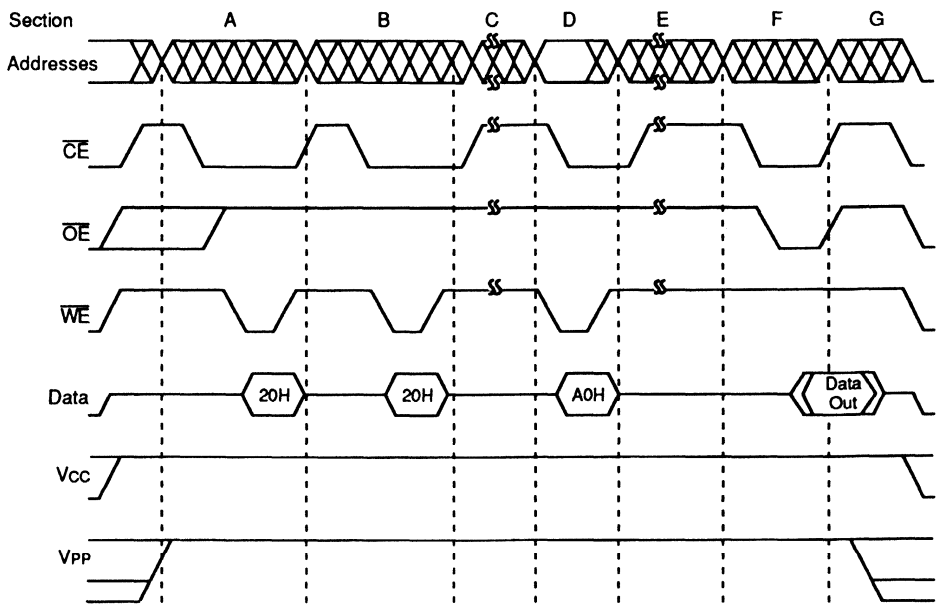
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite Programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 200 pulses (2 seconds). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase operations are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. Erasure typically occurs in one second. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 2) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Set-Up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Set-up Erase	Erase	Erase (10ms)	Erase-verify	Transition (6µs)	Erase verification	Stand by & Vcc Power down

Figure 2. A.C. Waveforms For Erase Operations

Analysis of Erase Timing Waveform

Note:
This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flasherase algorithm.

Set-up Erase/Erase

This analysis illustrates the use of two-cycle erase commands (section A & B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-out

A software timing routine (10 ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B. An integrated stop timer prevents any possibility of over-erasure.

Note:
An integrated stop timer prevents any possibility of over-erasure.

Erase-verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 200 erase pulses are required.

Notes:

1. All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.

Flashrite Programming Sequence

Set-up Program/Program Command

Set-up Program

The Am28F020 is programmed byte by byte. Bytes may be programmed sequentially or at random. Set-up Program is the first of a two-cycle program command. It stages the device for byte programming. The Set-up Program operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F020 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Set-up Program/Program). Figure 3 and Table 6 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F020 Flashrite Programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite Programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the programming algorithm.

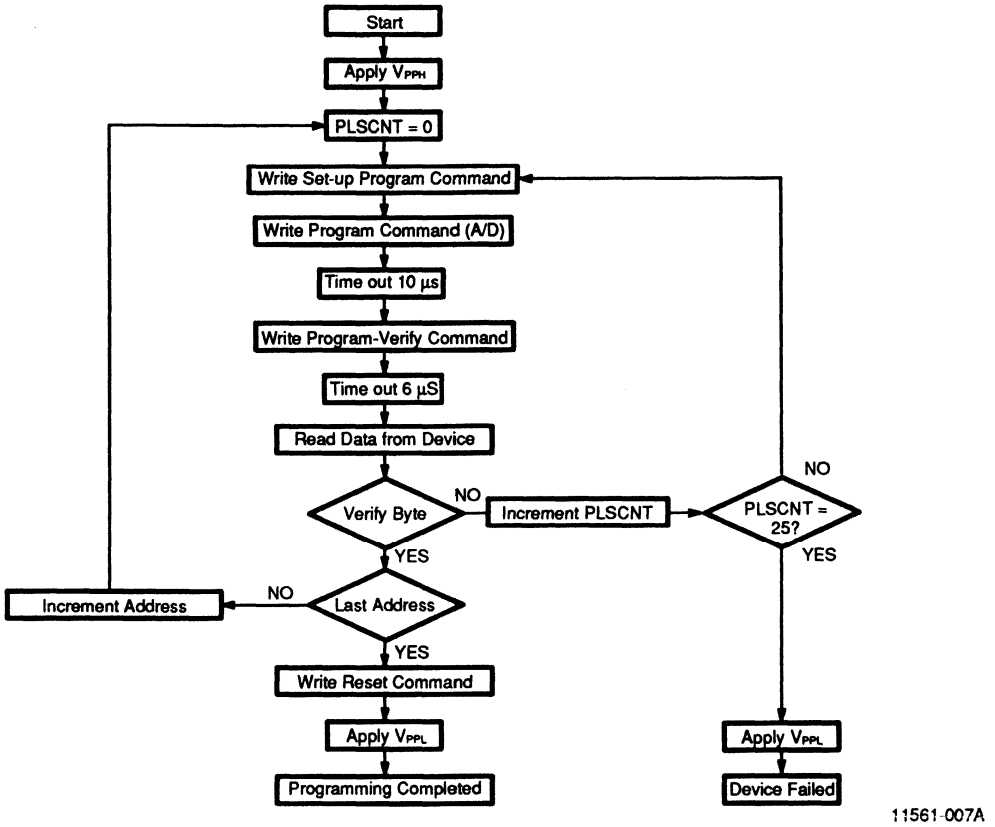


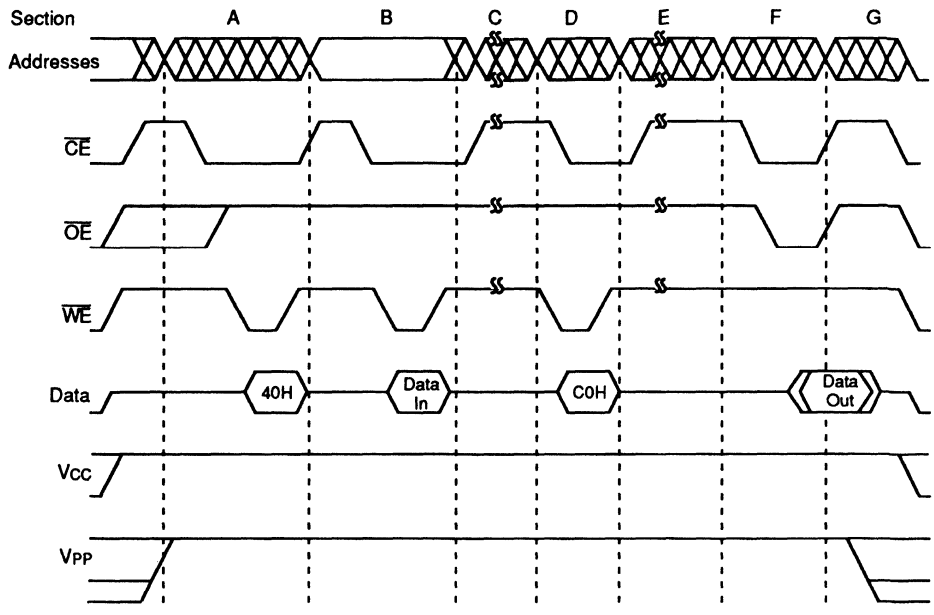
Figure 3. Flashrite Programming Algorithm

Table 6. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



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	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Set-up Program	Program Command Latch Address & Data	Program (10 µs)	Program verify	Transition (6 µs)	Program verification	Stand by & Vcc Power down

Figure 4. A.C. Waveforms for Programming Operations

Analysis Of Program Timing Waveforms

Set-up Program/Program

Two-cycle write commands are required for program operations (section A & B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-out

A software timing routine (10 µs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Note:

An integrated stop timer prevents any possibility of over-programming.

Program-verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Section II: Details AMD's Embedded Program and Erase Operations

Embedded Erase Algorithm

The automatic chip erase does not require the device to be entirely pre-programmed prior to executing the Embedded set-up erase command and Embedded erase command. Upon executing the Embedded erase command the device automatically will program and verify the entire memory for an all zero data pattern. The system is not required to provide any controls or timing during these operations.

When the device is automatically verified to contain an all zero pattern, a self-timed chip erase and verify begin. The erase and verify operation are complete when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode. The system is not required to provide any control or timing during these operations.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded set-up erase command is a command only operation that stages the device for automatic electrical erasure of all bytes in the array. Embedded set-up erase is performed by writing 30H to the command register.

To commence automatic chip erase, the command 30H must be written again to the command register. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode.

Figure 5 and Table 7 illustrate the Embedded Erase algorithm, a typical command string and bus operations.

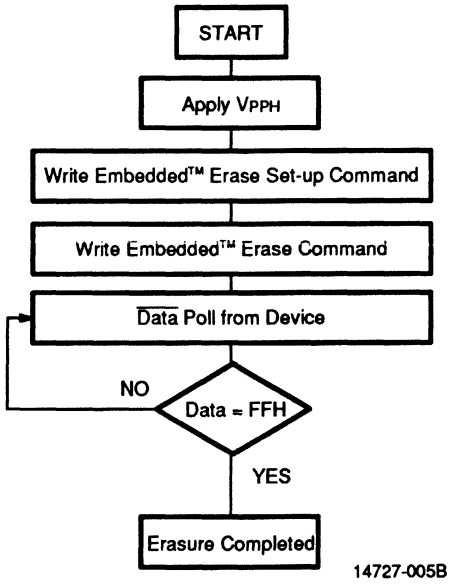


Figure 5. Embedded™ Erase Algorithm

Table 7. Embedded Erase Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Erase Set-up Command	Data = 30H
Write	Embedded Erase Command	Data = 30H
Read		Data Polling to Verify Erasure
Standby		Compare Output to FFH
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation.

Embedded Programming Algorithm

The Embedded Set-up Program is a command only operation that stages the device for automatic programming. Embedded Set-up Program is performed by writing 50H to the command register.

Once the Embedded Set-up Program operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the $\overline{WE}$ pulse. Data is internally latched on the rising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to Read mode (no program verify command is required).

Figure 6 and Table 8 illustrate the Embedded Program algorithm, a typical command string, and bus operation.

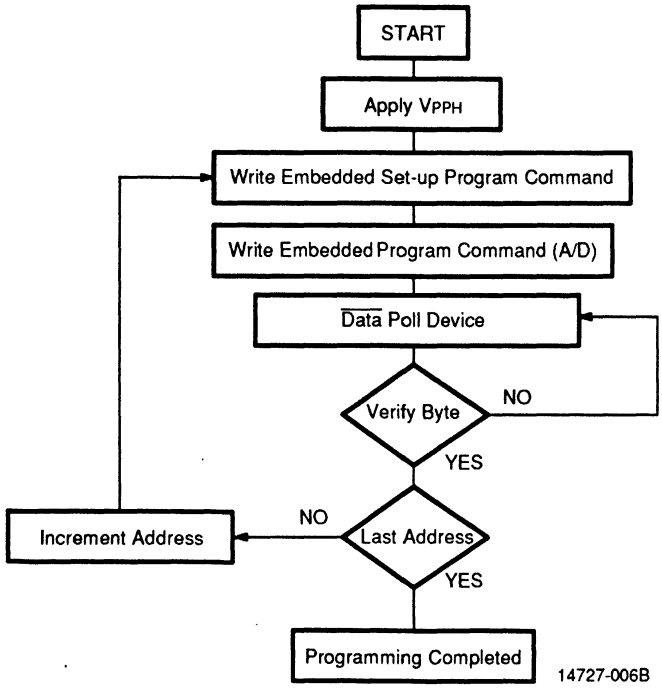


Figure 6. Embedded Programming Algorithm

Table 8. Embedded Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Erase Set-up Program Command	Data = 50H
Write	Embedded Program Command	Valid Address/Data
Read		Data Polling to Verify Erasure
Standby		Compare Output to FFH
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Principles of Operation. Device is either powered-down, erase inhibit or program inhibit.

Write Operation Status

$\overline{\text{Data}}$ Polling—DQ7

The Am28F020 features $\overline{\text{Data}}$ Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device will produce the compliment data of the data last written to DQ7. Upon completion of the Embedded Program algorithm an attempt to read the device will produce the true data last written to DQ7. The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two write pulse sequence.

While the Embedded Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1". The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two Write pulse sequence.

The $\overline{\text{Data}}$ Polling feature is only active during Embedded Programming or erase algorithms.

See Figure 7a and 8 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

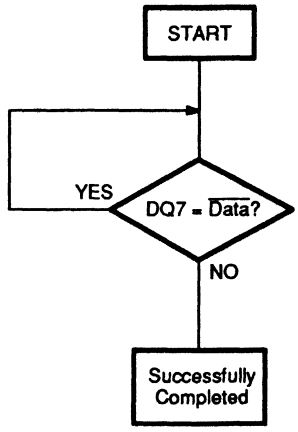


Figure 7a. $\overline{\text{Data}}$ Polling Algorithm

Toggle Bit—DQ6

The Am28F020 also features a "Toggle Bit" as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Program or Erase algorithm is in progress, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, DQ6 will stop toggling and valid data will be read. The toggle bit is valid after the rising edge of the first $\overline{WE}$ pulse of the two write pulse sequence, unlike $\overline{Data}$ Polling which is valid after the rising edge of the second $\overline{WE}$ pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

See 7b and 8 for the $\overline{Data}$ Polling timing specifications and diagrams.

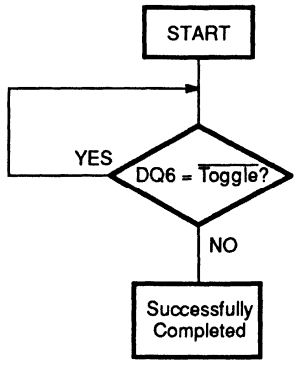


Figure 7b. Toggle Bit Algorithm

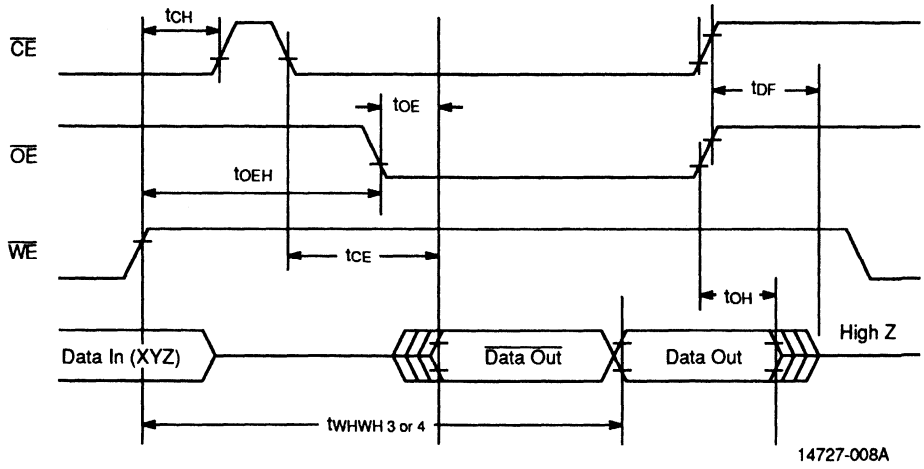


Figure 8. AC Waveforms for $\overline{Data}$ Polling and Toggle Bit during Embedded Algorithm Operations

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1µF/device. V_{PP} must reach its final value 100ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse, or the device may continue to erase until the memory cells are driven into depletion (over-erasure). Should this happen the internal circuitry will no longer select unique addresses. A symptom of over-erasure is an error attempting to program the next time. Occasionally it is possible to recover over-erased devices by programming all of the locations with 00H data.
3. A third delay time is required for each programming pulse width (10 µs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 µs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:
Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified separately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-up Sequence

V_{CC} Prior to V_{PP}

The Am28F020 powers-up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two step command sequence.

V_{PP} Prior to V_{CC}

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. With V_{PP} = 12 V, the Flash device resets to the Read mode when V_{CC} rises above 2 V.

Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the set-up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The set-up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the set-up Program state or not.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-system

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F020 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code 2AH (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
Ceramic Packages	– 65°C to +150°C
Plastic Packages	– 65°C to +125°C
Ambient Temperature with Power Applied	– 55°C to + 125°C
Voltage with Respect To Ground	
All pins except A_9 and V_{PP} (Note 1)	– 2.0 V to +7.0 V
V_{CC} (Note 1)	– 2.0 V to +7.0 V
A_9 (Note 2)	– 2.0 V to +14.0 V
V_{PP} (Note 2)	– 2.0 V to +14.0 V
Output Short Circuit Current (Note 3)	200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

2. *Minimum DC input voltage on A_9 and V_{PP} pins is –0.5V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*

3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second. Conditions equal V_{OUT} = 0.5 V or 5.0 V, V_{CC} = V_{CC} max. These values are chosen to avoid test problems caused by tester ground degradation. This parameter is sampled and not 100% tested, but guaranteed by characterization.*

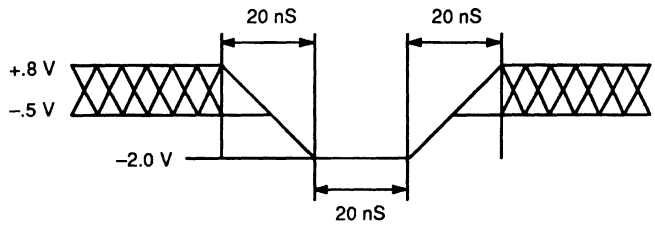
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (Tc)	0°C to +70°C
Industrial (I) Devices	
Case Temperature (Tc)	– 40°C to +85°C
Extended (E) Devices	
Case Temperature (Tc)	– 55°C to +125°C
Military (M) Devices	
Case Temperature (Tc)	– 55°C to +125°C
V_{CC} Supply Voltages	
V_{CC} for Am28F020–X5	+ 4.75 V to +5.25 V
V_{CC} for Am28F020–XX0	+ 4.50 V to +5.50 V
V_{PP} Supply Voltages	
Read	– 0.5 V to +12.6 V
Program, Erase, and Verify	+ 11.4 V to +12.6 V

MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



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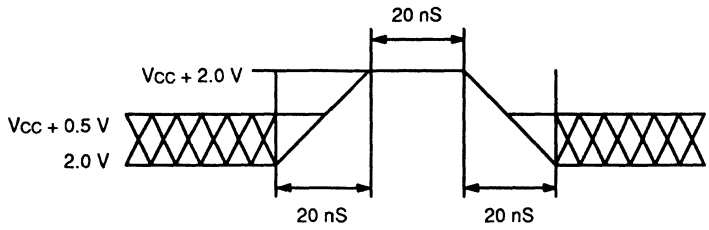
Maximum Positive Input Overshoot



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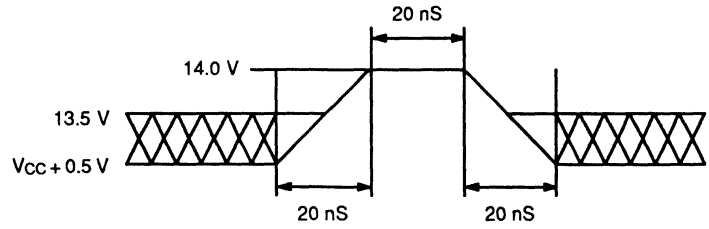
Maximum V_{PP} Overshoot



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DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted) (Notes 1–3)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		+1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		+1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{IH}		1.0	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}		+1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		200	µA
		V_{PP} = V_{PPL}		+1.0	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA V_{CC} = V_{CC} Min.	2.4		V
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		35	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0	V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2		V

DC CHARACTERISTICS-CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		+1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		+1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{CC} ± 0.5 V		100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}		+1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85 V_{CC}		V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC} –0.4		
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		35	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/ Program are inhibited when V_{PP} = V_{PPL}	0.0	V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2		V

Notes:

1. **Caution:** the Am28F020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions $T_A = 25°C$, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Notes 1– 2)

Parameter Symbols				Am28F020				
JEDEC	Standard	Parameter Description		-90 -95	-120	-150	-200	Unit
t_{AVAV}	t_{RC}	Read Cycle Time	Min. Max.	90	120	150	200	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	90	120	150	200	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	90	120	150	200	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min. Max.	35	50	75	75	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	Min. Max.	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z	Min. Max.	20	30	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	Min. Max.	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z	Min. Max.	20	30	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	Min. Max.	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min. Max.	6	6	6	6	µs
t_{VCS}		V_{CC} Set-up Time to Valid Read	Min. Max.	50	50	50	50	µs

Notes:

1. Output Load (except Am28F020-95): 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: ≤ 10 ns, Input Pulse levels: 0.45 to 2.4 V, Timing Measurement Reference Level - Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F020-95 Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. t_{VCS} is guaranteed by design not tested.

AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1–4)

Parameter Symbols				Am28F020				
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	Min. Max.	90	120	150	200	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	60	60	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded™ Algorithm only	Min. Max.	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min. Max.	45	50	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation	Min. Max.	10 25	10 25	10 25	10 25	µs
t_{WHWH2}		Duration of Erase Operation	Min. Max.	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	ms
t_{WHWH3}		Embedded™ Programming Operation (Note 5)	Min. Max.	16	16	16	16	µs
t_{WHWH4}		Embedded™ Erase Operation	Min. Max.	9.5	9.5	9.5	9.5	ms
t_{EHVP}		Chip Enable Set-Up Time to V_{PP} Ramp	Min. Max.	100	100	100	100	ns
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	Min. Max.	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable Low	Min. Max.	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH}	Min. Max.	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 10% V_{PPL}	Min. Max.	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset	Min. Max.	100	100	100	100	ns

*See notes on following page.

Notes:

1. Read timing characteristics during read/write operations are the same as durng read-only operations. Refer to AC Characteristics for Read Only operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
3. All devices except Am28F020-95. Input Rise and Fall times: $\leq$ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
4. Am28F020-95. Input Rise and Fall times: $\leq$ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V
   Timing Measurement Reference Level: Inputs and Outputs: 1.5 V
5. Embedded Program Operation of 16 µs consists of 10 µs program pulse and 6 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.

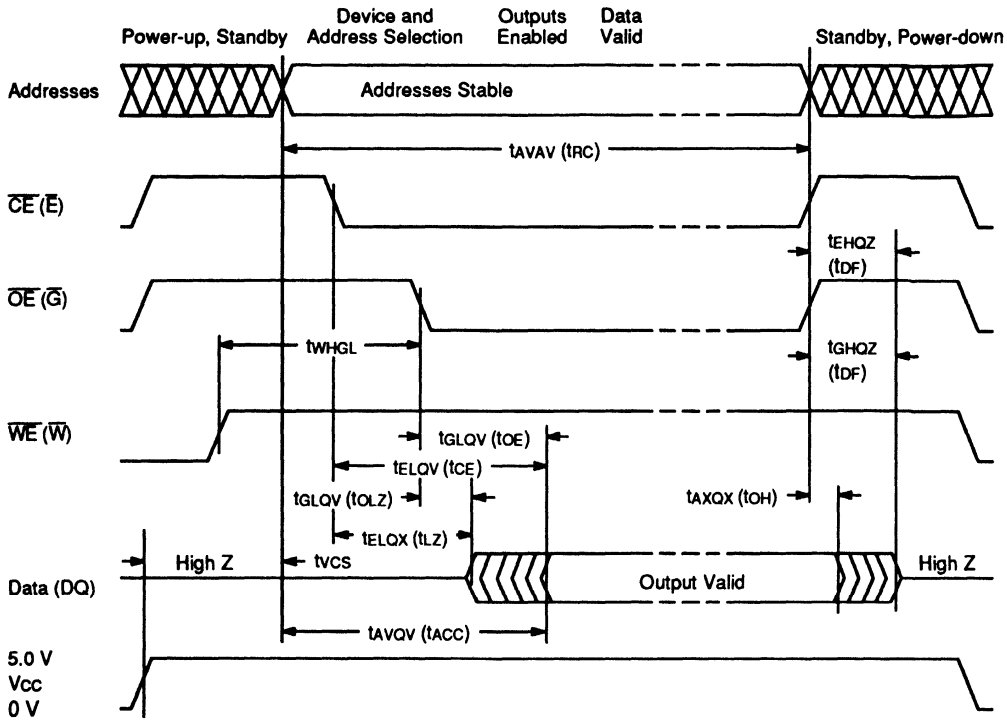

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Figure 9. AC Waveforms for Read Operations

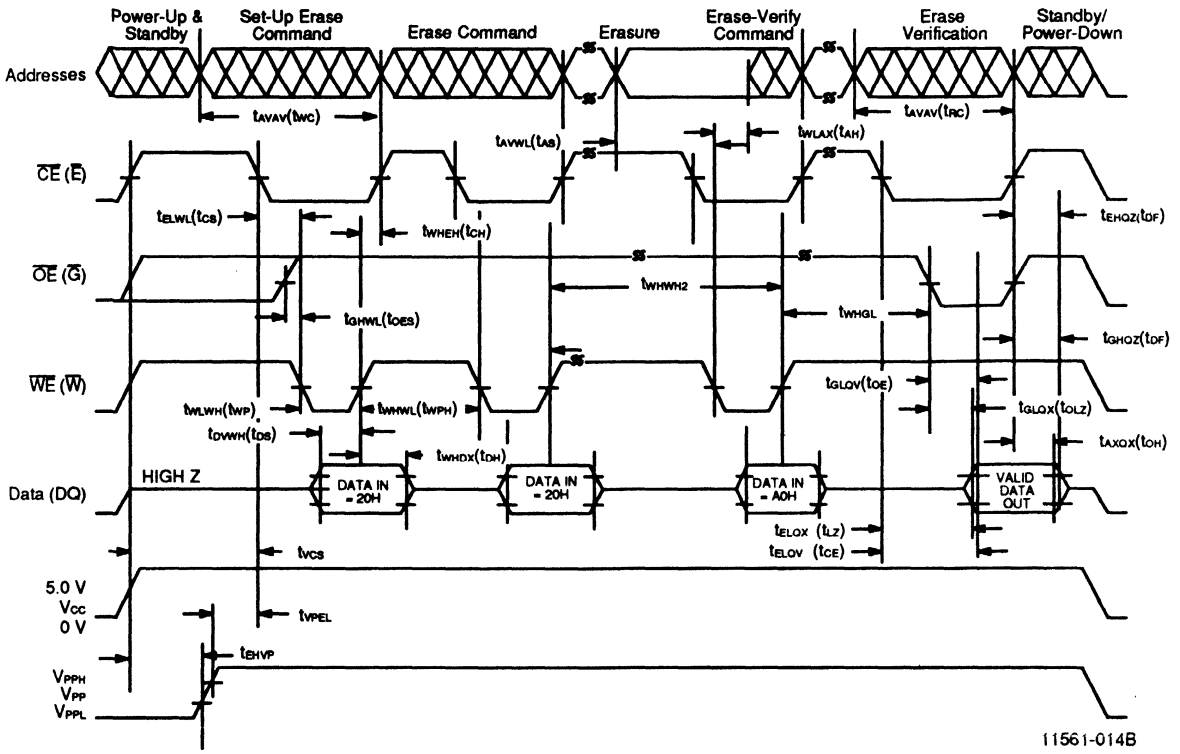


Figure 10. AC Waveforms for Erase Operations

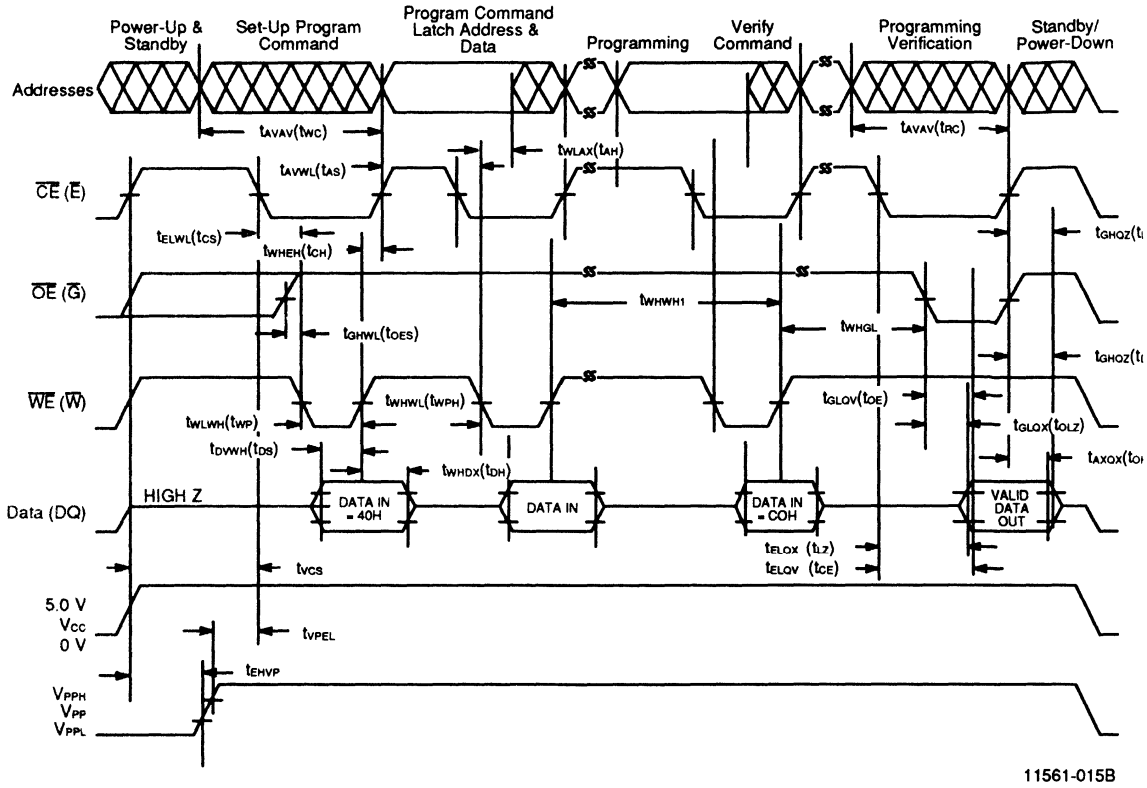
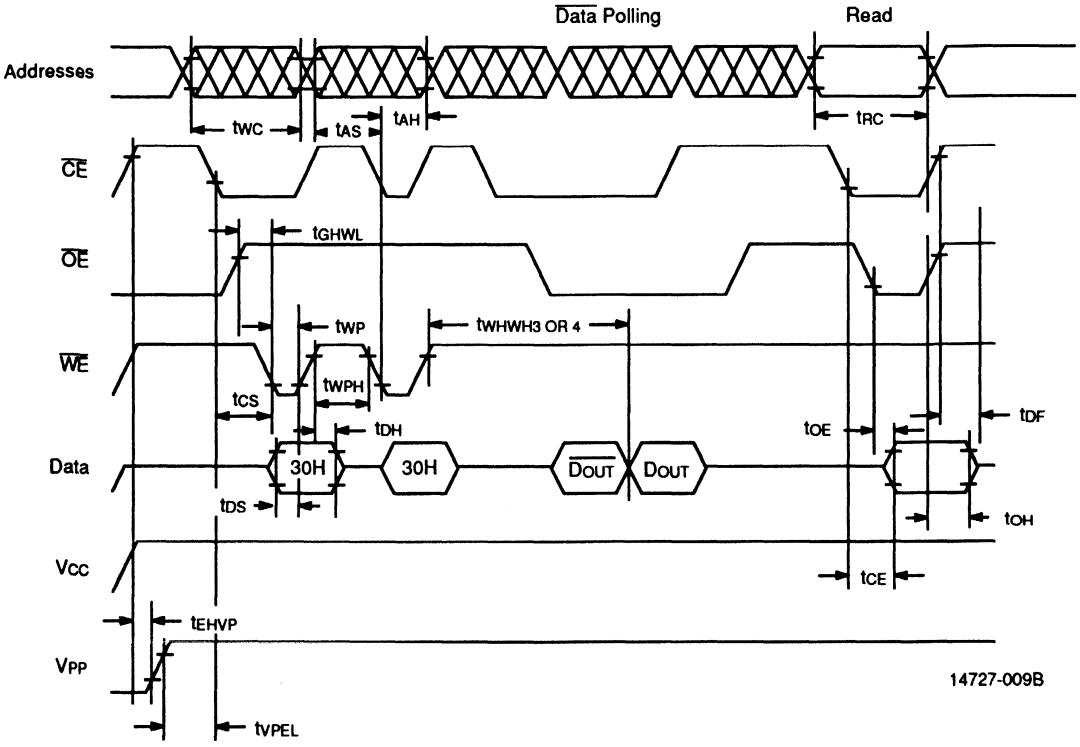


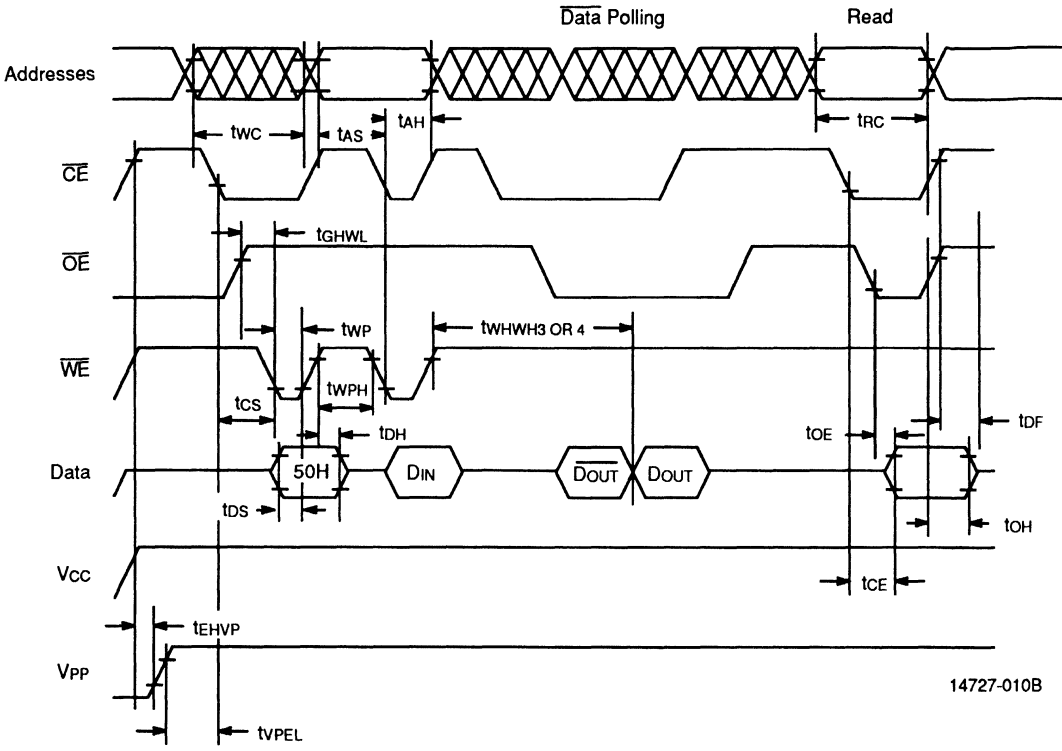
Figure 11. AC Waveforms for Programming Operations



Notes:

1. D_{IN} is data input to the device.
2. $\overline{D_{OUT}}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 12. AC Waveforms for Embedded Erase Operation

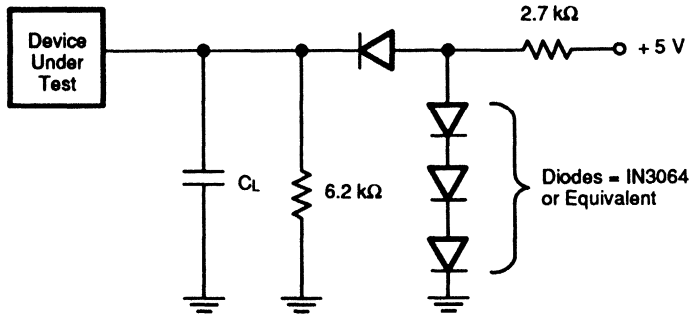


Notes:

1. D_{IN} is data input to the device.
2. $\overline{D_{OUT}}$ is the output of the complement of the data written to the device.
3. D_{OUT} is the output of the data written to the device.

Figure 13. AC Waveforms for Embedded Programming Operation

SWITCHING TEST CIRCUIT



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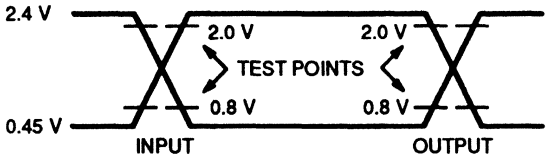
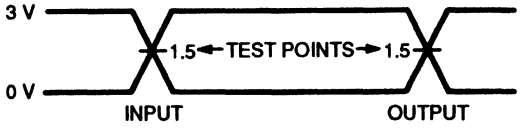
C_L = 100 pF including jig capacitance (30 pF for Am28F020-95)

SWITCHING TEST WAVEFORMS



All Devices Except Am28F020-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.



For Am28F020-95

AC Testing. Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

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ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Chip Erase Time		2 (Note 1)	30 (Note 2)	S	Excludes 00H programming prior to erasure
Chip Programming Time		4 (Note 1)	48	S	Excludes system-level overhead
Erase/Program Cycles					
Am28F020-95C4JC	10,000			Cycles	
Am28F020-95C3JC	1,000			Cycles	

Notes:

1. 25°C, 12V V_{PP}
2. The Embedded algorithm allows for 60 second erase time for military temperature range operations.

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	−1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	−1.0 V	V_{CC} + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

Considerations for In-System Programming

BASIC PRINCIPLES

AMD Flash memories use 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ±0.6 V power supply.

Read Only Memory

Without high V_{PP} voltage, the Flash memory functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. Two-cycle commands are required for erase and reprogramming operations. In addition, the traditional read, standby, output disable, and Auto select modes are available via the register.

The AMD Flash memory command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations.

For system design simplification, the AMD's Flash memory is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. All setup and hold times are with respect to the $\overline{WE}$ signal. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text.

Overview of Erase/Program Operations

Erase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase™ Algorithm.

1. **Erase Set-up:** Write the Erase/Erase Set-up command to the command register.
2. **Erase:** Write the Erase/Erase Set-up command to the command register again. The second command initiates the erase operation. Time-out the erase pulse width.
3. **Erase-verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Programming Sequence

A three-step command sequence (a two-cycle Program command and one-cycle verify command) is required to program a byte of the Flash array. Refer to the Flashrite™ Algorithm.

1. **Program Set-up:** Write the Program/Program Set-up command to the command register.
2. **Program:** Write the Program/Program Set-up command to the command register with the appropriate Address and Data. Time-out the program pulse width.
3. **Program-verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times per byte.

CONSIDERATIONS FOR IN-SYSTEM PROGRAMMING APPLICATIONS

V_{PP} Generation and Control

Constant V_{PP} voltage of 12.0 V ±0.6 V is required for erase and programming operations. Parallel device reprogramming (either 16-bit or 32-bit data words) requires 30 mA of current for each device in the Flash memory array.

V_{PP} voltage can be generated in a number of ways:

1. Use analog circuitry to pump 5 V to V_{PP} Voltage
2. Use DC/DC, monolithic convertor to pump 5 V to V_{PP} Voltage.
3. Hardwire V_{PP} Voltage to the Flash Device
4. Umbilical Cord Programming

It is important to maintain the specified V_{PP} voltages when reprogramming the Flash memory device. All internal device voltages are generated from the V_{PP} reference. Inappropriate V_{PP} voltage may impair device performance. Internal voltages do not exceed that of external V_{PP}.

Unlike other approaches to Flash memories, AMD's devices actually verify margin for each byte during erase and programming operations. This is accomplished during the Erase-verify and Program-verify operations respectively. During these operations, the appropriate margin-verify voltages are internally tapped off of the V_{PP} voltage via the command register and internal V_{PP} circuitry. This allows for Erase/Erase-verify and Program/Program-verify operations to be performed with static V_{CC} (5 V) and V_{PP} (12 V) voltages.

V_{PP} Supply

1. Use analog circuitry to Pump 5 V to V_{PP} Voltage.

See Application Note AN-102 on V_{PP} Generation and Control for circuit schematics and more detailed discussions.

2. Use DC/DC Monolithic Convertor to Pump 5.0 V to V_{PP}.

A monolithic DC/DC convertor from Valor Electronics, the PM9006, is appropriate for the digital world to supply the 12.0 V ±0.6 V V_{PP} voltage. The V_{PP} voltage is generated on a chip using the standard system V_{CC} (5.0 V) voltage. Standard TTL commands are used to disable the 12.0 V output supply when programming or erasing operations are not intended. The enable ($\overline{E}$) function provides absolute write protection to guarantee against inadvertent program or erasure. Flash memory contents cannot be altered without the active 12.0 V V_{PP} supply. The enable pin also saves system power when the DC/DC convertor is not required. The PM9006 has a minimum efficiency of 50% at full load. The PM9006 comes in a 24-pin package.

The Valor PM9006 provides a controlled 12.0 V output that is regulated within the ±5% (±0.6 V) V_{PP} specification. The standard system V_{CC} (5.0 V) supply is converted to the V_{PP} (12.0 V) supply by the DC/DC convertor. The voltage transitions are smooth and protect against destructive positive or negative overshoot.

The PM9006 can supply 165 mA of current at the regulated 12.0 V ±0.6 V output. The 5.0 V ±0.5 V DC input supply of the DC/DC convertor uses a maximum of 840 mA of input current. The Am28F010 specifies a maximum V_{PP} current of 30 mA for either the erase or program operations. Actual current required for these operations is substantially lower than this. Given the maximum V_{PP} current of 30 mA for each device, four (4) Am28F010 may be programmed and erased in parallel (120 mA) with one PM9006 device. The PM9006 V_{PP} supply current = 165 mA.

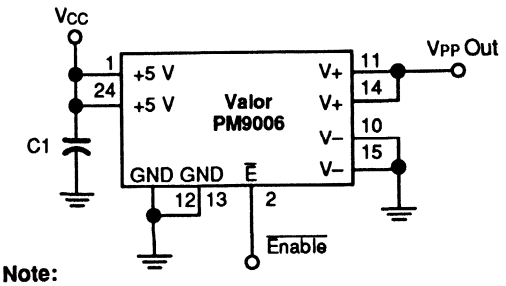
Parallel programming and erasure allows for the most efficient method to reprogram x16 or x32 bit data words. Refer to the following application note for parallel program and erase flow charts.

Board Level Resets

System designs should not allow the Flash device to perform any programming or erase operations when the CPU does not have control of the Flash device. Some designs incorporate board level reset circuitry that suspends operation of the local CPU if the V_{CC} level falls below a predetermined value (such as 4.6 V). If this is the case, the reset circuitry should also disable the V_{PP} power supply whenever the CPU is held in reset.

If the local CPU is forced into reset mode while it is programming or erasing the Flash device, the system reset circuit should also terminate that operation. To accomplish this, the PM9006's enable pin should be driven high whenever the reset circuitry is active. Drive the chip enable pin of the PM9006 with the logical OR of the reset circuitry's output signal and the chip enable control line to the PM9006. This will disable the V_{PP} supply and hence termiante any programming or erase operation. The Flash device automatically resets to the read mode when V_{PP} is disabled.

Please reference the PM9006 data sheet for complete details of device operation. One method of implementing the PM9006 DC/DC convertor is illustrated on page four.



Note:

Pins 3 through 9 and 16 through 23 are not internally connected to the device and do not need to be driven.

Generate and Control 12.0 V

3. Hardwire V_{PP} Voltage to the Flash Device.

Typically this approach is used in the most cost sensitive applications. Regulated 12.0 V supplies are commonly available in many systems.

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. The Flash device automatically resets to the read mode when V_{CC} rises above 2 V. This occurs even when V_{PP} = 12 V.

Power Supply sequencing is not required.

The device will only respond to the correct sequence of commands in order to change the state of the Flash memory from Read mode to any other mode. In addition, the three control pins must be in their correct state ($\overline{CE}$ = Low, $\overline{OE}$ = High, and $\overline{WE}$ = Low) in order to accept a command from the data bus.

A number of additional procedures are available to further prevent inadvertent writes should system glitches occur during system/device power transitions:

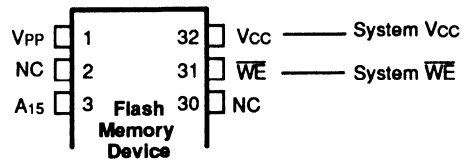
- Hold any control pin ($\overline{CE}$, $\overline{OE}$, or $\overline{WE}$) in a non-write condition. This disables the device from executing a write operation. Please refer to following example.
- Any "illegal" command (an illegal command is one that is not defined in the AMD Flash Memory data sheet under the section – Command Definitions) written to the Flash device will automatically terminate any operation and reset the device to the Read Mode.

4. Umbilical Cord Programming

Many applications perform system updates using the umbilical cord or edge connector programming method. The external programming equipment supplies the 12.0 V ±0.6 V V_{PP} voltage. When the umbilical cord is disconnected, be aware that electrostatic discharge may build up on the floating V_{PP} pin. To prevent this problem, tie the V_{PP} pin to ground via a large (10K Ω) pull-up resistor and a capacitor.

Example:

Holding $\overline{WE}$ in a non-write condition during power transitions.



In systems where the V_{PP} pin is to be connected directly to the +12 V supply, $\overline{WE}$ should be held in a non-write state during power supply transitions. This will prevent against inadvertent write conditions.

During power supply transitions, V_{PP} voltage is internally disabled from the Flash device until V_{CC} rises above 2 V. In addition, the Flash device automatically resets to the read mode as V_{CC} rises above 2 V. When write enable is at V_{IH} the command register is internally disabled from the internal state machine of the Flash device. When the command register is disabled, data commands can not be transferred to the state machine. Therefore the state of the Flash device will not be altered from the read mode. Access to the command register will be prevented until the $\overline{WE}$ line is driven to a logic level low by the system write control.

Note: V_{IH} Min. = 2.0 V

V_{PP} Layout and Circuitry

Be aware that AC current is a component of DC power switching characteristics. Design the printed circuit board traces handling this current to accommodate high frequency.

Printed Circuit Board Trace Layout: Use a single ground plane to eliminate potential loops. Keep all inductive impedances at a minimum on all high current traces.

V_{PP} Regulator Circuitry Layout: Locate the V_{PP} generation circuitry as close to the Flash memory array as possible. In addition, minimize lead lengths of the network. To help prevent noise from being picked up in feedback loops, locate all resistors and capacitors as close to the V_{PP} network as possible. In order to prevent input ground loops, use separate returns for input and output capacitors.

Device Decoupling

Switching $\overline{CE}$ inputs for memory selection causes transient current peaks at the Flash device. The Flash memory devices should be decoupled with the appropriate capacitance.

- Connect a 0.1 µF ceramic capacitor between V_{CC} and V_{SS} and one between V_{PP} and V_{SS}. The capacitors should be placed as close to each device as possible.
- In addition, connect a 4.7 µF electrolytic capacitor between V_{CC} and V_{SS} on the memory arrays' power supply. Do this for each set of eight memory devices. This bulk capacitor will maintain even voltage to the memory array.

System Initialization

During remote code updates the possibility that the communication link could be disrupted during a reprogramming sequence exists. Should this occur, the state of the Flash device (Erased, Partially Programmed, etc.) may not be known. Bootcode should always reset the Flash memory as part of the initialization sequence. Also, status flags should be read to determine the state of the Flash device upon reset.

Systems that are designed for remote updates should contain the following as at least a subset of the bootcode program:

- In-system reprogramming routines for Flash,
- Standard initialization and diagnostic routines,
- A set of communication routines,

as part of the boot code. The boot code can be cost effectively stored in an AMD ExpressROM™ as a separate memory device.

As with any logic device, the Reset command initializes the Flash memory to a known state: the Read mode. This is accomplished by writing the Reset command twice in succession to the Flash device. This should occur in the first part of the system initialization routine.

First we will discuss resetting the Flash device as part of the initialization sequence. Then we will discuss the use of reprogramming flags to keep track of the state of the Flash device after remote updates (i.e., does the memory content contain valid data).

Interrupt Sequences

Interrupt sequences should always reset the Flash device as the first part of any routine. In addition, it is advisable to disable the V_{PP} voltage during interrupts. The Reset command should be written twice in a row to all Flash devices as part of the interrupt sequence. This resets the Flash device to the Read mode. Reset the Flash device as the initial commands of any routine. This procedure is also relevant should a software or hardware reset occur while the system is in the process of reprogramming the Flash memory. By including the consecutive reset command sequence in the bootcode the erase or program operations will be terminated when the system reboots.

Hardware resets may be implemented by connecting the reset signal directly to an interrupt controller. The software interrupt sequence to reset the Flash memory is then executed by the corttroller.

Data Transmission

In order to guarantee accurate data updates, reprogramming protocols may include echo techniques or error-free transmission algorithms.

The echo technique is a straight forward approach to verify transmission of accurate data. The remote system sends back the Flash memory instructions (i.e. Set-up Erase/Erase) to the host system. The remote system waits for a confirmation of the instruction prior to execution. Once the memory array is reprogrammed, the remote system transmits the data to the host for verification. Upon confirmation the remote system programs the Data Valid word. This concept is explained in the Data Valid section.

Handshaking

Communication protocols for the host system in charge of remote updates should require a status check from the target system prior to sending reprogramming commands. If the system indicates it is available, the appropriate command is issued by the host system. Should the remote system indicate it is not available the host may break the communication link and wait for a request to reconnect later. Handshaking protocols are recommended in applications where system downtime is not acceptable to accommodate reprogramming routines.

Data Valid Flags

Once the Flash memory and other system components have been reset the system should check for the validity of data contained in the Flash memory devices. This is an issue when the system resets or the communication link is disrupted during remote reprogramming routines.

The system should check the Flash device for valid data upon initialization.

The Data Valid flag is a data word that is the final word programmed into the Flash array. This word is programmed after verification that valid data has been successfully reprogrammed into the Flash memory array. The Data Valid word will not be programmed if the memory array data is invalid or the communication link was disrupted during a reprogramming sequence. During system initialization the CPU will look for the Data Valid word. If it is not programmed, the system will recognize that the Flash memory is not programmed with accurate data. The Flash memory must be accurately programmed before the system initialization routine can be completed.

Data Protection

Because AMD's Flash memories are designed to be reprogrammed in-system AMD has incorporated a number of data protection methods against inadvertent erase or program.

Software

AMD's Flash Memories require a two-cycle Write command to initiate either the erase or program operations. Refer to the Set-up Erase/Erase or Set-up Program/Program commands. These commands drive an internal state machine that controls the device operation. The state machine is designed to expect the first Write cycle command to be a set-up command. Set-up commands will not alter the memory data. Successful execution of the appropriate second Write cycle command will initiate the erase or program operations.

Control Inputs

AMD's Flash memory devices require that $\overline{OE} = V_{IH}$ and $\overline{CE} = \overline{WE} = V_{IL}$ in order to load the register with a command. If any pin is not in the correct state a write cycle cannot be initiated.

POWER-UP SEQUENCE

V_{CC} Prior to V_{PP}

AMD's Flash devices always power-up in the Read only mode. In addition, memory contents may only be altered after successful completion of a two step command sequence.

V_{PP} Prior to V_{PP}

When $V_{CC} = 0$ V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. When $V_{PP} = 12.0$ V, the Flash device will reset to the Read mode when V_{CC} rises avove 2.0 V.

Power supply sequencing is not required.

AUTO SELECT COMMAND

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-System

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not a generally desired system design practice.

AMD's Flash memories contain an Auto select operation to supplement traditional PROM programming methodology. The operation is initiated by writing either 80H or 90H into the command register. Following this command, a Read cycle from address 0000H retrieves the manufacturer code of 01H. A Read cycle from address 0001H returns the appropriate device code. To terminate the operation, it is necessary to write another valid command into the register.

Data Change Sequence

Flash memories perform data change cycles differently than full-featured E²PROMs. Flash memories must always be completely programmed prior to erasure. This ensures against over-erasure, because all bytes are erased from the fully programmed state.

A data change sequence will include the following:

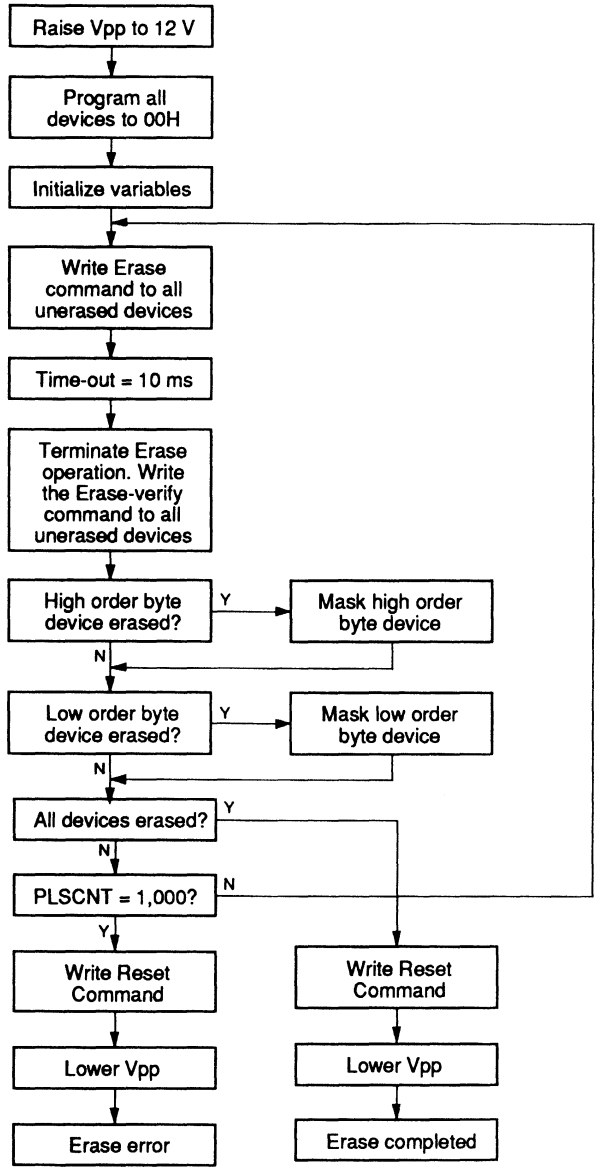
- Program the entire array to 00H data using the Flashrite™ Algorithm.
- Bulk-Erase the entire device using AMD's Flashrite™ Algorithm.
- Program the array with the appropriate data pattern using AMD's Flashrite™ Algorithm.

As long as the user follows AMD's Flasherase™ and Flashrite™ Algorithms, the device will not over-erase.

PROGRAMMING MULTIPLE MEMORY ARRAYS

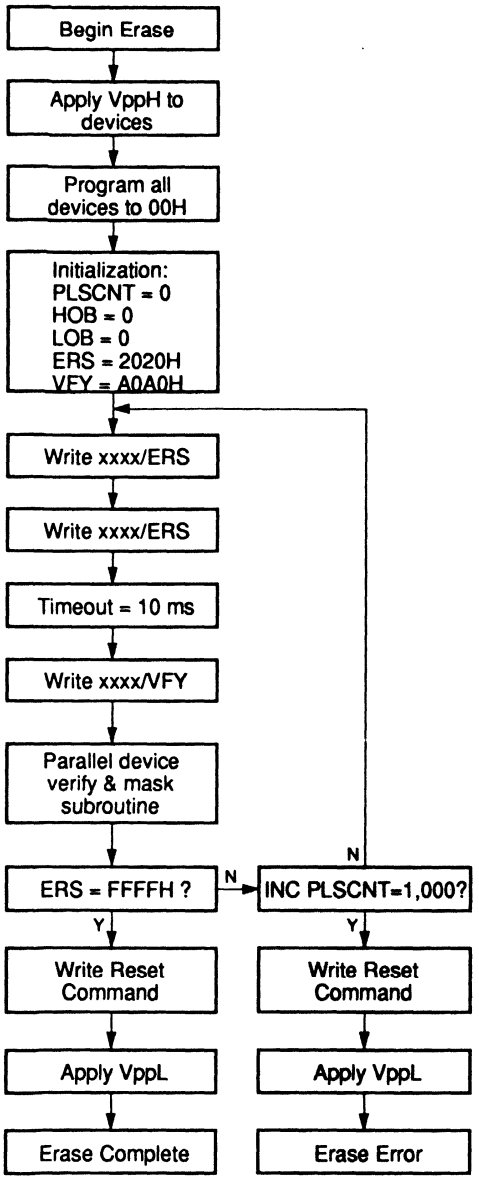
Many applications require multi-memory device arrays. AMD's Flash memories provide the standard $\overline{OE}$ and $\overline{CE}$ device control inputs. These two controls allow for specific selection of one memory device in an array and help prevent the potential for bus contention. Because all non-selected memories may be left in standby mode, the memory arrays' power dissipation is maintained at its lowest level.

PARALLEL DEVICE ERASURE—OVERVIEW



13008-001A

PARALLEL DEVICE ERASURE FLOW CHART



13008-002B

Activity

Allow V_{PP} to stabilize.

Follow Flashrite programming algorithm.

Initialize Erase Variables:
PLSCNT = Pulse Counter
HOB = High Order Address Byte
LOB = Low Order Address Byte
ERS = Erase Command
VFY = Erase-verify Command

xxxx = Address do not care.
Write Erase Set-up command.

Initiate erase pulse.

Duration of erase pulse.

Erase-verify command terminates the erase pulse.

See Parallel Device Erasure subroutine. Each device is independently verified. The command is masked by the Reset command (FFH) for all devices that are completely erased. Please see note below.

ERS = FFFFH when all devices are erased. Please see note below.

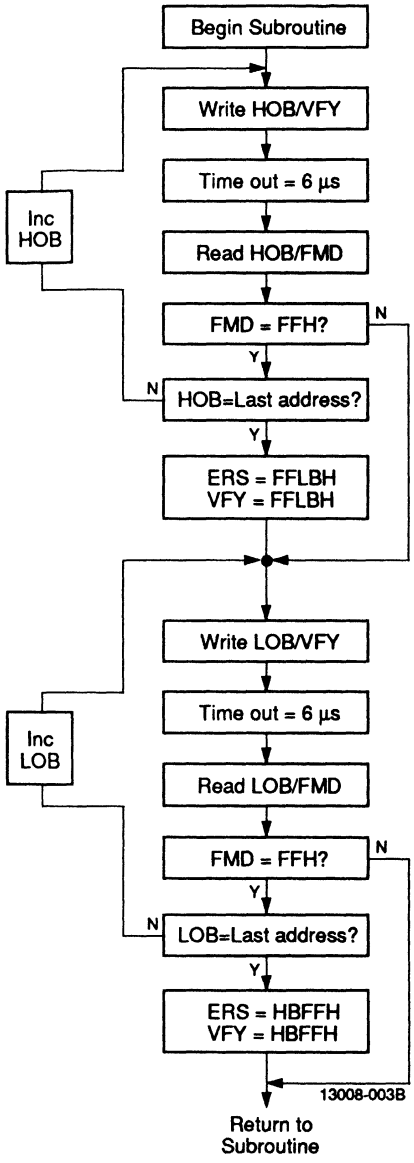
Reset devices for read operation.

V_{PP}L deactivates the command register. Device is in the Read Only Mode.

Note:
Although the Reset command (FFH) is recommended, the Read command (00H) will also mask any completely erased devices from further erase operations.

PARALLEL DEVICE ERASURE—SUBROUTINE

High Order Byte and Low Order Byte Device Program Verify and Mask Subroutine.



Activity

The Subroutine verifies each device independently and masks the completely erased device from further erasure.

Verify High Order Byte Device:
Addresses are latched (HOB) on Erase-verify command.

Internal margin verify voltages are tapped from external 12 V V_{PP} for proper byte verification.

Read HOB from previously latched Address.
FMD = Flash Memory Data.

Compare Flash Memory Data to FFH. If verified, then compare next high order byte address. If invalid, then Jump to low order byte device.

If all addresses of the high order byte device are verified, mask the Erase and Verify commands with the Reset command, (FFH). Low order byte (LB) device commands are not altered. Please see note below.

Verify Low Order Byte:
Addresses are latched (LOB) on verify command.

Internal margin verify voltages are tapped from external 12 V V_{PP} for proper byte verification.

Read LOB from previously latched address. FMD = Flash Memory Data.

Compare Flash Memory Data to FFH. If verified, then compare next low order byte address. If invalid, return to main parallel erase flow for next erase pulse.

If all addresses of the low order byte device are verified, mask the erase and verify command with the Reset command (FFH). High order byte (HB) device commands are not altered. Please see note below.

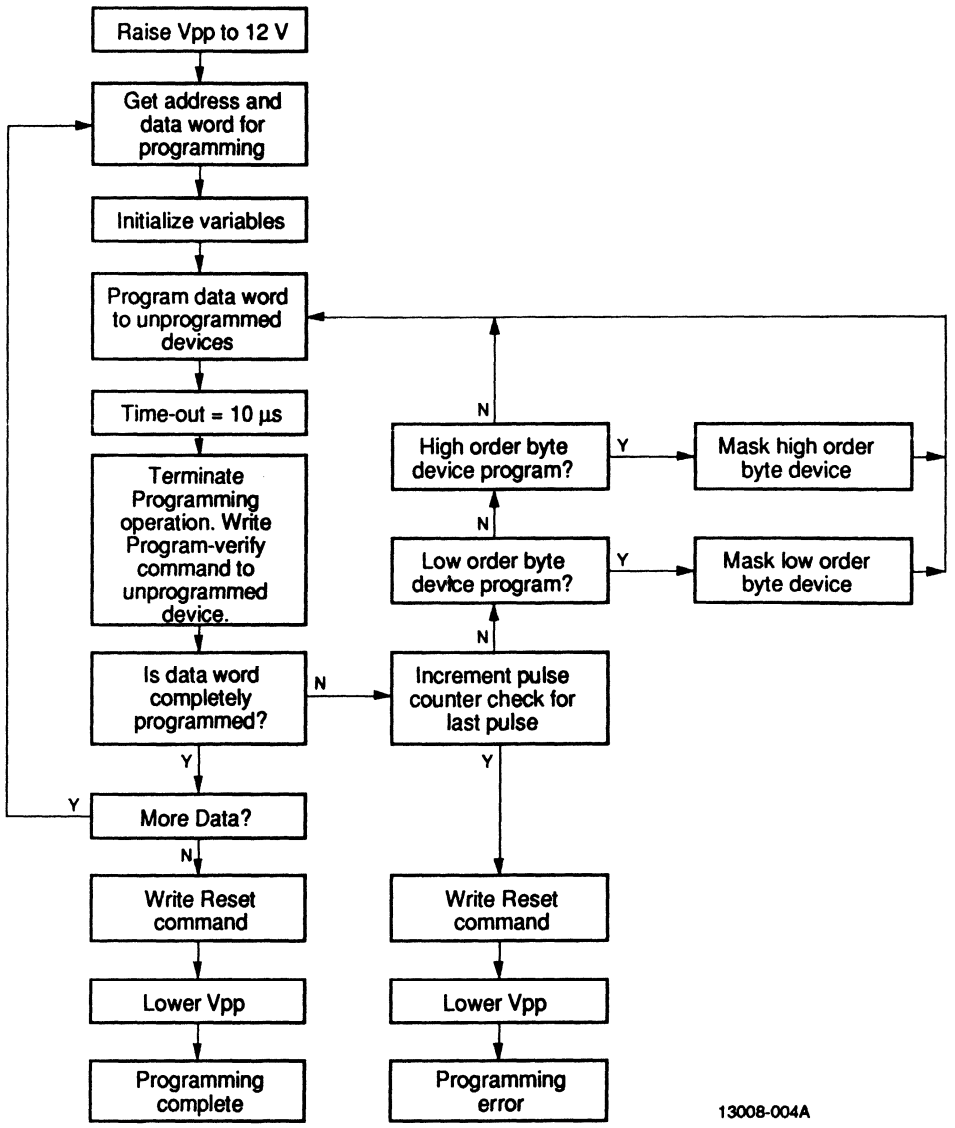
Note:
Although the Reset command (FFH) is recommended, the Read command (00H) will also mask any completely erased devices from further erase operations.

The $\overline{CE}$ control pins should be driven by the outputs of an address decoder. The system's memory Read and Write signal should control the $\overline{OE}$ and $\overline{WE}$ controls of the memory array respectively.

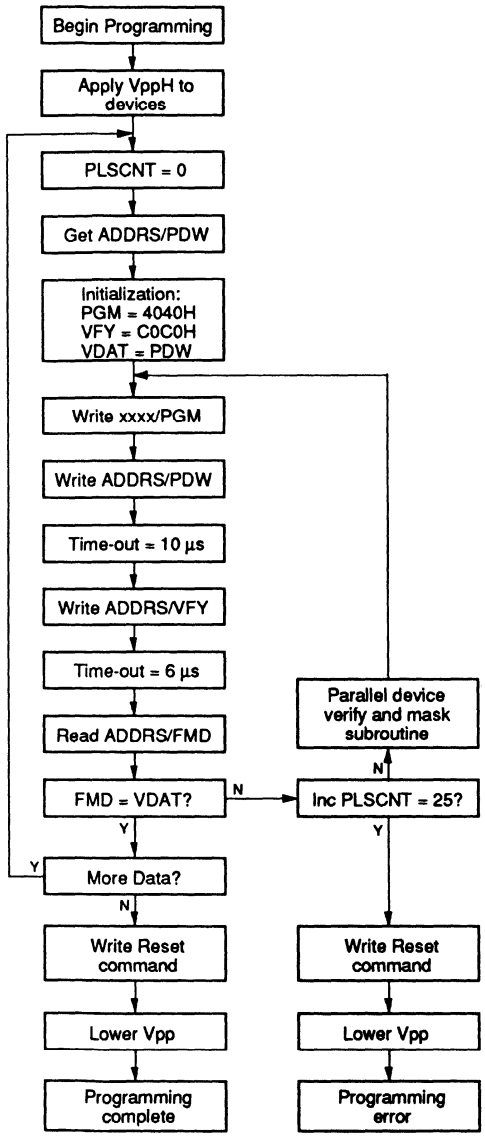
Parallel Device Erasure

A bank of Flash memories may be erased in parallel. This reduces total erase time when compared to erasing each device individually. Each Flash memory may erase at different rates. Therefore each device must be verified separately after every erase pulse. Once a device has successfully completed erasure do not issue the erase command again to that device. Issue the Reset command FFH to the erased device. The Erase command sequence may be issued to each of the remaining devices that have not erased yet. In addition to the address verify register required for each device you will need an erase complete flag for each device.

PARALLEL DEVICE PROGRAMMING – OVERVIEW



PARALLEL DEVICE PROGRAMMING FLOW CHART



Activity

Allow V_{PP} to stabilize.

PLSCNT = Pulse Counter.

ADDRS = Word Address to program.
PDW = Data Word to program.

Initialize Programming Variables:
PGM = Program Command
VFY = Program-verify Command
VDAT = Valid Data

xxxx = Address do not care.
Write Program Set-up command.

Appropriate address and data for programming.

Duration of programming pulse.

Program-verify command terminates the programming pulse.

Internal margin verify voltages are tapped from external 12 V V_{PP} for proper byte verification.

Read from previously latched address. FMD = Flash Memory Data.

See Parallel Device Programming subroutine. Each device is independently verified. The Program command is masked by the Reset command (FFH) for all devices that are completely Programmed. Please see note below.

Compare Flash Memory Data to valid word data. If verified, reset PLSCNT and get next address and data word for programming. If invalid, increment pulse counter. If not last pulse, compare high order byte device and low order byte device for valid byte data.

Reset devices for read operation.

$V_{PP}L$ deactivates command register. Device is in Read Only Mode.

Note:
Although the Reset command (FFH) is recommended, the Read command (00H) will also mask any device from programming operations.

Example: Parallel Erasure and Programming for Two Devices

Parallel Erasure

The erase sequence will be followed as usual. The CPU will issue word commands. The erase word command is 2020H. Each device is independently verified and the address of the last verified byte per device is stored in separate registers. When one of the erase flags is active, indicating that a particular device has successfully completed erasure the CPU will change the command for that device from Erase to Reset. This effectively masks the erased device from further erasure.

Should the high order byte device verify first, the next erase command will be FF20H. The low order byte device erases on each subsequent erase command until verified. The high order byte device remains in Reset/Read mode. During verification, write the erase verify command of FFA0H. This will enable the low order byte device for verify operations and maintains the erased high order byte device in the Reset/Read mode.

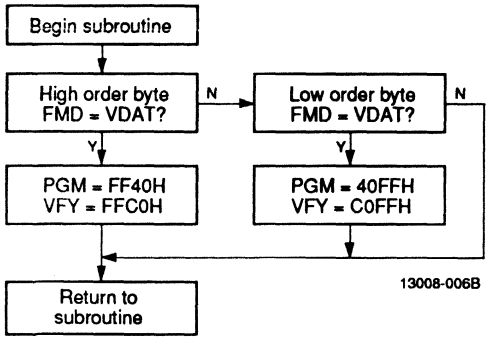
Parallel Programming

The program sequence will be followed as usual. The CPU will issue word commands. The program word command is 4040H. Each device is independently verified. When one of the program flags is active, indicating that a particular device has successfully completed programming, the CPU will change the command for that device from Program to Reset. The CPU will also change the Program Data to the null data set (FFH). This effectively masks the programmed device from further programming.

Should the high order byte device verify first, the next program command will be FF40H. The low order byte device programs on each subsequent program command until verified. The high order byte device remains in Reset/Read mode. During verification, write the program verify command of FFC0H. This will enable the low order byte device for verify operations and maintains the programmed high order byte device in Reset/Read mode.

PARALLEL DEVICE PROGRAMMING – SUBROUTINE

High Order Byte and Low Order Byte Device Erase-verify and Mask Routine



This Subroutine verifies the high order and low order bytes independently. If either byte verifies, all commands are masked from that device.

The program command and program data are changed to a Reset command (FFH) and null data (FFH) respectively. Please see note below.

The Program-verify command is changed to a Read command (00H).

Notes:

- During programming operations, FFH data is a null condition. Only "0"s can be programmed into Flash memory cells.
- If the high order byte verifies, then that byte is masked from further Program/Program-verify operations. The low order byte (LB) commands are not changed.
- If the low order byte verifies, then that byte is masked from further Program/Program-verify operations. The high order byte (HB) commands are not changed.
- Although the Reset command (FFH) is recommended, the Read Command (00H) will also mask any device from program/program-verify operations.

Generation and Control of V_{PP} Programming Voltage for Flash Memories

INTRODUCTION

Constant V_{PP} voltage of 12.0 V ±0.6 V is required for erase and programming operations. Parallel device reprogramming (either 16-bit or 32-bit data words) requires 30 mA of current for each device in the Flash memory array.

V_{PP} voltage may be generated in a number of ways. Each of these options will be discussed during the text.

1. Hardwire V_{PP} Voltage to the Flash Device.
2. Umbilical Cord Type Programming.
3. Use DC/DC Convertor to pump 5 V to V_{PP} Voltage.
4. Pump 5 V to V_{PP} Voltage with Analog Circuitry.

It is important to maintain the specified V_{PP} voltages when programming the Flash memory device. All internal device voltages are generated from the V_{PP} reference. Inappropriate V_{PP} voltage may impair device performance. Internal voltages do not exceed that of external V_{PP}.

Unlike other approaches to Flash memories, AMD's devices actually verify margin for each byte during erase and programming operations. This is accomplished during the Erase-verify and Program-verify operations respectively. During these operations, the appropriate margin-verify voltages are internally tapped off of the V_{PP} voltage via the command register and internal V_{PP} circuitry. This allows for Erase/Erase-verify and Program/Program-verify operations to be performed with static V_{CC} (5 V) and V_{PP} (12 V) voltages.

Before proceeding, a few comments regarding basic design philosophy should be mentioned. Please make note of these comments for any of the V_{PP} generation methods implemented.

V_{PP} Trace and Circuitry

Be aware that AC current is a component of DC power switching characteristics. Design the printed circuit board traces handling this current to accommodate high frequency.

Printed Circuit Board Trace Layout

Use a single ground plane to eliminate potential loops. Keep all inductive impedances at a minimum on all high current traces.

V_{PP} Regulator Circuitry Layout

Locate the V_{PP} generation circuitry as close to the Flash memory array as possible. In addition, minimize lead lengths of the network. To help prevent noise from being picked up in feedback loops, locate all resistors and capacitors as close to the V_{PP} network as possible. In order to prevent input ground loops, use separate returns for input and output capacitors.

Device Decoupling

Switching $\overline{CE}$ inputs for memory selection causes transient current peaks at the Flash device. The Flash memory devices should be decoupled with the appropriate capacitance from these transients.

- Connect 0.1µF ceramic capacitor between V_{CC} and V_{SS} and one between V_{PP} and V_{SS}. The capacitors should be placed as close to each device as possible.
- In addition, connect 4.7µF electrolytic capacitor between V_{CC} and V_{SS} on the memory array's power supply. Do this for each set of eight memory devices. this bulk capacitor will maintain even voltage to the memory array.

1. HARDWIRE V_{PP} VOLTAGE TO THE FLASH DEVICE

Typically this approach is used in the most cost sensitive applications. Regulated 12.0 V supplies are commonly available in many systems.

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. The Flash device automatically resets to the read mode when V_{CC} rises above 2 V. This occurs even when V_{PP} = 12 V.

Power supply sequencing is not required.

The device will only respond to the correct sequence of commands in order to change the state of the Flash memory from Read mode to any other mode. In addition, the three control pins must be in their correct state ($\overline{CE}$ = Low, $\overline{OE}$ = High and $\overline{WE}$ = Low) in order to accept a command from the data bus.

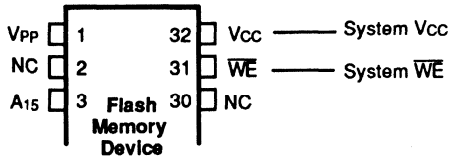
A number of additional procedures are available to further prevent inadvertent writes should system glitches occur during system/device power transitions.

- Hold any control pin ($\overline{CE}$, $\overline{OE}$, or $\overline{WE}$) in a non-write condition. This disables the device from executing any write operation (see example on the next page).
- Any "illegal" command (an illegal command is one that is not defined in the AMD Flash data sheet under the section – Command Definitions) written to the Flash device will automatically terminate any operation and reset the device to the Read Mode.

Publication #	Rev.	Amendment	Issue Date
10934	B	/0	3/91

Example:

Holding $\overline{WE}$ in a non-write condition during power transitions.



In systems where the V_{PP} pin is to be connected directly to the +12 V supply, $\overline{WE}$ should be held in a non-write state during power supply transitions. This will prevent against inadvertent write conditions.

During power supply transitions, V_{PP} voltage is internally disabled from the Flash device until V_{CC} rises above 2 V. In addition, the Flash device automatically resets to the read mode as V_{CC} rises above 2 V. When write enable is at V_{IH} the command register is internally disabled from the internal state machine of the Flash device. When the command register is disabled, data commands can not be transferred to the state machine. Therefore the state of the Flash device will not be altered from the read mode. Access to the command register will be prevented until the $\overline{WE}$ line is driven to a logic level low by the system write control.

Note: V_{IH} Min. = 2.0 V

2. UMBILICAL CORD PROGRAMMING

Many applications perform system updates using the umbilical cord or edge connector programming method. The external programming equipment supplies the 12.0 V ±0.6 V V_{PP} voltage. When the umbilical cord is disconnected, be aware that electrostatic discharge may build up on the floating V_{PP} pin. To prevent against this problem, tie the V_{PP} pin to ground via a large (10KΩ) pull-up resistor and a capacitor (see Figure 1).

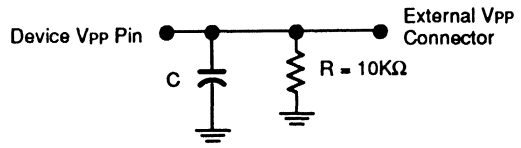


Figure 1.

3. V_{CC} (5.0 V) to V_{PP} (12.0 V) DC/DC Convertor

A monolithic DC/DC convertor from Valor Electronics, the PM9006, is appropriate for the digital world to supply the 12.0 V ±0.6 V V_{PP} voltage. The V_{PP} voltage is generated on chip using the standard system V_{CC} (5.0 V) voltage. Standard TTL commands are used to disable the 12.0 V output supply when programming or erasing operations are not intended. The enable ($\overline{E}$) function provides absolute write protection to guarantee against inadvertent program or erasure. Flash memory contentscannot be altered without the active 12.0 V V_{PP} supply. The enable pin also saves system power when DC/DC convertor is not required. The PM9006 has a minimum efficiency of 50% at full load. The PM9006 comes in a 24-pin package.

The Valor PM9006 provides a controlled 12.0 V output that is regulated within the ±5% (±0.6 V) V_{PP} specification. The standard system V_{CC} (5.0 V) supply is converted to the V_{PP} (12.0 V) supply by the DC/DC convertor. The voltage transitions are smooth and protect against destructive positive or negative overshoot.

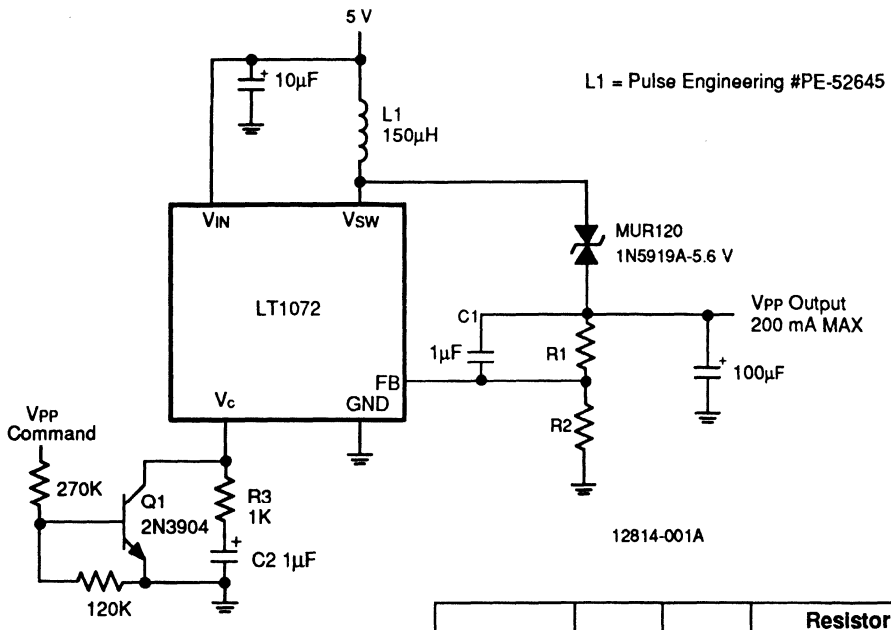
The PM9006 can supply 165 mA of current at the regulated 12.0 V ±0.6 V output. The 5.0 V ±0.5 V DC input supply of the DC/DC convertor uses a maximum of 840 mA of input current. The Am28F010 specifies a maximum V_{PP} current of 30 mA for either the erase or program operations. Actual current required for these operations is substantially lower than this. Given the maximum V_{PP} current of 30 mA for each device, four(4) Am28F010 may be programmed and erased in parallel with one PM9006 device. The PM9006 V_{PP} supply current = 165 mA – 4 x 30 mA of V_{PP} current required for the Flash memory array = 45 mA of additional current available from the DC/DC convertor.

Parallel programming and erasure allows for the most efficient method to reprogram x16 or x32-bit data words. Refer to the previous application note for parallel program and erasue flow charts.

Board Level Resets

System designs should not allow the Flash device to perform any programming or erase operations when the CPU does not have control of the Flash device. Some designs incorporate board level reset circuitry that suspends operation of the local CPU if the V_{CC} level falls below a predetermined value (such as 4.6 V). If this is the case, the reset circuitry should also disable the V_{PP} power supply whenever the CPU is held in reset.

If the local CPU is forced into reset mode while it is programming or erasing the Flash device, the system reset circuit should also terminate that operation. To accomplish this, the PM9006's enable pin should be driven high whenever the reset circuitry is active. Drive the chip enable pin of the PM9006 with the logical OR of the reset circuit's output signal and the chip enable control line to the PM9006. This will disable the V_{PP} supply and hence terminate any programming or erase operation. The Flash device automatically resets to the read mode when V_{PP} is disabled.



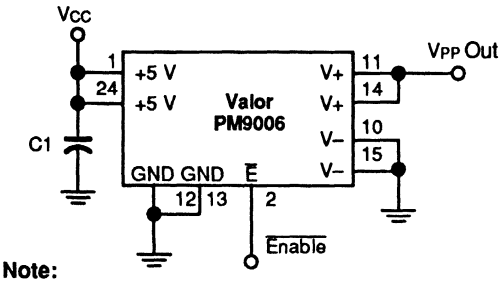
V_{PP} Out	R1	R2	Resistor Tolerance
12.0 V	10.7K	1.24K	1%

Note:

The circuit of Figure 2 will not spuriously overshoot during power-up or power-down. This prevents destruction of the device due to voltages that exceed specification. V_{PP} outputs are predictable and controllable during power supply transitions as a result of the referenced circuit designs. The compensation of the LT1072 causes a very overdamped pulse response. In addition, the control loops of the circuit are functioning even at low supply voltages. Thus the control loop is active before the memory circuits settle and prevents uncontrolled V_{PP} pulse outputs.

Figure 2. Basic Flash Memory V_{PP} Programming Voltage Supply

Please reference the PM9006 data sheet for complete details of device operation. One method of implementing the PM9006 DC/DC convertor is illustrated below.



Note:

Pins 3 through 9 and 16 through 23 are not internally connected to the device and do not need to be driven.

Generate and Control 12.0 V

4. PUMP 5 V TO V_{PP} VOLTAGE WITH ANALOG CIRCUITRY

Flash memories require a V_{PP} voltage of 12.0 V ±0.6 V. It is important to note that V_{PP} voltage must be maintained within the device specification for reliable operation. V_{PP} voltages that exceed 14 V for 20 ns or longer are likely to destroy the device. Thus, we need to carefully control the high voltage programming circuitry. It should be noted that proper design of the V_{PP} circuitry eliminates the issues of device destruction due to application of voltages outside of the specified operating range. In addition, it is preferable to control the V_{PP} voltage with a 5.0 V logic command.

The Starter Kit: V_{PP} Generation and Control

The basic circuit described in Figure 2 satisfies just about all V_{PP} requirements for Flash memories. High voltage is produced by driving the V_{PP} command low. The low V_{PP} command (Trace A, Figure 3) activates the LT1072 switching regulator to drive L1. The resistor network of R1 and R2 provides the DC feedback. C1, R3

and C2 control the AC roll-off. Trace B illustrates the resulting V_{PP} voltage that rises smoothly to the required level. The values specified for R1 and R2 determine the12.0 V output. Leave the 5.6 V zener in the circuit in order to return the output to 0 V when the V_{PP} command goes high. When a 4.5 V minimum output is desired the zener may be omitted. Circuit trimming requirements are eliminated due to the tight internal references of the LT1072. Only precision resistors are required.

The table in Figure 4 gives additional information required to provide greater power output from the referenced circuit. The synchronous switch option of Figure 4 may replace the zener and eliminate its power dissipation.

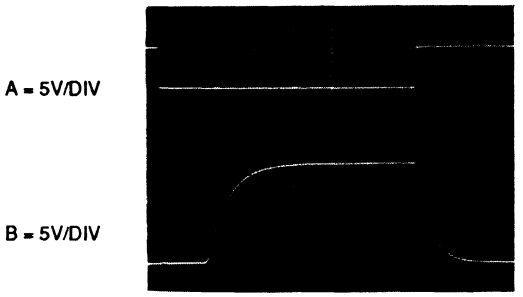
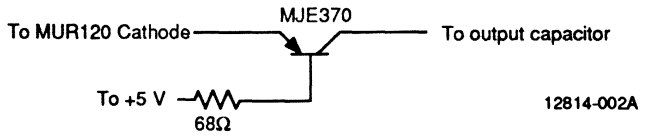


Figure 3. Waveforms for Basic Flash Programming Supply



Power Options for Basic V_{PP} Generator

Output Current	C_{OUT}	Regulator	Inductor	Zener
400mA	200 µF	LT1071	PE-52645	1N5339A or Synchronous Switch Option
800mA	400 µF	LT1070	PE-51516	1N5339A or Synchronous Switch Option

Note:
Assume each Flash device requires 30mA V_{PP} current.

Figure 4. Synchronous Switch Option

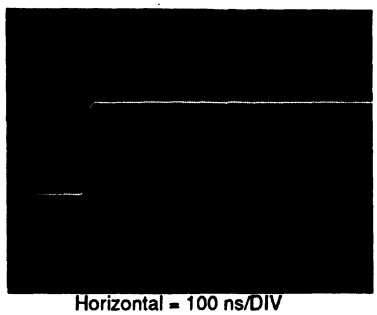


Figure B1. An "Ideal' Flash Memory V_{PP} Output

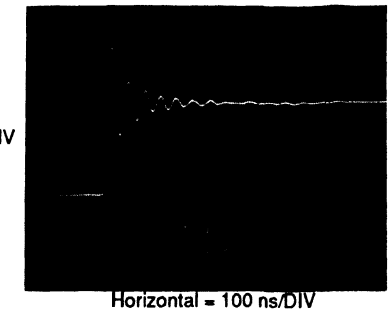


Figure B2. Rings at Destructive Voltages After a PC Trace Run

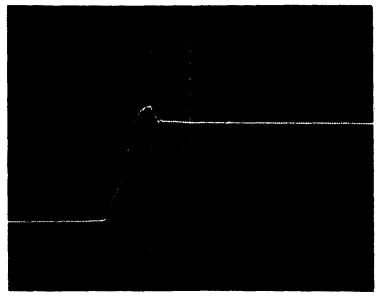


Figure B3.

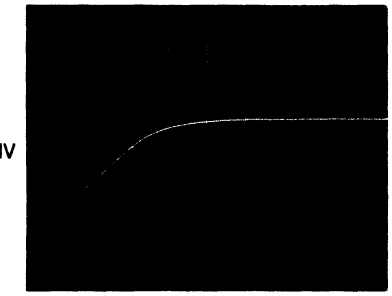


Figure B4.

Note:

Short Circuit Recovery for Poorly (Figured B3) and Properly (Figure B4) Designed Connections. Figure B3's Overshoot on Recovery Can Cause Memory Chip Failures

Transmission Line Effects of Printed Circuit Board Traces on V_{PP} Voltages

One might ask: "Why not use a simple low resistance FET to switch the output of the switching regulator when its level is correctly set?" This sounds good – too good.

In real life, the printed circuit board traces exhibit transmission line effects. Voltages seen at the memory device's pins are not the same as at the output of the regulator. Overshoots result at the junction of the printed circuit board trace and device pins. Thus voltages may exceed device specifications. This concern is compounded since the V_{PP} supply voltages are unusually close to the device's absolute maximum limit of 14V.

Figure B1 illustrates an ideal V_{PP} pulse seen at the output of a simple low loss transistor that is switching the power supply. No overshoot is observed and the V_{PP} pulse settles quickly. The same output is measured (Figure B2) at the memory device pins after running the printed circuit board trace.

Because of mismatching, the PCB trace appears as an unterminated transmission line. Ringing can exceed 20V because of reflections at the junction of the PC trace and device pin. This condition is obviously detrimental to the device. The negative overshoot occurring on the falling edge of the V_{PP} transition may cause equally destructive negative voltages at the device pins.

Properly controlled V_{PP} rise time prevents this type of overshoot. The closed loop circuits discussed earlier eliminate overshoot through controlled edge timings. In addition, the referenced circuits protect the V_{PP} generator against short circuit damage which also protects the memory device.

The V_{PP} output recovery when the diode is removed is shown in Figure B3. Contrast this with Figure B4. Here the diode is in place and the V_{PP} recovery is smooth. Similar considerations apply during power-up/down. During application or removal of power, the V_{PP} generator must not produce spurious output pulses.

V_{PP} outputs are predictable and controllable during transient power supply considerations as a result of the referenced circuit designs. The compensation of the LT1072 causes a very overdamped pulse response. In addition, the control loops of the circuit are functioning even at low supply voltages. Thus the control loop is active before the memory circuits settle and prevent uncontrolled V_{PP} pulse outputs.

Note:

The above circuitry is designed for maximum system protection. Should you desire to modify any circuity, it is advisable to contact Jim Williams of Linear Technology.

This Document was adapted from Linear Technology's Application Note 31 "Linear Circuits for Digital Sytems: Some Affable Analogs for Digital Devotees," written by Jim Williams, February, 1989.

Thin Small Outline Package

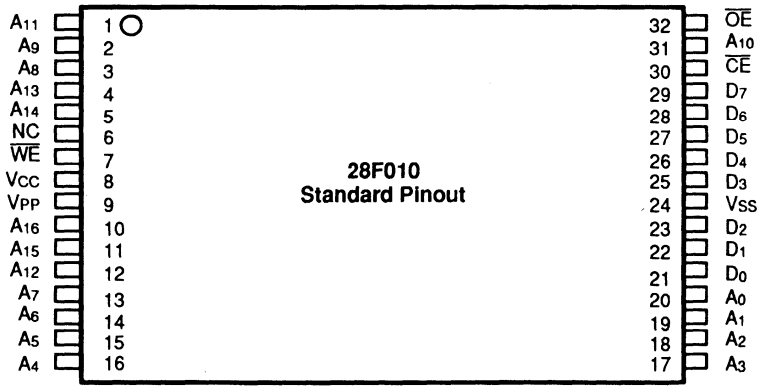
THIN SMALL OUTLINE PACKAGE (TSOP) DESCRIPTION

AMD presents the Thin Small Outline Package. The TSOP is the industry's leading edge plastic, surface mountable memory package today. System requirements for higher density and smaller form fit memory arrays are driving this package evolution. TSOP offers a form fit close to that of bare die yet provides the added benefit of being shipped from the factory completely tested, something not available with bare die. This increases system yield because there is no loss due to cleanroom assembly related defects and/or parametric failures. In addition to supporting Flash memory technology, AMD may also support EPROM (OTP/Express ROM™) technology in TSOP.

Primary Characteristics

- JEDEC/EIAJ standard dimensions and 32-pin pinout
- Standard and reverse pinout options
- Maximum package thickness of 1.27mm

This is AMD's initial offering in state of the art small form fit packaging. The 32-pin package is available in the 8 mm x 20 mm x 1.27 mm package outline. As densities increase, package leadcount will also.



28F010 128K x 8 Flash Memory in 32 Lead TSOP

Packaging Evolution

The continuing trend toward smaller systems and/or higher density memory arrays

Computers:	Desktop	Notebook	Palmtop
Disk drives:	3–1/2"	2–1/2"/Flash "Disk"	Flash "Disk"
Instrumentation:	Benchtop	Portable	Handheld

has led to a significant evolution in newer small form fit packaging. This trend is outlined below.

Package Type	Package Volume (cubic inchs)
PDIP (100 mil Pitch)	0.18
Slim DIP (100 mil Pitch)	0.09
ZIP (100 mil Pitch)	0.072
SOIC/SOJ (50 mil Pitch)	0.075
PLCC (50 mil Pitch)	0.045
TSOP (20 mil Pitch)	0.01

The TSOP is not only suited for standard printed circuit board and single in-line Memory Module (SIMM) applications, but is the package of choice in the exploding new growth area of solid state memory cards. These high volume applications will quickly prove the reliability of this new package.

TSOP packaging is well suited to high density, small form fit systems. This latest evolution offers significant packaging volume savings in comparison with the above alternatives. Increasingly, TSOP is being used in disk drive controller boards, notebook and palm top PCs, high density memory subsystems, and PCMCIA 68-pin standard memory cards. This is just the beginning.

An emerging market segment with explosive growth is the PCMCIA 68-pin memory card standard. The TSOP can be used to pack both sides of a memory board in order to increase the memory density available within a given space constraint. In addition, the TSOP packaged devices are tested to AMD's standard test flows. This allows AMD to guarantee the highest level of quality and long term reliability.

Minimal Space Requirements

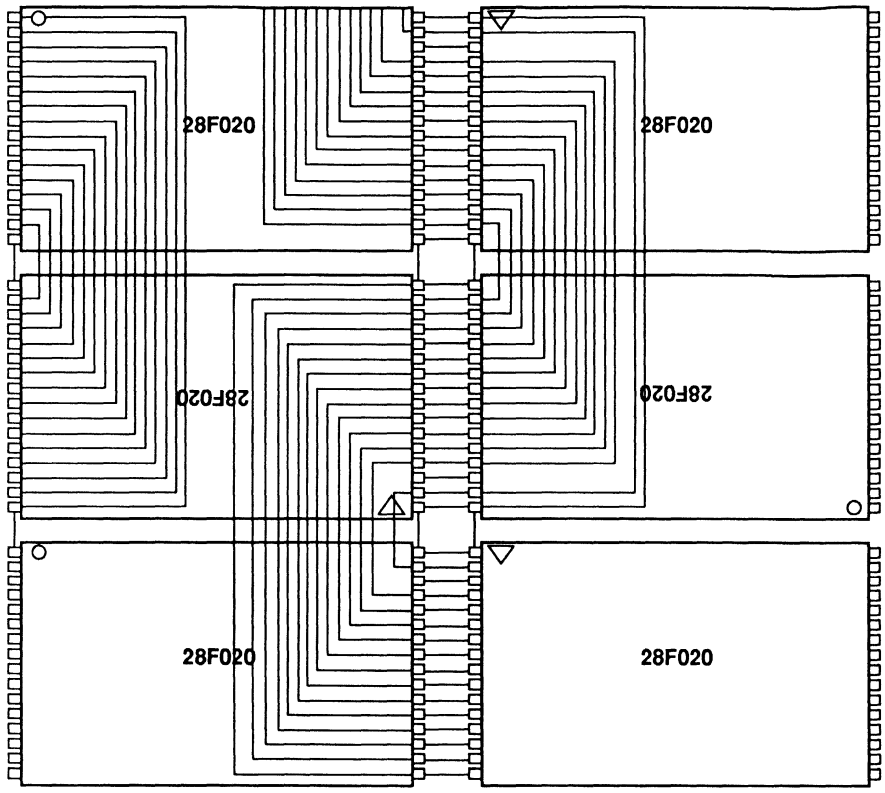
In addition to the TSOP's low height profile, maximum board space saving is achieved with the dual-in-line and standard/reverse pinouts. Board layers can be reduced because traces are routed under the two sides of the package that do not have leads. This allows packages to be mounted side by side and end to end. Packages can be mounted end to end because AMD offers both standard and mirror image reverse pinout packages (see figures below). All pins except chip enable pins can be connected in parallel. This is accomplished by using standard and reverse pinout packages in an alternating sequence as shown below.

HANDLING AND SHIPPING

Shipping Trays

TSOP devices will be shipped in JEDEC Standard dimension trays. JEDEC trays all have the same outside dimensions for easy stacking for use in manufacturing and storage. Trays are designed to prevent TSOP leads from touching any part of the holding tub.

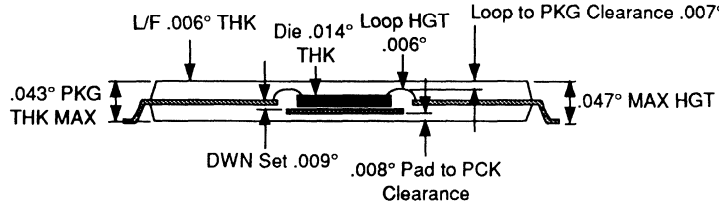
OPTIMAL BOARD LAYOUT WITH TSOP



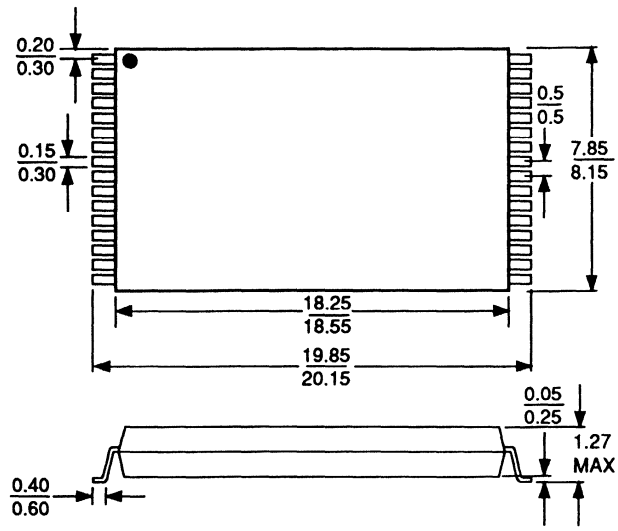
○ = Pin 1 indicator for standard bend pinout

△ = Pin 1 indicator for reverse bend pinout

TSOP Cross-Section



PACKAGE DRAWING*



* For reference only. All measurments measured in millimeters. BSC is an ANSI standard for Basic Space Centering. Package in development.

SECTION 5
Content Addressable Memory (CAM)

Am99C10A

256 x 48 Content Addressable Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **256 word x 48-bit Content Addressable Memory (CAM)**
  - Optimized for Address Decoding in Local Area Networks (LAN) and bridging applications
- **Each CAM word has a 48-bit register and 48-bit maskable comparator**
  - Maskable-bits and maskable-words
- **48-bit input word compared against all 256 words in the CAM in a single cycle**
- **Single and multiple match detection with fast on-chip priority address encoder**
- **Single cycle reset on all 256 words of the CAM Array**
- **100 nsec and 70 nsec cycle time devices available**
- **Flexible operation and diagnostics capability through user programmable control logic**
- **TTL-compatible inputs and outputs**
- **Available in a 28-pin 400 mil CERDIP, 300 mil plastic DIP and 32-pin PLCC**
- **Low power CMOS technology**
  - 880 mW max. operating power
  - 55 mW max. standby

GENERAL DESCRIPTION

The Am99C10A is a high performance Content Addressable Memory (CAM) with a capacity of 256 words and a user-programmable word width of 16 bits or 48 bits. The Am99C10A is ideal for use in high speed Ethernet and FDDI local area network applications where it can function as an address filter and perform the network address look-up function. It can also find use in Database Machines, File Servers, Image Processing, Neural Networks and many other applications.

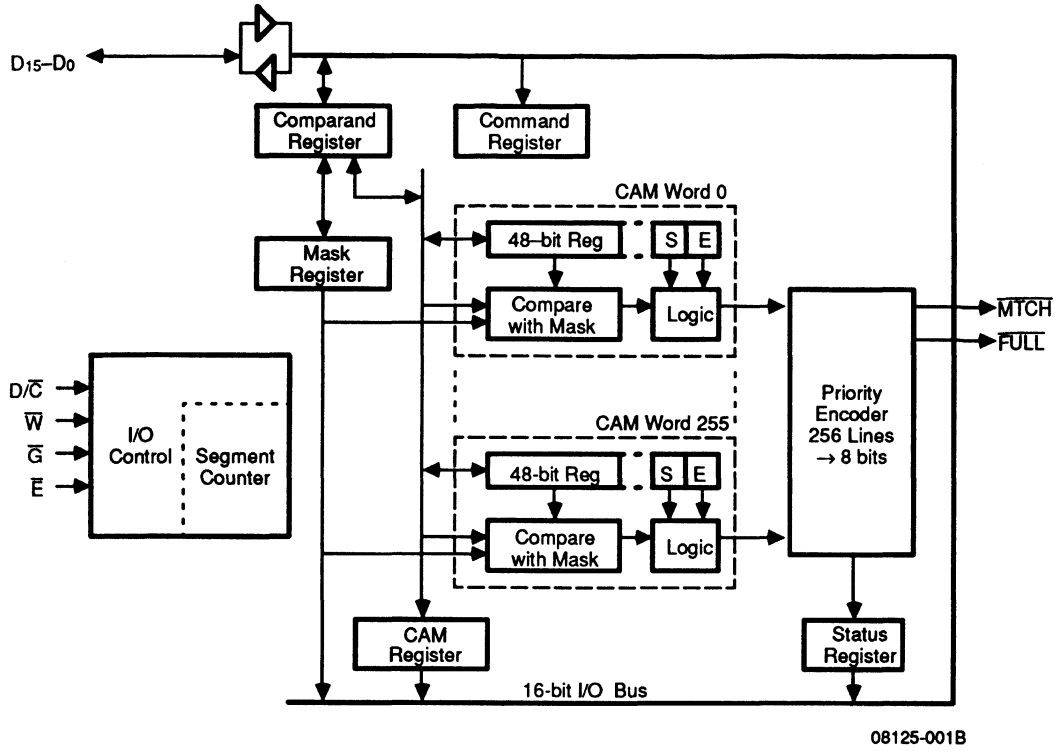
The Am99C10A CAM is composed of 256 words, each consisting of a 48-bit comparator and a 48-bit register. A block diagram of the Am99C10A is shown below. When data (the comparand) is presented to the CAM array, a simultaneous compare operation is performed between the comparand and all data (256 words) in the CAM in a single cycle. When the comparand and a word in the CAM are matched, the on-chip priority encoder generates a match word address identifying the location of the data in the CAM. If multiple matches occur, the encoder generates the lowest matched address. Any or all bits of the comparand value can be selectively masked. The masked bits do not participate in the compare decisions, allowing comparison on a portion of the data word.

The Am99C10A is user programmable. The user can read and write to any location in the CAM Array and to all of the Am99C10A internal registers. Each word in the CAM array can be loaded with data or set to the empty state so that it does not participate in match operations. All words in the CAM Array can be set to empty in a single cycle.

The Am99C10A is manufactured with state-of-the-art CMOS processing technology. It is assembled in a 28-pin, 400 mil CERDIP, a 300 mil plastic DIP, a 32-pin PLCC package, and requires a single 5-V power supply.

Publication# 08125 Rev. F Amendment/0
Issue Date: March 1991

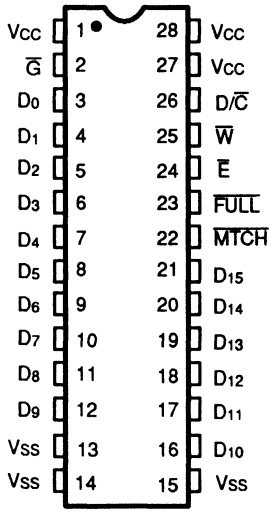
BLOCK DIAGRAM



Am99C10A Block Diagram

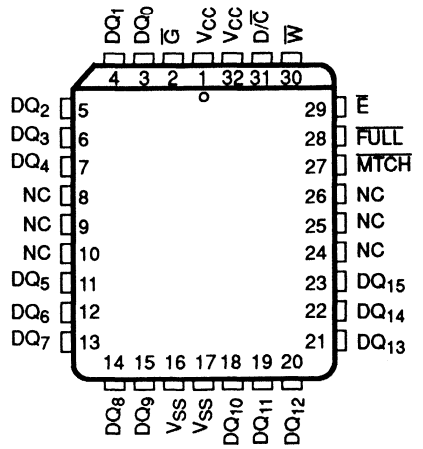
CONNECTION DIAGRAMS

DIP



08125-004A

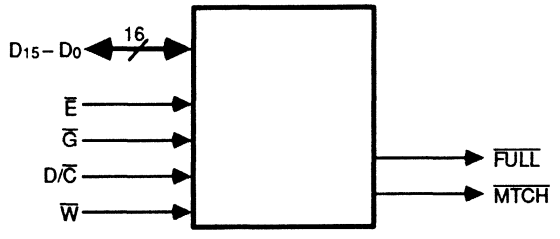
PLCC



08125-040A

Vcc = Power Supply
Vss = Ground

LOGIC SYMBOL

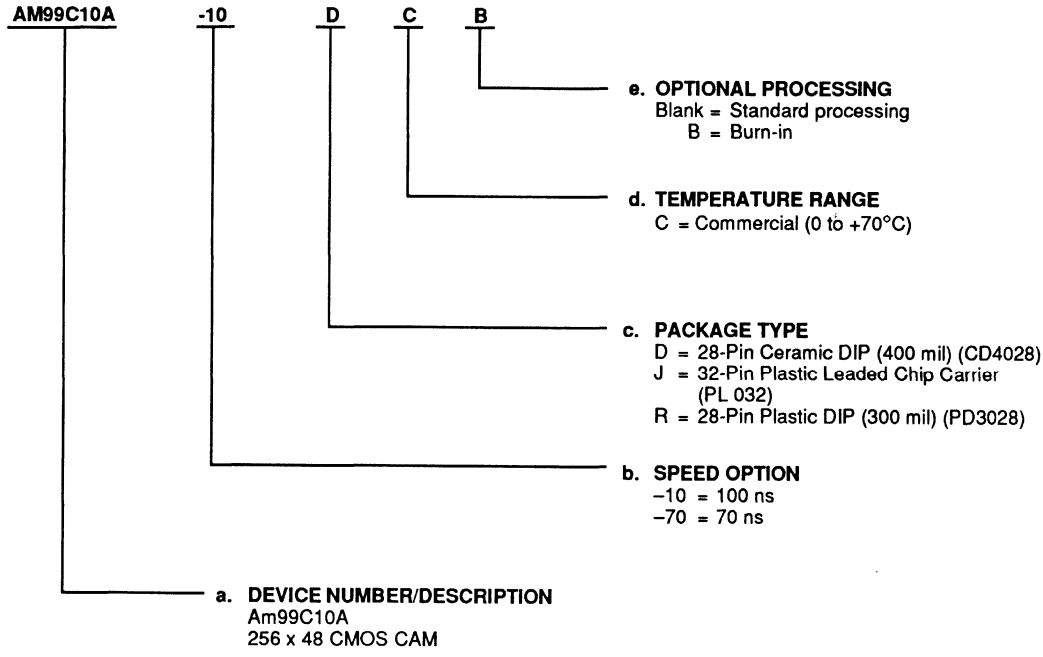


08125-002A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM99C10A	RC, RCB, DC, DCB, JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

D/$\overline{C}$

Data/Command mode selection, Input, TTL

A LOW on this input selects the command mode. A HIGH on this input selects the data mode.

$\overline{W}$

Write enable, Input, TTL

This pin controls the writing of the internal registers and the CAM Array. New data may be written into a register or memory by forcing the appropriate state of D/$\overline{C}$ and $\overline{E}$, and by switching $\overline{W}$ LOW and back HIGH.

$\overline{G}$

Output Enable, Input, TTL

This pin controls reading of the internal registers. A LOW on both the $\overline{E}$ and $\overline{G}$ inputs gates the selected register onto the data bus and turns on the output drivers.

$\overline{E}$

Chip Enable, Input, TTL

A LOW on this input enables the chip operations as specified by the state of D/$\overline{C}$, $\overline{W}$, $\overline{G}$ inputs and the Command Register. A HIGH on this pin powers down the chip. This signal must be low during all operations including match.

D_{15-0}

Data Bus, 16-bit, Bidirectional, Three-state

D0 is the least significant bit position and D_{15} is the most significant bit position. A HIGH on the Data Bus specifies logic 1 and a LOW specifies logic 0. The Data Bus is not driven by the device when $\overline{W}$ is LOW, when $\overline{G}$ is HIGH or when chip enable $\overline{E}$ is HIGH.

$\overline{FULL}$

Address Full, Output, TTL

A LOW on this output indicates that all the words in the 256 address locations in CAM Array are full. A HIGH on this output indicates that one or more words in the CAM Array are still available or that the $\overline{FULL}$ output is disabled. The $\overline{FULL}$ output is in the HIGH state when $\overline{E}$ is HIGH and is valid otherwise.

$\overline{MTCH}$

Match, Output, TTL

A LOW on this output indicates that the masked data of the Comparand Register and one or more words in the CAM Array are matched. A HIGH on this output indicates that a mismatch has taken place or that the match output is disabled. The match output is in the HIGH state when $\overline{E}$ is HIGH and is valid otherwise.

V_{CC}

Power Supply Pin, Input, +5 Volts

V_{SS}

Ground Supply Pin, Input, 0 Volts

FUNCTIONAL DESCRIPTION

The CAM ARRAY is a bank of 256 CAM words, each a combination of a 48 bit wide logic comparator and a 48 bit register, as shown in Figure 1. The CAM Array compares a 48 bit input data word against all of its 256 words simultaneously for logic equality in one cycle. If any of the CAM Array 256 words find an exact match with the incoming bit pattern, the CAM Array raises a Match flag and outputs the 8 bit address of the matching word.

When a Match cycle is initiated, every CAM word compares each bit in its register against the appropriate bit of the incoming 48 bit pattern. Additionally, a logic "1" (HIGH level) set in any Mask Register bit will disable that bit position in the CAM Array. A match is declared if all enabled CAM cells find an exact comparison with the input data. The CAM Array word that finds a match activates an internal signal called the Match Line (ML). There are 256 match lines: ML0 to ML255.

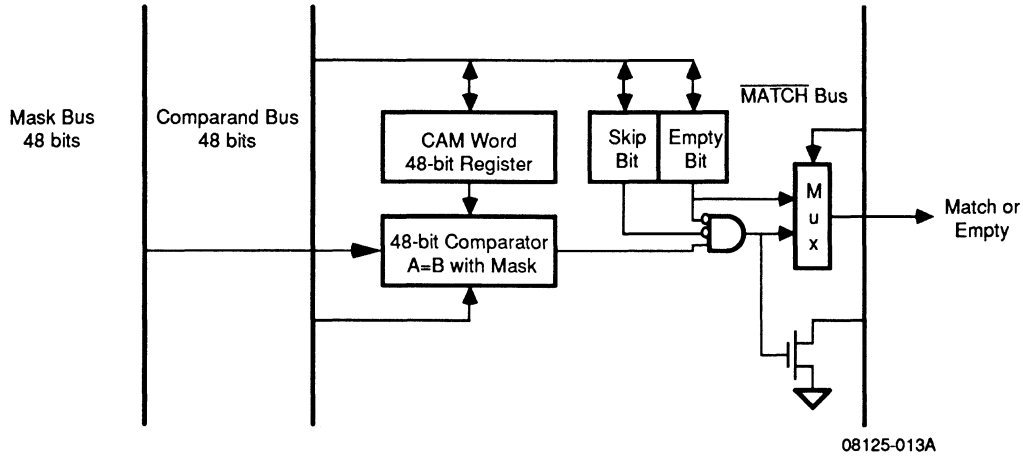


Figure 1. CAM Word Block Diagram

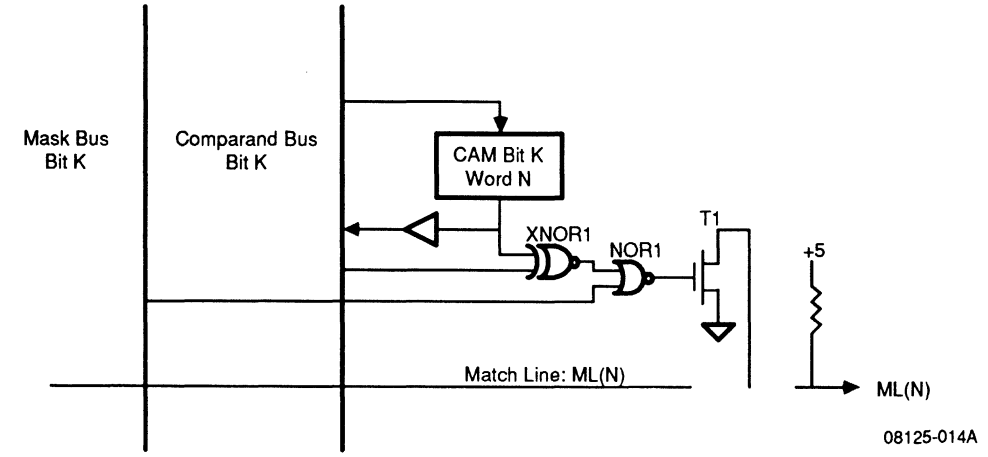


Figure 2. CAM Bit Block Diagram

Each CAM word consists of 48 CAM data bits. Each CAM data bit consists of a register bit latch, an exclusive-NOR comparator, an OR gate for masking, and a transistor for performing a 48-bit wire-AND across the 48 data bits, as shown in Figure 2. The logic comparator exclusive-Nors the contents of the register bit with the corresponding bit of the Comparand Register. A match between the two bits result in a HIGH level at the output of the exclusive-Nor gate (XNOR1). The output of XNOR1 is further gated (Nor function) with a bit of the Mask Register. A HIGH level on either one of the inputs to NOR1 forces its output LOW, indicating a match. The

ML signal will stay HIGH (indicating a match for that CAM word) if all 48 CAM cells of this word have their T1 transistors shut off by their NOR1 gates. If any one of the 48 NOR1outputs is HIGH, the ML line will be forced LOW, indicating a mismatch.

The Priority Encoder identifies the address of the CAM word that found a match. All 256 comparators of the CAM Array receive the same bit pattern for matching at the same time, and more than one of them can find a match with the masked data. All 256 ML lines are presented to the Priority Encoder block that decides which comparator of the ones that activate their MLs has the lowest address. If at least one ML is active the Priority Encoder will activate the $\overline{\text{MTCH}}$ line and at the same time will set the $\overline{\text{MTC}}$ bit in the Status Register. The Priority Encoder will transfer the 8 bit address of the lowest matching CAM Array word to the Status Register.

Each of the 256 words of the CAM Array has two additional bits of memory associated with it – A Skip bit and an Empty bit. These are shown in the CAM Word Block Diagram. The actual size of the CAM is therefore 256 X 50 (48+2). Both the Skip and the Empty bits can disable a match for their word. The Skip bit can be used in situations where there are multiple matches – it gives the user the ability to detect additional words that were matched other than the one with the lowest address. The Empty bit indicates available or empty addresses in the CAM into which data can be written.

The Empty bit is also used by the Priority Encoder. The Priority Encoder identifies the lowest address of an Empty CAM Array word if no match occurred in any of the 256 words. If a match operation did not result in a positive match (the $\overline{\text{MTCH}}$ signal is HIGH) and if the CAM Array is not full (the $\overline{\text{FULL}}$ signal is HIGH) the Priority Encoder will generate the lowest empty address. The 8 bit empty address is accessed by reading the Status Register.

Initializing the CAM

When powering up the CAM, the data and status bits may come up at any state. Opcode 0 is used to globally set the Empty bits of the CAM to "1" and reset the Skip bits to "0". Opcode 0 may be used to empty the CAM during system operation. When command write of Opcode 0 follows a second data write of the 48-bit data write sequence, Opcode 0 must be preceded by Opcode F command write (Set Segment Counter) to ensure proper initialization.

CAM Registers - Reading and Writing

The Am99C10A has 5 programmable registers involved in data transfers. The Command and Status registers are 16 bits wide, and the Comparand, Mask and CAM registers are 48 bits wide. Figure 3. is a model of the Am99C10A registers and their interaction with each other and the CAM Array. Table 1 lists the registers and their respective data sources and destinations.

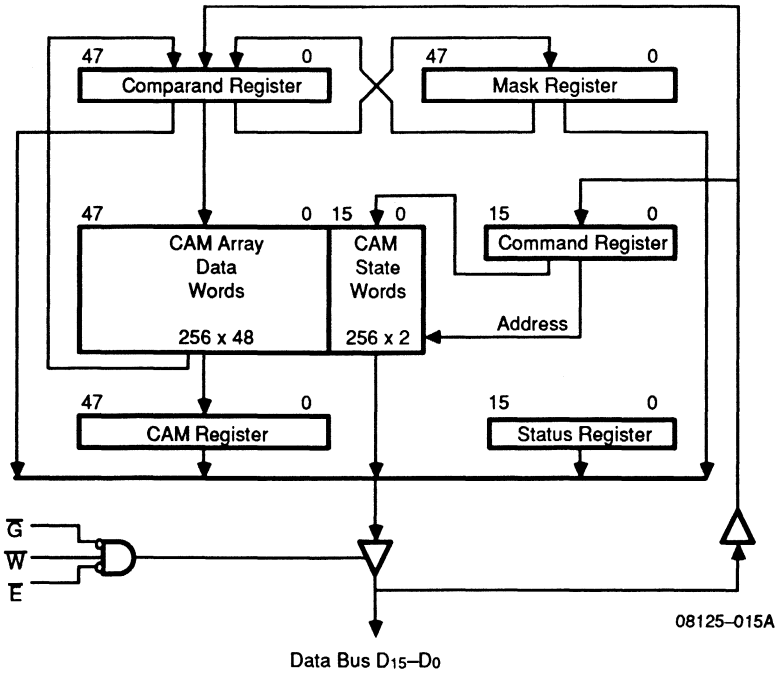


Figure 3. CAM Register Transfer Model

Table 1. Am99C10A Registers

Register	Type	Size	Direction	Data Source	Destination
Command	Cmd	16	Input	D-Bus	—
Status	Cmd	16	Output	—	D-Bus
Comparand	Data	48	In/Out	D-Bus, CAM Array Mask Register	D-Bus, CAM Array Mask Register
Mask	Data	48	Output	Comparand Register	D-Bus, Comparand Register
CAM	Data	48	Output	CAM Array	D-Bus, Comparand Register

Data Bus Transfers

All data is transferred to and from the CAM over the 16-bit bidirectional Data Bus. Data transfer is controlled by a combination of 4 control signals ($\overline{E}$, D/$\overline{C}$, $\overline{W}$, and $\overline{G}$), as described in the Pin Description section.

Data is written into the Am99C10A by placing the data on the Data Bus and activating $\overline{W}$ and $\overline{E}$. When D/$\overline{C}$ is low (Command Write cycle), the input data is loaded into the Command Register. When D/$\overline{C}$ is high (Data Write cycle), the input data is loaded into the Comparand Register.

Data is read from the Am99C10A (output drivers enabled) when $\overline{G}$ and $\overline{E}$ are low and W is high. When D/$\overline{C}$ is low (Status Read cycle) the Status register is gated onto the Data Bus. When D/$\overline{C}$ is high (Data Read cycle) one of the data registers is gated onto the Data Bus. This register is selected by the contents of the Command register. Prior to reading, a command is loaded into the Command Register to select which of the internal registers is to be read.

Data can be read from any register by loading the appropriate command into the Command register; however, data can be written only to the Comparand register. Data to be written to the Mask register or to the CAM array must first be written into the Comparand register and transferred to the Mask register or CAM array word by writing the appropriate transfer command to the Command register.

48-bit Data Transfers

Data is transferred to and from the Am99C10A in 16-bit words. Data for the 16-bit Command and Status registers are transferred in one read or write cycle. Data for the 48-bit Comparand, Mask and CAM registers are transferred to and from the chip in three cycles. Data transfer to and from each 48-bit register is done by dividing each register into three 16-bit segments. A two-bit counter, the Segment Counter is used to select which segment of a 48-bit register is to be loaded or read.

The Segment Counter is a two-bit binary counter that counts from 0 to 2 (modulo-three). It can be preset by writing a command code of "B", "C", "D", or "F" to the Command register. In all four commands bits 10 and 11 (S0, S1) define the binary value (0,1 or 2) to be preset into the counter. Note that a value of 3 (S1,S0 = 11) in these bits will result in a value of 0 in the counter. The counter is also reset to 0 by the Initialize command, Opcode "0".

The Segment Counter is incremented after each data read or write cycle if the CAM is in the 48-bit mode. This allows a 48-bit register to be loaded or read in three successive cycles. The counter is clocked by the LOW-to-HIGH transition of $\overline{W}$ in case of a Data Write cycle and by the LOW-to-HIGH transition of $\overline{G}$ in case of a Data Read cycle.

When the Am99C10A is set to 48-bit mode, the user will normally execute 3 Data Write cycles or 3 Data Read cycles in sequence to transfer a 48 bit data word. At the end of such sequence the state of the Segment Counter is equal to its initial state before the data transfer began. This allows continuous 48-bit transfers without having to preset the Segment Counter between words. This is useful in the CAM's normal operating mode of checking a stream of 48-bit words for a match.

Note that reading a 16-bit State word requires only one cycle. If the CAM is in the 48-bit mode, this data read operation will increment the Segment Counter. Any subsequent cycles that use the Segment Counter have to take this into account.

16-bit Mode Data Transfers

In 16 bit mode the Segment Counter is not incremented and it points to one of the three segments of the Comparand, Mask and CAM Registers. Writing and reading the selected segment of those registers is achieved in one cycle. However, internal transfers between the registers and the CAM Array as well as the Match operation are done on all 48 bits.

CAM Array-Reading and Writing

To write a word into the CAM Array, the data is first loaded into the Comparand register and then transferred from the Comparand register to the register in the selected CAM word by executing a transfer command.

The transfer command is executed by writing a command word (command code = 6 or E) into the Command register. The transfer command contains the address of the CAM word to be written.

To read a word from the CAM Array, data is transferred from the CAM array to either the Comparand or CAM registers by writing the appropriate command (command code = 7 or D, respectively) into the Command register. The transfer command contains the address of the CAM word to be read. The CAM Array word is then read from the register selected by the command.

Writing into the Skip or Empty bit in a CAM word is done directly by writing the appropriate command code (command code = 9 or A, respectively) into the Command register. The command word contains the value of the Skip or Empty bit to be written and the address of the CAM word containing the bit.

The same command codes (9 or A) which are used to set a specific Skip or Empty bit can also be used to set all Skip or Empty bits in the CAM array. If bit 11of these command words is a one, the address portion of the command is ignored and the value of the Skip or Empty bit is written into all words of the CAM array. This is useful in clearing all Skip and Empty bits.

The Skip and Empty bits of a CAM word are also cleared to zero when data is written into the CAM using command code E. This allows writing a new word of data into an empty CAM word without requiring an extra cycle to clear the Skip and Empty bits.

The Skip and Empty bits of all CAM words can be preset to the empty state by writing an Initialize command (command code = 0) to the Command register. Initialize clears all Skip bits to zero and sets all Empty bits to one, corresponding to an empty CAM condition.

To read the Skip and Empty bits of a word from the CAM Array, the State Memory is selected as the source of data driving the Data Bus by writing the appropriate command (command code = 5) into the Command register. That command contains the address of the CAM word whose state is to be read. The State word (i.e., the Skip and Empty bits of the CAM Array word) are then read directly. Reading the State word requires only one Data Read cycle.

Match Operations

Comparison of data in the Comparand against the 256 words of data in the CAM array is called a match operation. The result of a match operation is a match address which appears in the Status register and the activation of the $\overline{\text{MTCH}}$ and $\overline{\text{FULL}}$ flags.

A match operation can be initiated by writing a command into the Command register or by writing data into the Comparand register. A match operation begins after a single data write to the Comparand Register in 16-bit mode or after three data write cycles to the Comparand Register in 48-bit mode. Note that the $\overline{\text{E}}$ line must be kept low for the match time, t_{WMPE} or t_{WMPE48} after write start to allow the match to occur.

If a match occurs, the $\overline{\text{MTC}}$ bit is set in the Status register and the $\overline{\text{MTCH}}$ pin is activated if it has been enabled. The address of the word that matched appears in the lower 8 bits of the Status register. If more than one match occurs, the $\overline{\text{MUL}}$ bit is set in the status register, indicating a multiple match. In this case, the match address is that of the match word with the lowest numerical address. If no match occurs, the $\overline{\text{MTC}}$ bit and $\overline{\text{MTCH}}$ flag are not set, and the address is that of the first empty word, i.e. the empty word with the lowest address.

Both $\overline{\text{MTCH}}$ flag and $\overline{\text{MTC}}$ bit change their state upon 16-bit and 48-bit data write cycles, and upon command write cycle for commands 9 and A. Commands 3, 4, 6, 7 and E change the state of the $\overline{\text{MTC}}$ bit only but do not affect the physical $\overline{\text{MTCH}}$ flag.

The match flag access time is measured from a high-to-low transition of $\overline{\text{W}}$ to the transition of $\overline{\text{MTCH}}$ flag. The state of the $\overline{\text{MTCH}}$ flag changes after the high-to-low transition of the $\overline{\text{W}}$ line on the third data write in the 48-bit mode, on each high-to-low transition of $\overline{\text{W}}$ in 16-bit mode, and after each high-to-low transition of $\overline{\text{W}}$ for command writes which initiate a match. (See Table 2.)

Match and Full Flags

The Am99C10A has two output signals that indicate its status - Full, $\overline{\text{FULL}}$ and Match, $\overline{\text{MTCH}}$.

The Full signal, $\overline{\text{FULL}}$, indicates whether the CAM Array is full or not. A low level on $\overline{\text{FULL}}$ indicates that all 256 words of the CAM Array are full. A HIGH on this output indicates that one or more words in the CAM Array are still available or that the $\overline{\text{FULL}}$ output is disabled. The $\overline{\text{FULL}}$ output can be disabled (= HIGH) under program control or when the chip is disabled (Chip Enable $\overline{\text{E}}$ is high).

The Match signal, $\overline{\text{MTCH}}$, indicates whether a match has been detected, i.e. that the masked data of the Comparand Register and one or more words in the CAM Array are matched. A HIGH on this output indicates that a mismatch has taken place or that the match output is disabled. The $\overline{\text{MTCH}}$ output can be disabled (= HIGH) under program control or when the chip is disabled (Chip Enable $\overline{\text{E}}$ is high).

Status Register Format

The Status register shows the results of match operations and the contents of the Segment Counter. The State Register is read onto the Data Bus by executing a Status Read cycle. Since it takes time to encode a match address (t_{WMPE}), the Status Read cannot immedi-

ately follow a Command Write cycle or a Data Write cycle if a valid match address is sought. A time delay of (t_{WMPE}) after the last command or data write before reading the Status register will guarantee proper address encoding. A Status Read operation does not affect the state of the flags or other register contents.

The Status Register has 3 fields - the Address field (A_0 - A_7), the Segment Counter State (S0 - S1) and the Flags field ($\overline{MTC}$, $\overline{MUL}$ and $\overline{FUL}$), as shown in Figure 4.

$\overline{MTC}$

A LOW on $\overline{MTC}$ (D_{15}) indicates that at least one word in the CAM Array and the masked data of the Comparand Register are matched. A HIGH indicates that no word in the CAM Array found a match. The $\overline{MTC}$ bit is the same as the match output signal $\overline{MTCH}$ during data writes and commands 9 and A.

$\overline{MUL}$

A LOW on $\overline{MUL}$ (D_{14}) indicates that two or more words in the CAM Array match the masked data of the Comparand Register. It is activated during a Match operation and latched by an internal clock at the end of the Match cycle.

$\overline{FUL}$

A LOW on $\overline{FUL}$ (D_{13}) indicates that the CAM Array is full. The $\overline{FUL}$ flag is the same as the full output signal $\overline{FULL}$ except the $\overline{FUL}$ flag cannot be disabled. It is activated during a Match operation and latched by an internal clock at the end of the Match cycle.

S1, S0

The Segment Counter bits (S0 - S1) are driven by the two flip-flops that comprise the Segment Counter. These two bits (D_{10} and D_{11}) reflect the current state of the Segment Counter.

15	14	13	12	11	10	9	8	7	0
$\overline{MTC}$	$\overline{MUL}$	$\overline{FUL}$	0	S1	S0	0	0	Address	

08125-017A

Figure 4. Status Word Bit Assignment

A_7-A_0

Lowest address of the matched word in the CAM when data in the Comparand Register and the data in the CAM are matched ($\overline{MTCH}$ = L, $\overline{MTC}$ = L and $\overline{FULL}$ = don't care). Lowest address of empty 48-bit word in the CAM when data is mismatched and the CAM is not full ($\overline{FULL}$ = H). Address is undefined when data is mismatched and CAM is full. After initialize, $A_7 - A_0$ holds the value FF (Hex). Once a data read or write or a command write is executed, $A_7 - A_0$ holds the address of the first match or the first empty location.

Command Register Format

The Am99C10A can execute a variety of commands. Each command is executed by writing the appropriate command word to the Command register. All commands are executed during the write pulse applied to the the write clock, $\overline{W}$. The format of the Command Register is shown in Figure 5, and a summary of the commands is shown in Table 2.

15	12	11	10	9	8	7	0
F3–F0		S1	S0	X	X	$A_7 - A_0$	

F3-F0: A 4 bit Instruction Code which defines one of sixteen commands.

S0 - S1: Modifier bits for the various commands.

A_0 - A_7 An Address field which selects one of the 256 CAM Array data or State words.

Bits 8, 9: Not used.

08125-018A

Figure 5. Command Register Bit Assignment

Table 2. 99C10A Command Summary

Op Code	Operation		S1	S0	A_0-A_7	Start Match
0	Initialize		X	X	X	X
1	Flag Output control enable/disable		MTCH	FULL	X	X
2	16/48 bit Mode Select		48-bit	X	X	X
3	Comparand Reg. --> Mask Reg		X	X	X	Start
4	Mask Reg. --> Comparand Reg.		X	X	X	Start
5	SIM --> Data Bus		X	X	CAM State	X
6	Comparand Reg. --> CAM Array		X	X	CAM Data	Start
7	CAM Array --> Comparand Reg.		X	X	CAM Data	Start
8	Reserved		X	X	X	X
9	Skip Control	Per Word All Words	0 1	Skip Skip	CAM State X	Start
A	Empty control	Per Word All Words	0 1	Empty Empty	CAM State X	Start
B	Comparand Reg. --> Data Bus		Segment Counter		X	X
C	Mask Reg. --> Data Bus		Segment Counter		X	X
D	CAM Array --> CAM Reg. --> Data Bus		Segment Counter		CAM Data	X
E	Comparand Reg. -->CAM Array, clear S +E		X	X	CAM Data	Start
F	Set Segment Counter		Segment Counter		X	X

Am99C10A COMMAND DESCRIPTIONS

Op Code 0
Initialization

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	Not Used											

08125-019A

All Skip-bits are set to "0" (LOW level) meaning–don't skip, and all Empty-bits are set to "1" (HIGH level) meaning-empty. This is equivalent to resetting the CAM Array. The $\overline{MTCH}$ and $\overline{FULL}$ outputs are enabled. The mode is set to 48-bit mode. The Mask Register and Segment Counter are reset to zero. Subsequent data writes and reads are to and from the Comparand Register.

Op Code 1
Flag Output Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	S1	S0	Not Used									

08125-020A

This command controls the enable and disable of the $\overline{FULL}$ and $\overline{MTCH}$ status output pins. The S0 and S1 fields of this command are latched into the control logic. Once loaded, they control the status output pins $\overline{FULL}$ and $\overline{MTCH}$ as follows: When S0 is 0, the $\overline{FULL}$ output is disabled and remains unconditionally HIGH. When S0 is 1, the $\overline{FULL}$ output is enabled and may be asserted when $\overline{E}$ is low. When S1 is 0, the $\overline{MTCH}$ output is disabled and remains unconditionally high. When S1 is 1, the $\overline{MTCH}$ output is enabled and may be asserted if $\overline{E}$ is low.

Op Code 2
Mode Select

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	S1	Not Used										

08125-021A

This command sets the 99C10 into the 16-bit or 48-bit mode. The S1 bit in the command is loaded into the 16/48-bit mode control register. The 16-bit mode is enabled when S1 is 0, and the 48-bit mode is enabled when S1 is 1. The Am99C10A will remain in the mode selected until another Command Write is executed with Op Code "0" or "2".

Op Code 3
Move Comparand Register to Mask Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	Not Used											

08125-022A

The 48-bit contents of the Comparand Register is loaded into the Mask Register. The Segment Counter is not affected. A Match cycle will begin automatically following this command.

Op Code 4
Move Mask Register to Comparand Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	Not Used											

08125-023A

The 48-bit contents of the Mask Register is loaded into the Comparand Register. The Segment Counter is not changed. A Match cycle will begin automatically following this command.

Op Code 5

Enable Output from State Memory to Data Bus

15	14	13	12	11 10 9 8	7 6 5 4 3 2 1 0
0	1	0	1	Not Used	$A_7 - A_0$

08125-024A

This command selects a State word in the CAM Array as the source of data to be read. The Skip-bit and Empty-bit appear on bits D_{14} and D_{15} of the Data Bus, all other bits of the bus are driven LOW. The Segment Counter is not changed.

Op Code 6

Move Comparand Register to CAM Array

15	14	13	12	11 10 9 8	7 6 5 4 3 2 1 0
0	1	1	0	Not Used	$A_7 - A_0$

08125-025B

The 48-bit contents of the Comparand Register are written into the CAM Array data word. The 16/48 bit mode select setting does not affect this instruction. The Empty-bit and Skip-bit in the State Memory are not changed. The CAM Array address is specified by the Command Register address field. The Segment Counter is not changed. A Match cycle will begin automatically following this command.

Op Code 7

Move CAM Array to Comparand Register

15	14	13	12	11 10 9 8	7 6 5 4 3 2 1 0
0	1	1	1	Not Used	$A_7 - A_0$

08125-026A

The 48-bit contents of the CAM Array data word specified by the address field are loaded into the Comparand Register. The Segment Counter is not changed. The State Memory is not changed. The 16/48 bit mode select setting does not affect this instruction. A Match cycle will begin automatically following this command.

Op Code 8

Reserved

15	14	13	12	11 10 9 8 7 6 5 4 3 2 1 0
1	0	0	0	Not Used

08125-027A

Op Code 9

Skip-bit Control

15	14	13	12	11	10	9 8	7 6 5 4 3 2 1 0
1	0	0	1	0	S0	Not Used	$A_7 - A_0$

08125-028A

When bit 11 in the Command Register is LOW, S0 is loaded into the Skip-bit within the State word location specified by the Command Register address field. A Match cycle will begin automatically following this command.

15	14	13	12	11	10	9 8 7 6 5 4 3 2 1 0
1	0	0	1	1	S0	Not Used

08125-029A

When bit 11 in the Command Register is HIGH, S0 is loaded into all skip-bit memory locations. The Segment Counter is not changed. A Match cycle will begin automatically following this command.

Op Code A

Empty-bit Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	S0	Not Used		$A_7 - A_0$							

08125-030A

When bit 11 in the Command Register is LOW, S0 is loaded into the Empty-bit within the State word location specified by the Command Register address field. A Match cycle will begin automatically following this command.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	1	S0	Not Used									

08125-031A

When bit 11 in the Command Register is HIGH, S0 is loaded into all Empty-bit memory locations. The Segment Counter is not changed. A Match cycle will begin automatically following this command

Op Code B

Enable Output from Comparand Register to Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	S1	S0	Not Used									

08125-032A

This command selects the Comparand Register as the source of data to be read. The S0 and S1 data in the Command Register are clocked into the Segment Counter at the end of this Command Write cycle. When S0 and S1 are both 0 or both 1, the Segment Counter is reset to zero. Subsequent Data Read operations result in data flowing from the Comparand Register segment specified by the Segment Counter to the Data Bus. In 48 bit mode each Data Read cycle will automatically increment the modulo-three Segment Counter.

Op Code C

Enable Output from Mask Register to Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	S1	S0	Not Used									

08125-033A

This command selects the Mask Register as the source of data to be read. The S0 and S1 data in the Command Register are clocked into the Segment Counter at the end of this Command Write cycle. When S0 and S1 are both 0 or both 1, the Segment Counter is reset to zero. Subsequent Data Read operations result in data flowing from the Mask Register segment specified by the Segment Counter to the Data Bus. In 48 bit mode each Data Read cycle will automatically increment the modulo-three Segment Counter.

Op Code D

Move CAM to CAM Register, Enable Output from CAM Register to Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	S1	S0	Not Used		$A_7 - A_0$							

08125-034A

This command selects the CAM Register as the source of data to be read. The S0 and S1 data in the Command Register are moved to the Segment Counter. When S0 and S1 are both 0 or both 1, the Segment Counter is reset to zero. The CAM Array word specified by the address field is transferred to the CAM Register. Subsequent Data Read operations result in data flowing from the CAM Register segment specified by the Segment Counter to the Data Bus. In 48 bit mode each Data Read cycle automatically increments the modulo-three Segment Counter.

Op Code E

Move Comparand Register to CAM (Set Empty-bit and Skip-bit LOW)

15	14	13	12	11 10 9 8	7 6 5 4 3 2 1 0
1	1	1	0	Not Used	$A_7 - A_0$

08125–035A

The 48-bit contents of the Comparand Register is written into the CAM Array data word specified by the address field. The 16/48 bit mode select setting does not affect this instruction. Both the Empty-bit and the Skip-bit in the State Memory address specified by the Command Register address field are set cleared to zero (Not Empty and Don't Skip). The Segment Counter is not changed. A Match cycle will begin automatically following this command.

Op Code F

Set Segment Counter

15	14	13	12	11	10	9 8 7 6 5 4 3 2 1 0
1	1	1	1	S1	S0	Not Used

08125–036B

This command clocks the data in S1, S0 into the Segment Counter. When S1, S0 are both 0 or both 1, the Segment Counter is reset to 0.

Typical Command Sequences

The following are examples of some common sequences of commands. Most command sequences assume segment counter set to zero.

Power-up Initialization

After power-up, the CAM must be initialized. This is done by executing the Initialize command. All the CAM words are reset to the empty state, and the device is set up in the 48-bit mode. Another command is needed if the16-bit mode is desired.

For 48-bit mode:

Command Write 0000 = Initialize (16/48 mode is set automatically to 48 bit mode)

For 16-bit mode:

Command Write 0000 = Initialize (16/48 mode is set automatically to 48 bit mode)
Command Write 2000 = Mode Select (S1=0, Set mode to 16 bit)

Loading CAM Array with Data

After initialization, the CAM must be loaded with data in order to be used. Since all locations are initialized to the empty state, the CAM can be loaded starting from address zero. This is done by loading the Comparand register and writing a command with an op code of E, which will transfer the data to a specified CAM word and clear the Skip and Empty bits of that word.

Filling the CAM in the 48-bit mode is normally done using the following command sequence:

Set Segment Counter to zero
Data Write (D_{15} -- D_0 --> Comparand Register (15-0))
Data Write (D_{15} -- D_0 -->Comparand Register (31-16))
Data Write (D_{15} -- D_0 -->Comparand Register (47-32))
Command Write E0XX = Comparand Register -->CAM Array + Clear S+E
(Repeat for every CAM Array word to be loaded.)

Filling the CAM in the 16-bit mode is done using the following command sequence:

Set Segment Counter to zero
Command Write BX00 = Comparand Register -->Data Bus (Load Segment Counter)
Data Write (D_{15} -- D_0 -->Comparand Register) (segment selected by counter)
Command Write E0XX = Comparand Register -->CAM Array + Clear S+E (all 48 bits are written).

Repeat the last two steps for every CAM Array word to be loaded.
Repeat all three steps when a different 16 bit segment is to be loaded.

Load Mask Register

The mask register is loaded by writing the data into the Comparand Register and then writing a command to transfer the data from the Comparand register to the Mask register.

Set Segment Counter to zero
Data Write (D_{15} -- D_0 -->Comparand Register (15-0))
Data Write (D_{15} -- D_0 -->Comparand Register (31-16))
Data Write (D_{15} -- D_0 -->Comparand Register (47-32))
Command Write 3000 = Comparand Register -->Mask Register

48-Bit Compare for Match (48-bit Mode)

To perform a match operation on new data, the data to be tested is written into the Comparand register, time is allowed for the match operation to be performed, and then the match flag and match address are read from the Status register. Note that no special command is required to start the match: it begins after the last word is loaded into the Comparand register.

Set Segment Counter to zero
Data Write (D_{15} -- D_0 -->Comparand Register (15-0))
Data Write (D_{15} -- D_0 -->Comparand Register (31-16))
Data Write (D_{15} -- D_0 -->Comparand Register (47-32))
Allow time for Match operation
Check $\overline{\text{MTCH}}$ output pin after t_{WMAF48} or t_{WMA}; Status Read,
check bits 13, 14 and 15 ($\overline{\text{MTC}}$, $\overline{\text{MUL}}$, $\overline{\text{FUL}}$) after t_{WMAF48} or t_{WMPE}.

Check for Multiple Matches

Typical match operations yield a single match. Some applications, however may yield multiple matches. In this case, the addresses of each match may be read by successively reading the current lowest address, setting its Skip bit, and reading the next lowest address, etc., until no matches are left.

Status Read, bit 15 ($\overline{\text{MTC}}$) = 0, bit 14 ($\overline{\text{MUL}}$) = 0
Status bits 7-0 contain the address of the lowest word in the CAM that found a match.
Read and save the match address, use it to form the next command

Command Write 94XX = Skip Control - F(9), set bit 11(S1) = 0, set bit 10 (S0) = 1(Skip),
Set the Skip bit: Command bits 7-0 to the lowest matching word address.

Wait for the next Match operation to complete and the Status register to settle
Status Read
Check $\overline{\text{MTC}}$ for match, save the address if $\overline{\text{MTC}}$ =0
Status bits 7-0 contain the address of the lowest word in the CAM that found a match.
Read and save the match address, use it to form the next command

Repeat the last three steps until there are no more matches

Finding and Loading an Empty Location

A CAM word may be empty since initialization or it can be declared empty by setting its Empty bit. Data is added to the CAM by finding an empty location and writing into it. This is done by loading the data to be written into the Comparand register and checking for a match. If the data is not already stored in the CAM, the match operation will respond with the address of the lowest empty word. The address of the empty location may be used to write the new data into the CAM. If a match is found, a copy of the data already exists in the CAM.

Set Segment Counter to zero
Data Write (D_{15} -- D_0 -->Comparand Register (15-0))
Data Write (D_{15} -- D_0 -->Comparand Register (31-16))
Data Write (D_{15} -- D_0 -->Comparand Register (47-32))
Allow time for Match operation and priority encode.
Status Read, check bits 15 ($\overline{MTC}$) should be 1, and 13 ($\overline{FUL}$) should be 1,
Bits 0-7 contain the address of the lowest empty word in the CAM.
Command Write E0XX = Comparand Register -->CAM Array + Flags,
Bits 0-7 should have the address of the empty word from the Status Read.

Reading Data

To read the contents of a word in the CAM Array

Command Write D0XX = CAM Array -->CAM Register -->Data Bus,
Bits 0-7 indicate the address of the word to be read.
Data Read - (CAM Register (15-0) -->D_{15} - D_0)
Data Read - (CAM Register (31-16) -->D_{15} - D_0)
Data Read - (CAM Register (47-32) -->D_{15} - D_0)

Example of a Command Sequence

Table 3 shows the control signals, data bus contents and Segment Counter contents for a typical command sequence. The sequence consists of initialization, filling the CAM Array, and loading the Mask Register. A data pattern is then loaded into the Comparand Register, a match is executed and the sequence terminates with the reading of the Status Register.

Table 3. Command Sequence Example

Cycle Type	Instruction	$\overline{E}$	D/$\overline{C}$	$\overline{W}$	$\overline{G}$	Data Bus (Hex)	Segment Counter Before	Segment Counter After	Operation
Command Write	Initialize	L	L	C	H	0XXX	XX	00	Set default conditions (repeat)
Data Write	—	L	H	C	H	3210	00	01	D_{15}–D_0 —> Comparand Reg (15–0)
Data Write	—	L	H	C	H	7654	01	10	D_{15}–D_0 —> Comparand Reg (31–16)
Data Write	—	L	H	C	H	BA98	10	00	D_{15}–D_0 —> Comparand Reg (47–32)
Command Write	Comparand Reg. —> CAM	L	L	C	H	E000	00	00	"BA9876543210" into CAM word 0
⋮	⋮					⋮	⋮	⋮	⋮
Data Write	—	L	H	C	H	1111	00	01	D_{15}–D_0 —> Comparand Reg (15–0)
Data Write	—	L	H	C	H	2222	01	10	D_{15}–D_0 —> Comparand Reg (31–16)
Data Write	—	L	H	C	H	4444	10	00	D_{15}–D_0 —> Comparand Reg (47–32)
Command Write	Comparand Reg. —> CAM	L	L	C	H	E0FF	00	00	"444222211111" into CAM word 255
Data Write	—	L	H	C	H	00FF	00	01	D_{15}–D_0 —> Comparand Reg (15–0)
Data Write	—	L	H	C	H	0000	01	10	D_{15}–D_0 —> Comparand Reg (31–16)
Data Write	—	L	H	C	H	FF00	10	00	D_{15}–D_0 —> Comparand Reg (47–32)
Command Write	Comparand Reg. —> Mask Reg.	L	L	C	H	3000	00	00	"FF00000000FF" into Mask Register
Data Write	—	L	H	C	H	7654	00	01	D_{15}–D_0 —> Comparand Reg (15–0)
Data Write	—	L	H	C	H	BA98	01	10	D_{15}–D_0 —> Comparand Reg (31–16)
Data Write	—	L	H	C	H	FEDC	10	00	D_{15}–D_0 —> Comparand Reg (47–32)
Wait (Match)	—	L	X	H	H	XXXX	00	00	Compare "XXDCBA9876XX" against CAM
Wait (Encode)	—	L	X	H	H	XXXX	00	00	Encode match address —> Status reg
Status Read	—	L	L	H	C	Status	00	00	Check Flags

L = LOW
H = HIGH
C = LOW going pulse

CAM Applications

Content Addressable Memory (CAM) devices have many potential applications. The availability of high density CAM devices such as the Am99C10A will allow many applications to be developed which were not practical in the past because of lack of CAM devices. Some of these application areas are:

Local Area Network (LAN) bridge address filtering
Local Area Network (LAN) ring message insertion and removal

Data base machine support - Search and sort accelerators
Pattern recognition - String search engines, etc.
Image processing and machine vision - Pattern recognition, Image registration, etc.
Neural net simulation
AI language support - (LISP, etc.) garbage collection support, PROLOG accelerators, etc.

Local Area Network Bridge Address Filtering

Bridges between high speed Local Area Networks (LAN) provide a good example of CAM use. A LAN bridge provides transparent communication between two networks. An example is a bridge between a 100MBit/second FDDI network and an Ethernet network. A block diagram of such a network system is shown in Figure 6, and a block diagram of the bridge is shown in Figure 7.

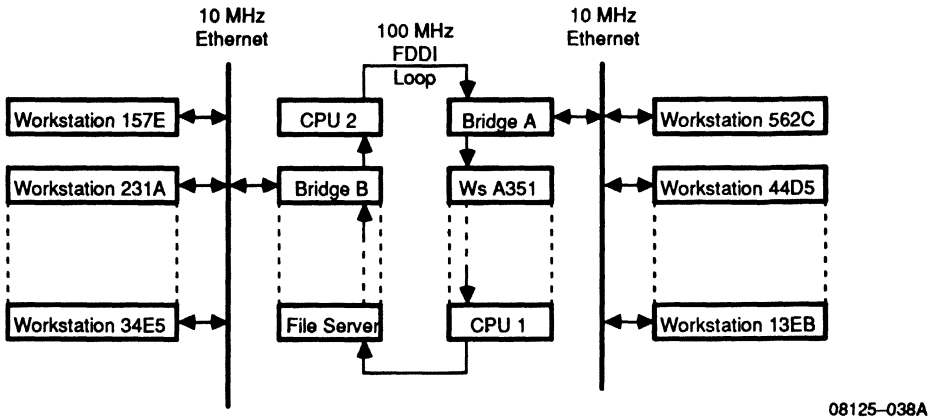


Figure 6. FDDI-Ethernet Network System

The function of the FDDI-Ethernet bridge is to pass messages between the two networks in order to allow the various workstations to communicate. Messages are sent according to unique 48-bit addresses assigned to each workstation. Each message contains the source address and the destination address. The notations shown in the workstation boxes in Figure 6 are assumed to be examples of these addresses: e.g. 157E, 231A, etc.. F

Let us assume that workstation 562C sends a message to workstation 231A. In order for this to occur, the first FDDI-Ethernet bridge must pass along the address to the FDDI loop. The second bridge must recognize that the message is for one of the workstations on its Ethernet LAN and pass it along to workstation 231A.

The problem for the FDDI-Ethernet bridge is to recognize-in time-that the message is for a station on its Ethernet LAN and no other. There could be 4000 workstations on the Ethernet LAN. This means that the bridge must check the message destination address against 4000 addresses in order to determine whether to accept the message and pass it on to the Ethernet.

Address identification must be done quickly. The message acceptance decision must be made before the arrival of the next message, i.e. within the minimum message time. If the minimum message length is 9 bytes on a 100 mbit/sec FDDI network, the decision must be made in 720 ns, including 480 ns to acquire the address. The Am99C10A can do the job in 480+100=580 ns. At these speeds, the Am99C10A is not only effective, it is the only practical, cost effective approach.

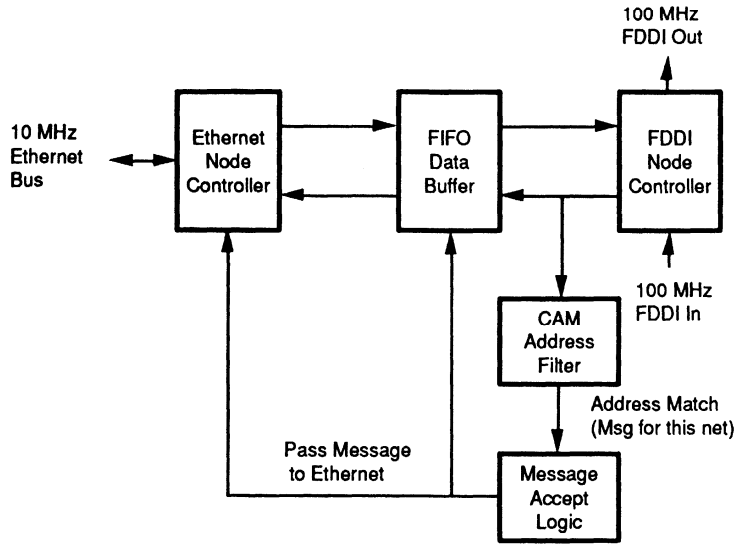


Figure 7. FDDI-Ethernet Bridge Block Diagram

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +150°C
Voltage on Any Pin with Respect to GND	–0.5 to + 7.0 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (T_C)	0 to + 70°C
Supply Voltage (V_{CC})	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS are valid over the operating range unless otherwise specified. All values are guaranteed maximum type limits.

Parameter Symbol	Parameter Description	Test Conditions	70 ns		100 ns		Unit
			Min.	Max.	Min.	Max.	
I_{OH}	Output High Current	V_{OH} = 2.4 V, V_{CC} = 4.5 V	–1.6		–1.6		mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V	+2.4		+2.4		mA
V_{IH}	Input High Voltage		2.2	V_{CC} + .5	2.2	V_{CC} + .5	V
V_{IL}	Input Low Voltage	(Note 3)	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$		2.0		2.0	µA
I_{OZ}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{E} \ge V_{IH}$ or $\overline{G} \ge V_{IH}$		2.0		2.0	µA
I_{CC1}	Static Operating Supply Current	$\overline{E} \ge V_{IL}$		70		70	mA
I_{CC2}	Dynamic Operating Supply Current, 48-bit mode	Cycle = 48-bit Data Write		140		110	mA
I_{CC3}	Dynamic Operating Current, 16-bit mode	Cycle = 16-bit Data Write $\overline{E} \ge V_{IL}$, f = 1/t_{WC}		160		130	mA
I_{SB1}	Standby Current TTL Input Levels	$\overline{E} \ge V_{IH}$ V_{CC} Max.		10		10	mA
I_{SB2}	Standby Current CMOS Input Levels	$\overline{E} \ge (V_{CC} - 0.2\ V)$; $V_{IN} \le 0.2$ V or $V_{IN} \ge (V_{CC} - 0.2)$		10		10	mA

AC CHARACTERISTICS

Parameter Symbol	Parameter Description (Note 2)	70 ns		100 ns		Unit	Notes
		Min.	Max.	Min.	Max.		
Common Parameters							
t_{DCS}	D/$\overline{C}$, $\overline{E}$ setup before read or write	0		0		ns	
t_{DCH}	D/$\overline{C}$, $\overline{E}$ hold time after read or write	0		5		ns	
Read Cycle Parameters							
t_{RC}	Read cycle time	70		100		ns	
t_{RP}	Read cycle pulse width	45		75		ns	4
t_{RR}	Read recovery time	20		25		ns	
t_{OLZ}	Output enable time to low Z	10		10		ns	1,3,4
t_{OHZ}	Output disable time to high Z	5	30	5	30	ns	1,3
t_{RA}	Read access time		45		65	ns	
t_{FA}	Flag enable time		25		30	ns	1,6
t_{FH}	Flag disable time		25		30	ns	1,6
Write Cycle Parameters							
t_{WC}	Write cycle time	70		100		ns	
t_{WP}	Write pulse time	40		75		ns	4
t_{WR}	Write recovery time	25		25		ns	
t_{WDS}	Data setup time before write	3		3		ns	
t_{WDH}	Data hold time after write start	15		80		ns	5
t_{WMA}	Match flag access after write start		125		175	ns	5,6,7
t_{WFA}	Full flag access after write end		70		100	ns	6,7
t_{WMPE}	Priority encode after write start		140		200	ns	5
Write Cycle Parameters – 48-Bit Data Write Mode Only							
t_{WC48}	Write cycle time	60		100		ns	
t_{WP48}	Write pulse width	25		75		ns	4
t_{WMAF48}	Match flag access after write start		90		175	ns	5,6,7
t_{WMPE48}	Priority encode after write start		100		200	ns	5

Notes:

1. Parameter guaranteed by design and characterization data but not 100% tested.
2. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified IOL/IOH and load capacitance (see test load A in switching test circuits) unless otherwise noted. Output timing reference is 1.5 V.
3. Test load B. Disable time is measured as the time to a ±500 mV change from prior output level.
4. $\overline{W}$ and $\overline{G}$ may not overlap: i.e., may not both be low at the same time (while $\overline{E}$ is low).
5. Data hold and match timings with respect to leading edge of $\overline{W}$.
6. Test Load C applies.
7. A $\overline{G}$ HIGH to LOW transition will cause the $\overline{MTCH}$ and $\overline{FULL}$ flags to be in an undefined state for a period = t_{RA}.

CAPACITANCE*

Parameter Symbol	Parameter Description	Test Conditions	Max.	Unit
C_I	Input Capacitance	f = 1 MHz, V_{IN} = 0 V	5	pF
$C_{I/O}$	Input/Output Capacitance	f = 1 MHz, $V_{I/O}$ = 0 V	7	pF

Notes:

1. These parameters are guaranteed by characterization but not tested. Measurements performed at T_A = +25°C.

Data Transfer Control Signals

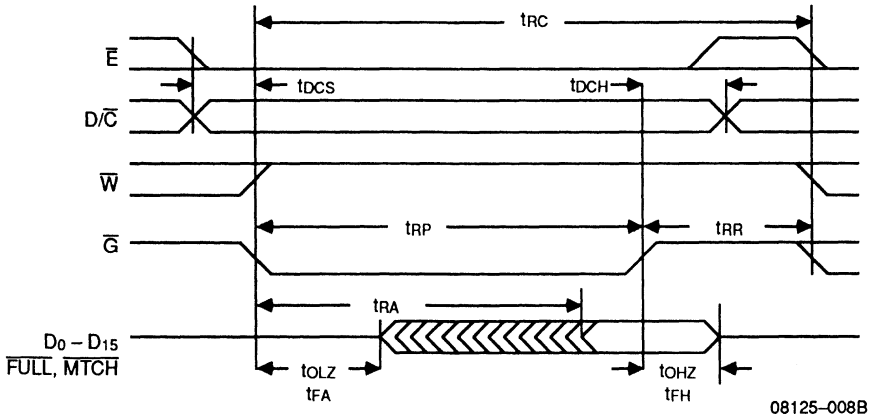
OPERATION MODE	CONTROL SIGNALS				DATA BUS	SUPPLY CURRENT
	$\overline{E}$	D/$\overline{C}$	$\overline{W}$	$\overline{G}$		
Command Write	L	L	L	H	Data In	I_{CC1}, I_{CC2}
Data Write	L	H	L	H	Data In	I_{CC1}, I_{CC2}, I_{CC3}
Status Read	L	L	H	L	Data Out	I_{CC1}, I_{CC2}
Data Read	L	H	H	L	Data Out	I_{CC1}, I_{CC2}
Output Disabled	L	X	H	H	Hi – Z	I_{CC1}
Standby	H	X	X	X	Hi – Z	I_{SB1}, I_{SB2}
Invalid	L	X	L	L	Hi – Z	—

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

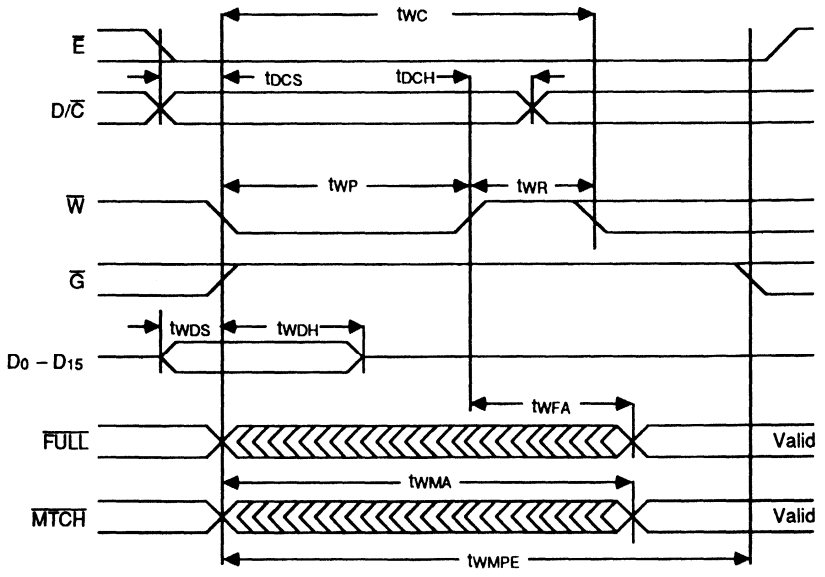


Note:

t_{OLZ} and t_{OHZ} may be measured from $\overline{E}$ transitions provided $\overline{G}$ is Low.

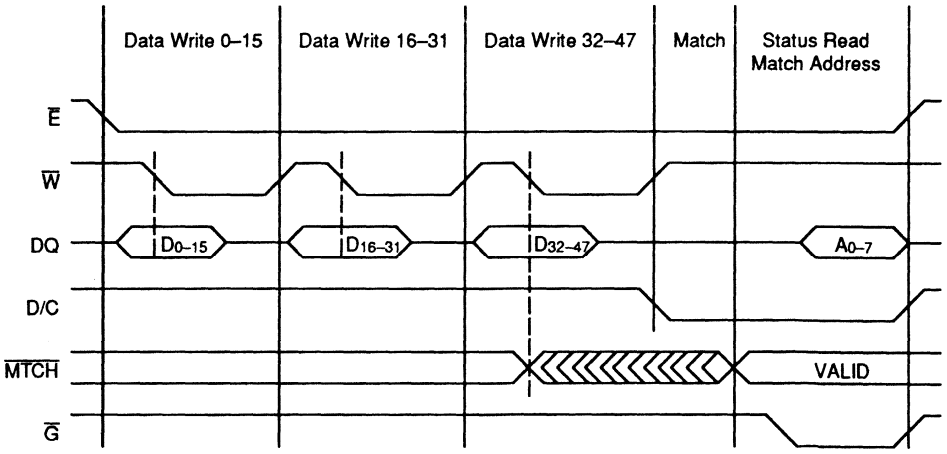
Read Timing Diagram

SWITCHING WAVEFORMS



08125-009B

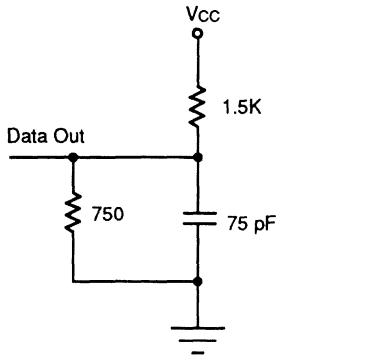
Write Timing Diagram



08125-010B

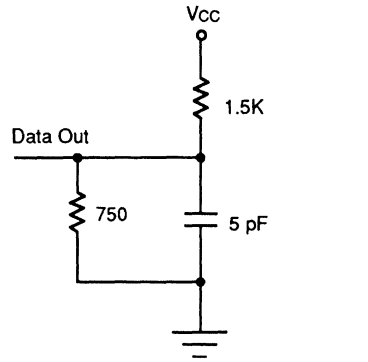
Match Timing Diagram (Reference)

SWITCHING TEST CIRCUITS



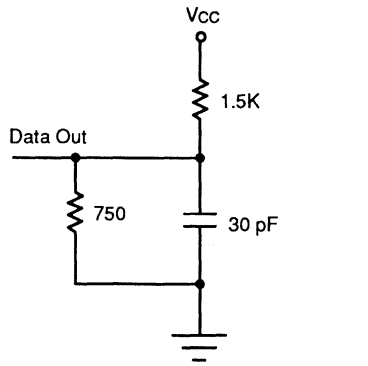
08125–011A

Test Load A



08125–012A

Test Load B



08125–041A

Test Load C

SECTION 6
CMOS First-In First Out (FIFO) Memories

SECTION 6
Introduction to First-In First-Out (FIFO) Memories

WHAT IS A FIFO?

First-in First-out (FIFO) memory provides temporary storage for data words. The dual-port memory device stores the data sequentially; therefore, the first word written to the input port of the FIFO will be the first word available to be read at the output port, followed by the 2nd word, etc. The input and output ports work independently.

Additional data words can be stored in the device as long as the current number of data words stored is less than the number of physical memory locations. When the FIFO is full, the device will be inhibited from reading additional words. Likewise, data words can be read from the FIFO as long as data is currently stored within the FIFO. If no data words are currently stored, then the output port of the FIFO will be inhibited from sending data.

WHEN WOULD YOU USE A FIFO?

The main application for a FIFO is to temporarily store data being transferred across a bus asynchronously. Data can be written into the FIFO at one rate and read out at another rate. Different CPU speeds, data packet sizes, and processor command lengths make the FIFO very attractive as a buffer component. The asynchronous feature may allow the CPU to load data at the CPUs full clock rate disallowing any wait states. The system or peripheral on the receiving side can extract data at its own clock rate. Optimal data throughput can be achieved by choosing the correct FIFO depth predicated on the read and write speeds of the two systems.

HOW FAST SHOULD THE FIFO BE?

The **cycle time** of the FIFO determines the system speed in which the device can operate without requiring system wait states (A wait state is a wasted system timing cycle due to a device requiring additional time to complete its' operation). The FIFO has cycle times associated with each operation, whether a Read, Write, Reset or Retransmit operation. Fortunately, most FIFOs have identical timing parameters for each operation.

The **cycle time** consists of two timing parameters: the **access time** and the **recovery time**.

$$\textbf{cycle time } (t_{xC}) = \textbf{access time } (t_{xA}) + \textbf{recovery time } (t_{xR})$$

The **access time** is the time allotted to complete the actual operation. The **recovery time** is the time allotted for the device to return to a steady state and prepare for the following operation.

AMD's High-Density FIFO part numbers are based on the **access time** of the FIFOs. For example: Am7204A-15PC corresponds to the 4K x 9 FIFO with 15 ns access time. To determine the **cycle time,** you must add the **recovery time** to the **access time** indicated in the part number. The **maximum operating frequency** can then be determined by taking the inverse of the **cycle time** [$1/(t_{xC})$].

Access Time (txA)	Recovery Time (t_{xR})	Cycle Time (t_{xC}) [(t_{xA}) + (t_{xR})]	Max. Oper. Freq. [1/(t_{xC})]
15	10	25	40.0 MHz
25	10	35	28.5 MHz
35	10	45	22.2 MHz
50	15	60	16.6 MHz
65	15	80	12.5 MHz
80	20	100	10.0 MHz

Therefore, for the Am7204-15PC example, the **maximum operating frequency** would be 40.0 MHz.

HOW DEEP SHOULD THE FIFO BE?

The data packet size, or the number of data words transferred at one time, determines the FIFO's density. The data packet may correspond to the data packet used in network communications, to the sector size of a hard drive, or the maximum data accumulated between two processors with different data rates. As system speeds increase, the FIFO must be capable of storing more data packets at one time, since the secondary or peripheral processor may be significantly slower than the main processor.

Am7200

High Density First-In First-Out (FIFO) 256 x 9-Bit CMOS Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **RAM based FIFO**
- **256x9 organization**
- **Cycle times of 35/45/65/80/100 nanoseconds for standard products**
- **Cycle times of 50/65/80/100 nanoseconds for APL products**
- **Asynchronous and simultaneous writes and reads**
- **Low power consumption**
- **Status flags – full, half-full, empty**
- **Retransmit capability**
- **Expandable in both width and depth**
- **Increased noise immunity for $\overline{XI}$ - CMOS threshold**
- **Functional and pin compatible with industry standard devices**

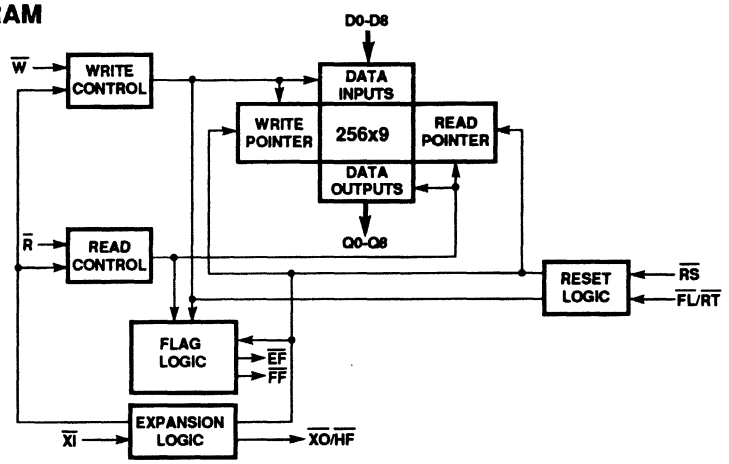
GENERAL DESCRIPTION

The Am7200 is a RAM-based CMOS FIFO that is 256 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 28.5 MHz for Standard Products and 0 to 20 MHz for APL products. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7200 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7200 useful in communication, image processing, mass storage, DSP, and printing systems.

BLOCK DIAGRAM



10804-001A

Figure 1.

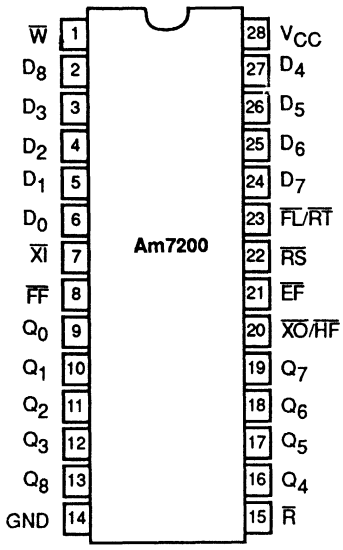
PRODUCT SELECTOR GUIDE

Part Number	Am7200-25	Am7200-35	Am7200-40	Am7200-50		Am7200-65		Am7200-80	
Access Time	25 ns	35 ns	40 ns	50 ns		65 ns		80 ns	
Maximum Power Supply Current	70 mA	60 mA	100 mA	60 mA	90 mA	60 mA	90 mA	60 mA	90 mA
Operating Frequency	28.5 MHZ	22.2 MHZ	20.0 MHZ	15.3 MHZ		12.5 MHZ		10.0 MHZ	
Operating Range	COM'L	COM'L	MIL	COM'L	MIL	COM'L	MIL	COM'L	MIL

Publication# 10804 Rev. E Amendment /0
Issue Date: March 1991

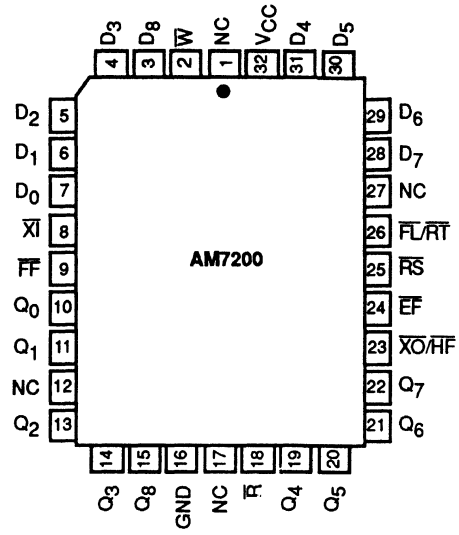
CONNECTION DIAGRAMS

DIPs*



10804-002A

PLCC



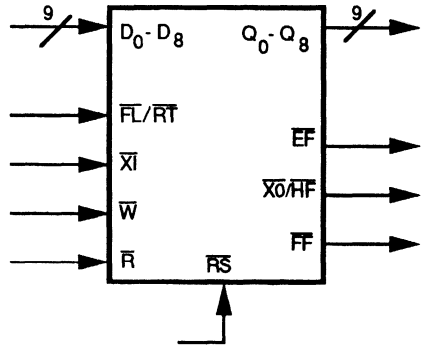
10804-003A

Pin Designations: $\overline{W}$ = Write
$\overline{R}$ = Read
$\overline{RS}$ = Reset
$\overline{FL/RT}$ = First Load/Retransmit
D_x = Data In
Q_x = Data Out
$\overline{XI}$ = Expansion In
$\overline{XO/HF}$ = Expansion Out/Half-Full Flag
$\overline{FF}$ = Full Flag
$\overline{EF}$ = Empty Flag
V_{cc} = Supply Voltage
GND = Ground
NC = No Connect

Note:
Pin 1 is marked for orientation for plastic packages.

* Pinout identical for both plastic and ceramic DIPs.

LOGIC SYMBOL



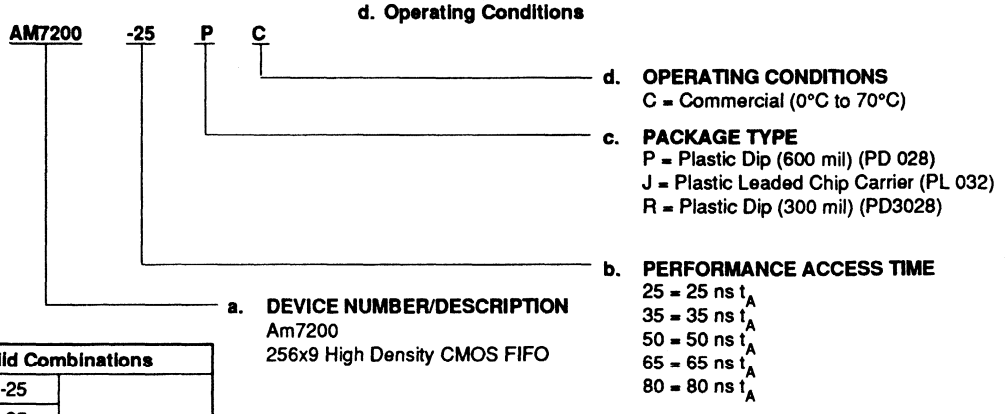
10804-004A

ORDERING INFORMATION

Standard Information

AMD standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Performance
c. Package Type
d. Operating Conditions

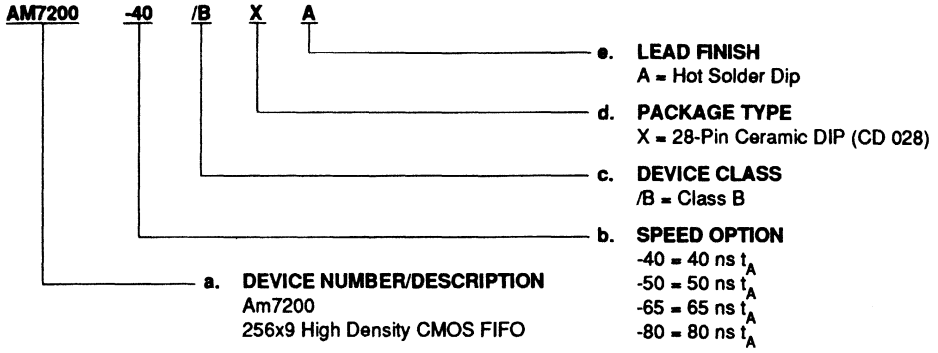


Valid Combinations	
AM7200-25	PC, JC, RC
AM7200-35	
AM7200-50	
AM7200-65	
AM7200-80	

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. Device Number
b. Speed Option
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM7200-40	/BXA
AM7200-50	
AM7200-65	
AM7200-80	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A Tests consist of subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

The Am7200 CMOS FIFO is designed around a 256x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 255. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the Am7200. The write, read, data-in and data-out lines of the Am7200 are connected in parallel, and the Expansion-Out ($\overline{XO}$) and the Expansion-In ($\overline{XI}$) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between $\overline{XO}$ and $\overline{XI}$.

OPERATIONAL DESCRIPTION

Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of $\overline{XI}$ and $\overline{FL}$ are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ($\overline{R}$) and Write ($\overline{W}$) signals must be HIGH t_{RSS} prior to and t_{RSR} after the rising edge of Reset ($\overline{RS}$). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ($\overline{EF}$) being LOW, active, and both the Half-Full ($\overline{HF}$) and Full Flag ($\overline{FF}$) being HIGH, inactive.

Writing Data To The FIFO

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The falling edge of Write ($\overline{W}$) initiates a write cycle. (See Figure 3.) Data appearing at inputs D0-D8 t_{DS} prior to and t_{DH} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The LOW- to-HIGH transition of the Empty Flag ($\overline{EF}$) occurs t_{WEF} after the rising edge of $\overline{W}$ during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag ($\overline{HF}$) will go LOW t_{WHF} after the falling edge of $\overline{W}$ during the write operation which creates the half-full condition. (See Figure 5.) $\overline{HF}$ will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 128 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ($\overline{FF}$) goes LOW t_{WFF} after the falling edge of $\overline{W}$ during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 256 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

A special case of write occurs when a write operation is initiated while the part is full. The next read will cause $\overline{FF}$ to go inactive, and data can then be latched into the FIFO T_{WPF} after the rising edge of $\overline{FF}$ (see Figure 9).

Reading Data From The FIFO

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO is ready to output data. The falling edge of Read ($\overline{R}$) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q0-Q8 t_A after the falling edge of $\overline{R}$, and remains until t_{DV} after the rising edge of R. Q0-Q8 return to a high-impedance state when $\overline{R}$ is inactive, when the FIFO is empty, or when the FIFO is in Depth Expansion Mode but is not active.

The Full Flag ($\overline{FF}$) will go HIGH t_{RFF} after the rising edge of $\overline{R}$ during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag ($\overline{HF}$) will go HIGH t_{RHF} after the rising edge of $\overline{R}$ during the read operation, which eliminates the half-full condition. (See Figure 5). $\overline{HF}$ will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 127 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of $\overline{EF}$ occurs t_{REF} after the falling edge of $\overline{R}$ during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

A special case of read occurs when a read operation is initiated while the part is empty. The data latched in by the next write will be accessed t_A ns after the rising edge of $\overline{EF}$. Read is held active, and cannot be deasserted until T_{RPE} after the rising edge of $\overline{EF}$ (see Figure 8).

Half-Full Flag

The Half-Full ($\overline{HF}$) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 128 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 128 words, and Read and Write pulses are applied simultaneously, the $\overline{HF}$ flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$ will always settle to the correct state after the appropriate delay, t_{WHF} or t_{RHF}. This property of the Half-Full Flag is clearly a function of the dynamic relation between $\overline{W}$ and $\overline{R}$. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

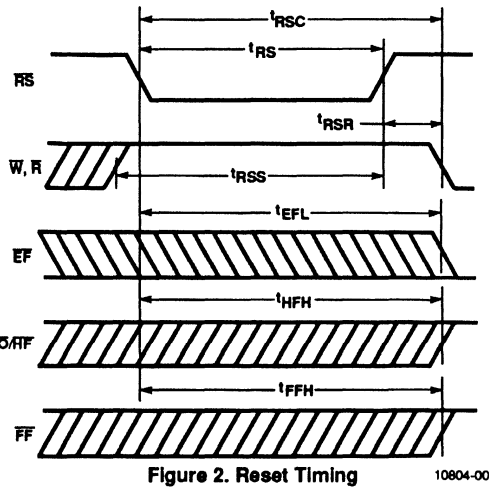


Figure 2. Reset Timing 10804-005A

Table 1. Reset and Retransmit Truth Table
(Single-Device Configuration/Width-Expansion Mode)

Mode	Input			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

Notes:

1. Flags will change to show correct state according to write pointer.
2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2. Reset and First Load Truth Table
(Depth-Expansion/Compound-Expansion Mode)

Mode	Input			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset–first device	0	0	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	$\overline{XO}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

Notes:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
2. Same as during Reset Cycle.
3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

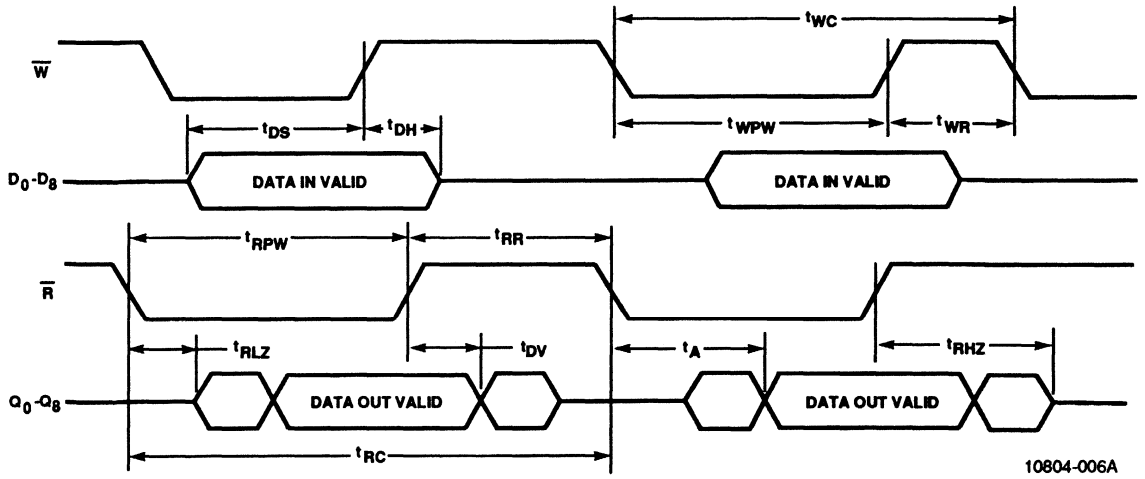


Figure 3. Asynchronous Write and Read Timing

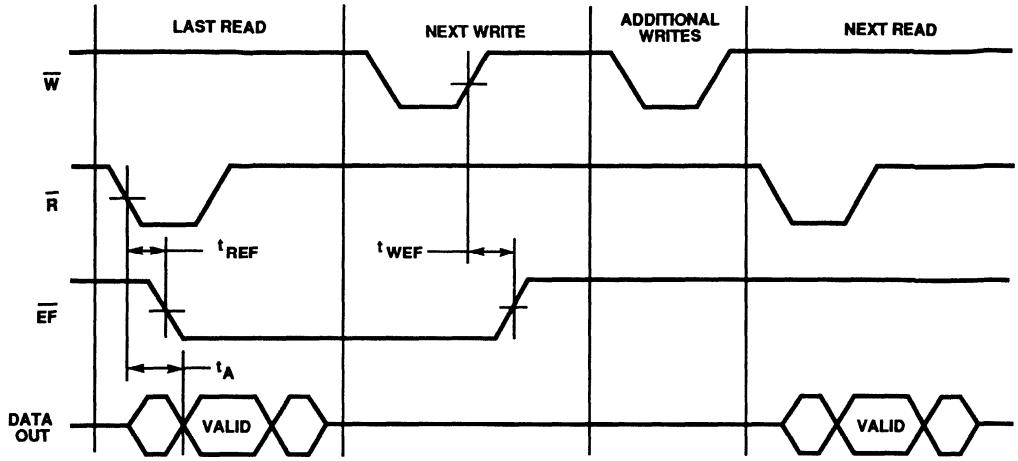
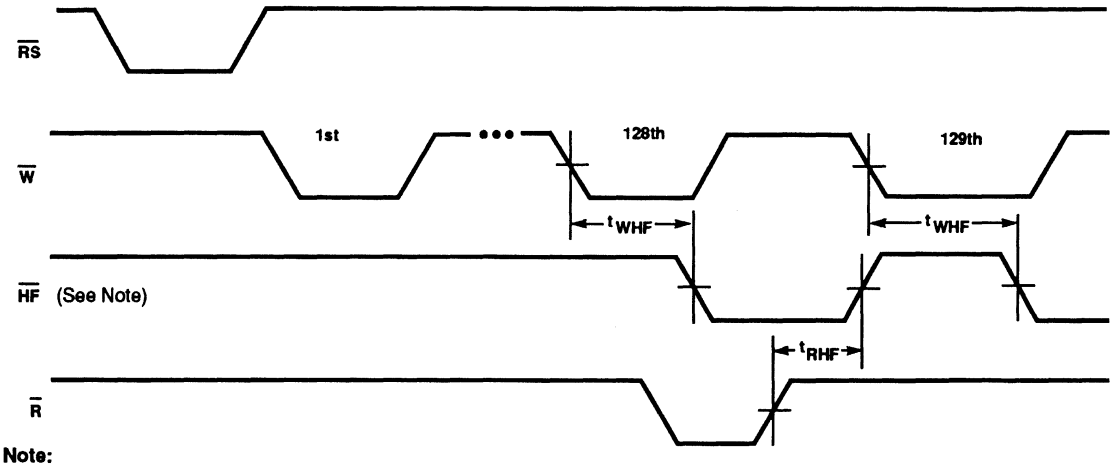


Figure 4. Empty Flag Timing

10804-007A



Note:
Depending on the precise phase of $\overline{W}$ and $\overline{R}$, the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when $\overline{W}$ and $\overline{R}$ are operating asynchronously near half full.

10804-008A

Figure 5. Half-Full Flag Timing

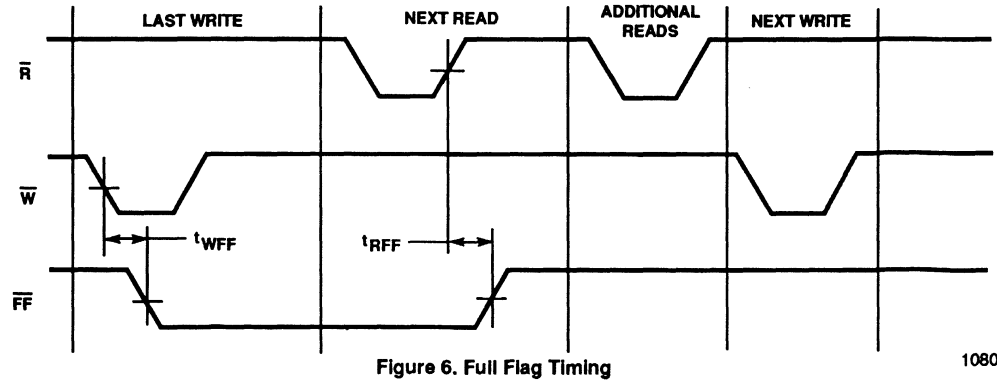


Figure 6. Full Flag Timing

10804-009A

Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 256 or less writes between reset cycles.

The $\overline{FL}/\overline{RT}$ is used as the Retransmit ($\overline{RT}$) input in Single-Device Mode. The retransmit capability is intended for use when there are 256 or less writes between reset cycles. $\overline{RT}$, an active LOW-going pulse of at least t_{RT} in duration, initializes the internal read pointer to address zero and leaves the write pointer unaffected. $\overline{R}$ must be HIGH during the retransmit cycle. The first read cycle should not start until t_{RTR} after the rising edge of $\overline{RT}$. The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO t_{RTC} after the falling edge of $\overline{RT}$. (See Figure 7 and Table 1).

Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ($\overline{XI}$) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The Am7200 can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1.) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated due to the skew between devices. 2.) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one device's flags are used as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time (t_{WEF}, t_{WHF}, t_{WFF}, t_{REF}, t_{RHF}, and t_{RFF}) for each flag has elapsed.

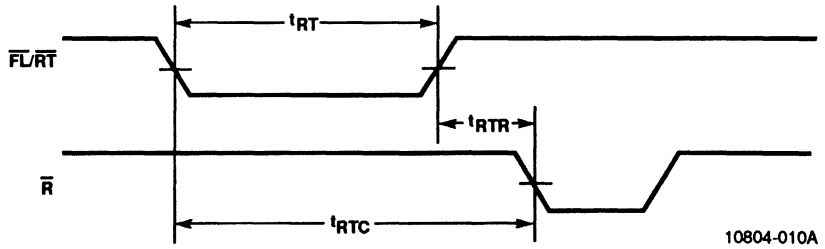
Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ($\overline{XO}$) of one device must be connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device being connected to $\overline{XI}$ of the first device. The device that is to receive data first has its First Load ($\overline{FL}$) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using $\overline{XO}$ and $\overline{XI}$. A LOW-going pulse on $\overline{XO}$ occurs when the last physical location of an active device, address 255, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the $\overline{FF}$ outputs together. Likewise, a composite Empty Flag is created by OR-ing all the $\overline{EF}$ outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

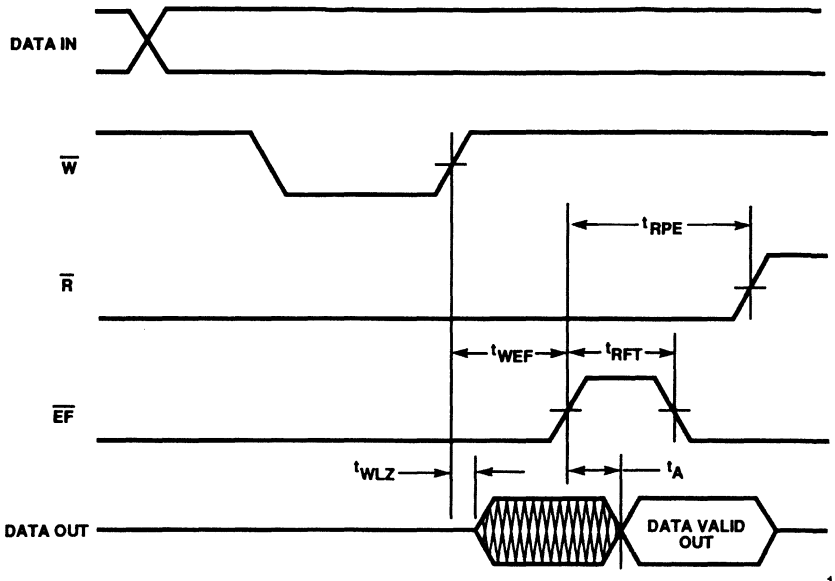
Compound Expansion

FIFOs of greater width and depth than the Am7200 can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)



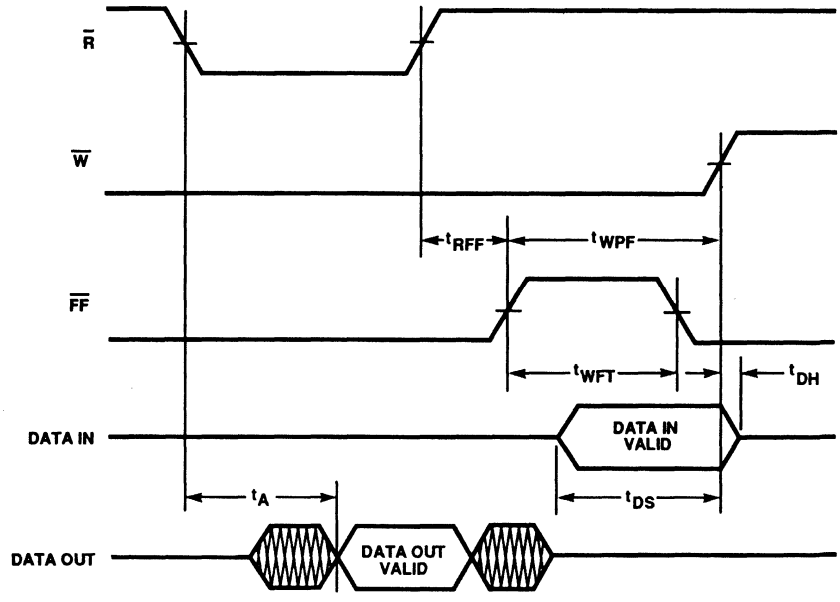
Note:
$\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at t_{RTC}.

Figure 7. Retransmit Timing



Note:
($t_{RPE} = t_{RPW}$, $t_{RFT} = t_{REF}$)

Figure 8. Read Data Flow-Through Mode



Note:
($t_{WPF} = t_{WPW}$, $t_{WFT} = t_{WFF}$)

Figure 9. Write Data Flow-Through Mode

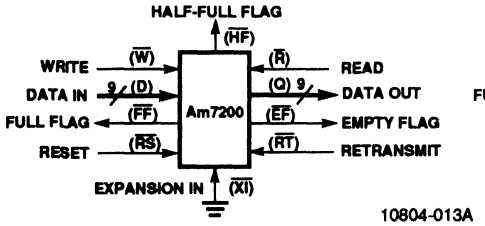


Figure 10. Single FIFO Configuration

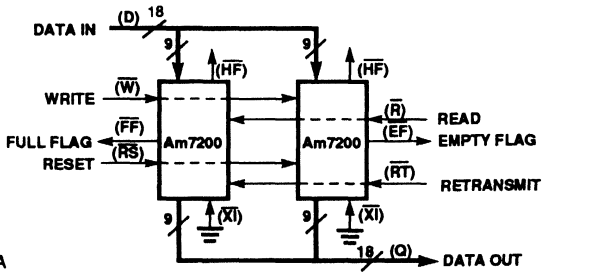


Figure 11. Width-Expansion to Form a 256x18 FIFO

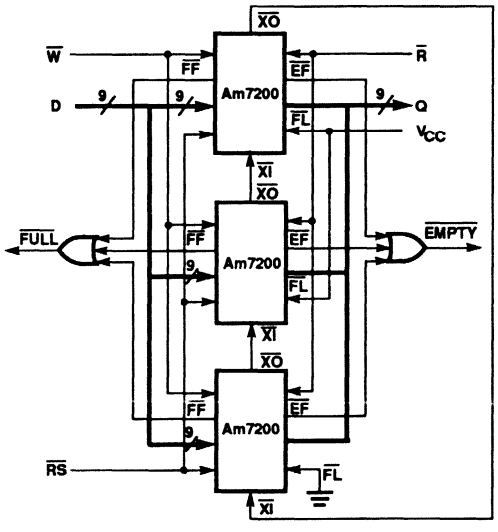


Figure 12. Depth-Expansion to Form a 768x9 FIFO

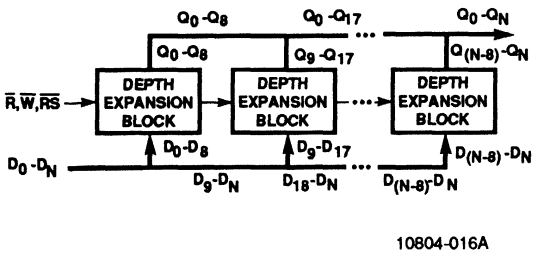


Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques

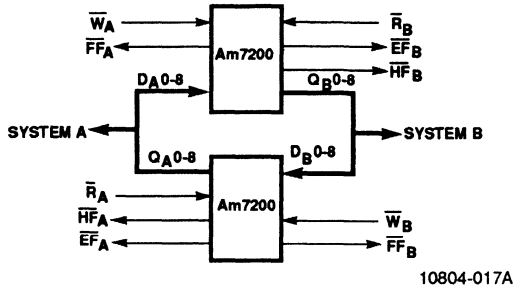


Figure 14. Bidirectional FIFO Mode

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.5 V to +7.0 V
Input voltage	-0.5 V to V_{CC} +0.5 V
Ambient temperature w/Power Applied	-55°C to +125°C
Storage temperature	-55°C to +150°C
Power dissipation	1.0 W
DC output current	50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0°C to 70°C
Supply Voltage (V_{CC})	+4.5V to +5.5V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Am7200-25 t_A = 25 ns		Am7200-35 t_A = 35 ns		Am7200-50 t_A = 50 ns		Am7200-65 t_A = 65 ns		Am7200-80 t_A = 80 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{IL}	Input Leakage Current (any input) (Note 1)	-1	1	-1	1	-1	1	-1	1	-1	1	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	-10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	–	0.8	–	0.8	–	0.8	–	0.8	–	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	–	3.5	–	3.5	–	3.5	–	3.5	–	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = -2 mA	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	V
V_{OL}	Output Logic "0" voltage I_{OL} = 8 mA	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	–	70	–	60	–	60	–	60	–	60	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (Note 4)	–	20	–	20	–	20	–	20	–	20	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} -0.2 V) (Note 4)	–	5	–	5	–	5	–	5	–	5	mA

Notes:

1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

AC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Figures	Am7200-25 Min.	Am7200-25 Max.	Am7200-35 Min.	Am7200-35 Max.	Am7200-50 Min.	Am7200-50 Max.	Am7200-65 Min.	Am7200-65 Max.	Am7200-80 Min.	Am7200-80 Max.	Unit
Write and Flag Timing													
t_{WC}	Write Cycle Time	3	35		45		65		80		100		ns
t_{WPW}	Write Pulse Width	3	25		35		50		65		80		ns
t_{WR}	Write Recovery Time	3	10		10		15		15		20		ns
t_{DS}	Data Setup Time	3,9	15		18		30		30		40		ns
t_{DH}	Data Hold Time	3,9	0		0		5		10		10		ns
t_{WFF}	Write LOW to Full Flag LOW	6,9		25		30		45		60		60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5		35		45		65		80		100	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8		25		30		45		60		60	ns
t_{WLZ}	Write pulse HIGH to data bus at LOW Z (Note 1)	8	5		10		15		15		20		ns
Read and Flag Timing													
t_{RC}	Read Cycle Time	3	35		45		65		80		100		ns
t_{A}	Access Time	3,4,8,9		25		35		50		65		80	ns
t_{RR}	Read Recovery Time	3	10		10		15		15		20		ns
t_{RPW}	Read Pulse Width	3	25		35		50		65		80		ns
t_{RLZ}	Read pulse LOW to data bus at LOW Z (Note 1)	3	5		5		10		10		10		ns
t_{DV}	Data Valid from read pulse HIGH	3	5		5		5		5		5		ns
t_{RHZ}	Read pulse HIGH to data bus at HIGH Z (Note 1)	3		18		20		30		30		30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9		25		30		45		60		60	ns
t_{RHF}	Read HIGH to Half Full-Flag HIGH	5		35		45		65		80		100	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8		25		30		45		60		60	ns
Reset Timing													
t_{RSC}	Reset Cycle Time	2	35		45		65		80		100		ns
t_{RS}	Reset Pulse Width	2	25		35		50		65		80		ns
t_{RSS}	Reset Setup Time	2	25		35		50		65		80		ns
t_{RSR}	Reset Recovery Time	2	10		10		15		15		20		ns
t_{EFL}	Reset to Empty Flag LOW	2		35		45		65		80		100	ns
t_{HFH}	Reset to Half-Full Flag High	2		35		45		65		80		100	ns
t_{FFH}	Reset to Full Flag HIGH	2		35		45		65		80		100	ns
Retransmit Timing													
t_{RTC}	Retransmit Cycle Time	7	35		45		65		80		100		ns
t_{RT}	Retransmit Pulse Width	7	25		35		50		65		80		ns
t_{RTR}	Retransmit Recovery Time	7	10		10		15		15		20		ns

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.5 V to +7.0 V
Input voltage	-0.5 V to V_{CC} +0.5 V
Ambient temperature w/Power Applied	–55°C to +125°C
Storage temperature	–65°C to +155°C
Power dissipation	1.0 W
DC output current	50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices*

Case Temperature (T_C)	-55°C to 125°C
Supply Voltage (V_{CC})	+4.5V to +5.5V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

DC CHARACTERISTICS over MILITARY operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Am7200-40 t_A = 40 ns Min.	Am7200-40 t_A = 40 ns Max.	Am7200-50 t_A = 50 ns Min.	Am7200-50 t_A = 50 ns Max.	Am7200-65 t_A = 65 ns Min.	Am7200-65 t_A = 65 ns Max.	Am7200-80 t_A = 80 ns Min.	Am7200-80 t_A = 80 ns Max.	Unit
I_{IL}	Input Leakage Current (any input) (Note 1)	-10	10	-10	10	-10	10	-10	10	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.2	–	2.2	–	2.2	–	2.2	–	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	–	0.8	–	0.8	–	0.8	–	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	–	3.5	–	3.5	–	3.5	–	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	–	1.5	–	1.5	–	1.5	–	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = -2 mA	2.4	–	2.4	–	2.4	–	2.4	–	V
V_{OL}	Output Logic "0" voltage I_{OL} = 8 mA	–	0.4	–	0.4	–	0.4	–	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	–	100	–	90	–	90	–	90	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (Note 4)	–	25	–	25	–	25	–	25	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} -0.2 V) (Note 4)	–	5	–	5	–	5	–	5	mA

Notes:

1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

AC CHARACTERISTICS over MILITARY operating range unless otherwise specified

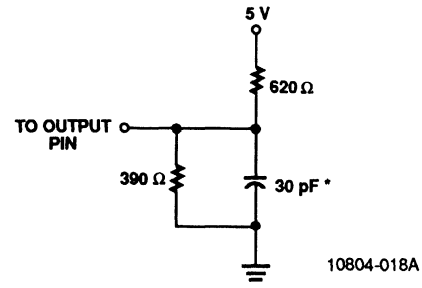
Parameter Symbol	Parameter Description	Figures	Am7200-40 Min.	Am7200-40 Max.	Am7200-50 Min.	Am7200-50 Max.	Am7200-65 Min.	Am7200-65 Max.	Am7200-80 Min.	Am7200-80 Max.	Unit
Write and Flag Timing											
t_{WC}	Write Cycle Time	3	50		65		80		100		ns
t_{WPW}	Write Pulse Width	3	40		50		65		80		ns
t_{WR}	Write Recovery Time	3	10		15		15		20		ns
t_{DS}	Data Setup Time	3,9	20		30		30		40		ns
t_{DH}	Data Hold Time	3,9	0		5		10		10		ns
t_{WFF}	Write LOW to Full Flag LOW	6,9		35		45		60		60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5		50		65		80		100	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8		35		45		60		60	ns
t_{WLZ}	Write pulse HIGH to data bus at LOW Z (Note 1)	8	10		15		15		15		ns
Read and Flag Timing											
t_{RC}	Read Cycle Time	3	50		65		80		100		ns
t_{A}	Access Time	3,4,8,9		40		50		65		80	ns
t_{RR}	Read Recovery Time	3	10		15		15		20		ns
t_{RPW}	Read Pulse Width	3	40		50		65		80		ns
t_{RLZ}	Read pulse LOW to data bus at LOW Z (Note 1)	3	5		10		10		10		ns
t_{DV}	Data Valid from read pulse HIGH	3	5		5		5		5		ns
t_{RHZ}	Read pulse HIGH to data bus at HIGH Z (Note 1)	3		25		30		30		30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9		35		45		60		60	ns
t_{RHF}	Read HIGH to Half Full-Flag HIGH	5		50		65		80		100	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8		30		45		60		60	ns
Reset Timing											
t_{RSC}	Reset Cycle Time	2	50		65		80		100		ns
t_{RS}	Reset Pulse Width	2	40		50		65		80		ns
t_{RSS}	Reset Setup Time	2	40		50		65		80		ns
t_{RSR}	Reset Recovery Time	2	10		15		15		20		ns
t_{EFL}	Reset to Empty Flag LOW	2		50		65		80		100	ns
t_{HFH}	Reset to Half-Full Flag High	2		50		65		80		100	ns
t_{FFH}	Reset to Full Flag HIGH	2		50		65		80		100	ns
Retransmit Timing											
t_{RTC}	Retransmit Cycle Time	7	50		65		80		100		ns
t_{RT}	Retransmit Pulse Width	7	40		50		65		80		ns
t_{RTR}	Retransmit Recovery Time	7	10		15		15		20		ns

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See Figure 15



* Includes jig and scope capacitances.

Figure 15. A.C. Test Load

CAPACITANCE (V_{CC} = 5.0V, T_A = + 25°C, f = 1.0 MHz)

Symbol	Parameter (Note 1)	Conditions	Typ.	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V	5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	7	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

Am7201

High Density First-In First-Out (FIFO) 512 x 9-Bit CMOS Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 512 x 9 organization
- Cycle times of 35/45/65/80/100 nanoseconds for standard products
- Cycle times of 50/65/80/100 nanoseconds for APL products
- Asynchronous and simultaneous writes and reads
- Low power consumption
- Status flags—full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for $\overline{XI}$ – CMOS threshold
- Functional and pin compatible with industry standard devices

GENERAL DESCRIPTION

The Am7201 is a RAM-based CMOS FIFO that is 512 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 28.5 MHz for Standard Products and 0 to 20 MHz for APL products. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7201 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7201 useful in communication, image processing, mass storage, DSP, and printing systems.

BLOCK DIAGRAM

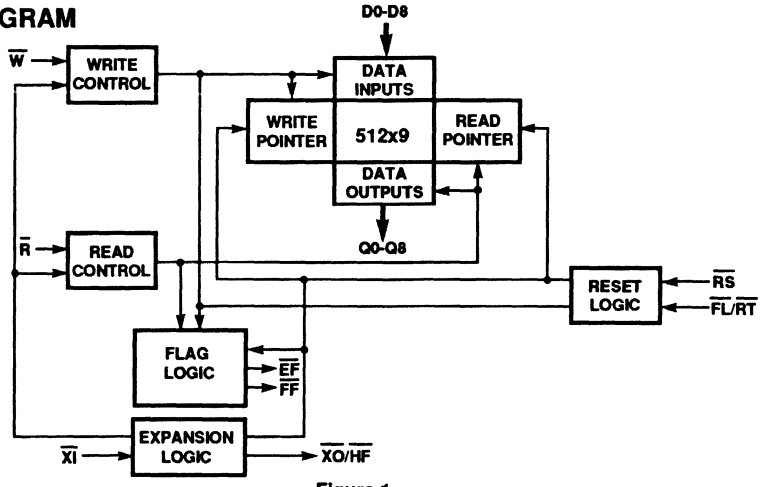


Figure 1.

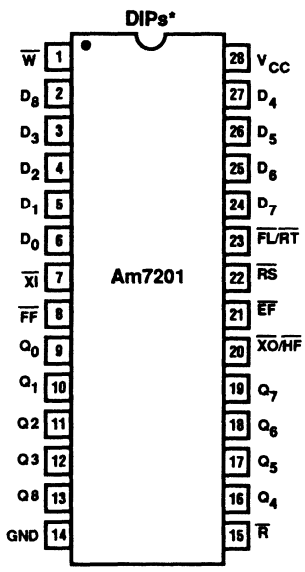
PRODUCT SELECTOR GUIDE

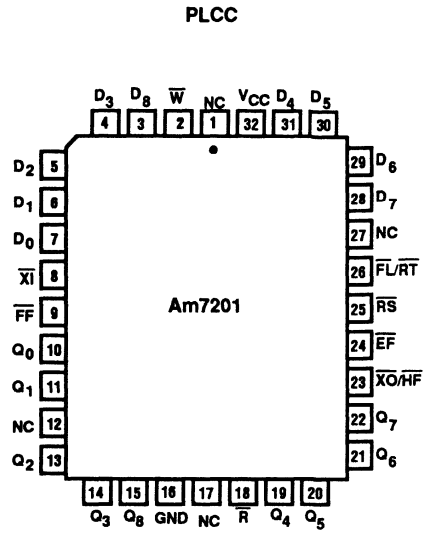
Part Number	Am7201-25	Am7201-35	Am7201-40	Am7201-50		Am7201-65		Am7201-80	
Access Time	25 ns	35 ns	40 ns	50 ns		65 ns		80 ns	
Maximum Power Supply Current	70 mA	60 mA	100 mA	60 mA	90 mA	60 mA	90 mA	60 mA	90 mA
Operating Frequency	28.5 MHz	22.2 MHz	20.0 MHz	15.3 MHz		12.5 MHz		10.0 MHz	
Operating Range	COM'L	COM'L	MIL	COM'L	MIL	COM'L	MIL	COM'L	MIL

Publication # 10175 Rev. F Amendment /0
Issue Date: March 1991

CONNECTION DIAGRAMS

Top View





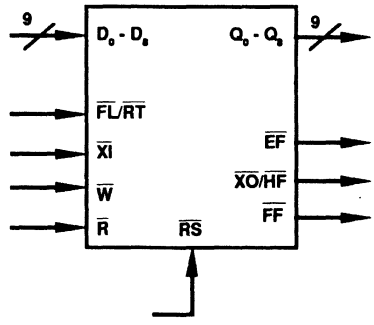
Note: Pin 1 is marked for orientation for plastic packages.

* Pinout identical for both plastic and ceramic DIPs.

PIN DESCRIPTION

$\overline{W}$ = Write
$\overline{R}$ = Read
$\overline{RS}$ = Reset
$\overline{FL/RT}$ = First Load/Retransmit
D_x = Data In
Q_x = Data Out
$\overline{XI}$ = Expansion In
$\overline{XO/HF}$ = Expansion Out/Half-Full Flag
$\overline{FF}$ = Full Flag
$\overline{EF}$ = Empty Flag
V_{CC} = Supply Voltage
GND = Ground
NC = No Connect

LOGIC SYMBOL

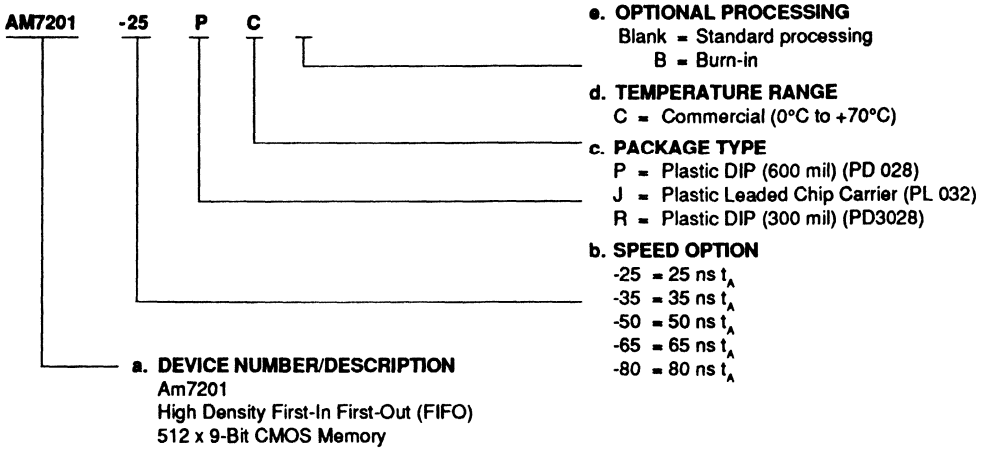


ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

a. Device Number/Description
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7201-25 AM7201-35 AM7201-50 AM7201-65 AM7201-80	PC, JC, RC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM7201 -40 /B X A

e. LEAD FINISH
A = Hot Solder Dip

d. PACKAGE TYPE
X = 28-Pin Ceramic DIP (CD 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
-40 = 40 ns t_A
-50 = 50 ns t_A
-65 = 65 ns t_A
-80 = 80 ns t_A

a. DEVICE NUMBER/DESCRIPTION
Am7201
High Density First-In First-Out (FIFO)
512 x 9-Bit CMOS Memory

Valid Combinations	
AM7201-40 AM7201-50 AM7201-65 AM7201-80	/BXA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Group A Tests

Group A Tests consist of subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

The Am7201 CMOS FIFO is designed around a 512 x 9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 511. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the Am7201. The write, read, data-in and data-out lines of the Am7201 are connected in parallel, and the Expansion-Out ($\overline{XO}$) and the Expansion-In ($\overline{XI}$) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between $\overline{XO}$ and $\overline{XI}$.

OPERATIONAL DESCRIPTION

Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of $\overline{XI}$ and $\overline{FL}$ are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ($\overline{R}$) and Write ($\overline{W}$) signals must be HIGH t_{RSS} prior to and t_{RSR} after the rising edge of Reset ($\overline{RS}$). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ($\overline{EF}$) being LOW, active, and both the Half-Full ($\overline{HF}$) and Full Flag ($\overline{FF}$) being HIGH, inactive.

Writing Data To The FIFO

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The falling edge of Write ($\overline{W}$) initiates a write cycle. (See Figure 3.) Data appearing at inputs D0-D8 t_{DS} prior to and t_{DH} after the rising edge of W will be stored sequentially in the FIFO.

The LOW- to-HIGH transition of the Empty Flag ($\overline{EF}$) occurs t_{WEF} after the rising edge of $\overline{W}$ during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag ($\overline{HF}$) will go LOW t_{WHF} after the falling edge of during the write operation which creates the half-full condition. (See Figure 5.) $\overline{HF}$ will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 256 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ($\overline{FF}$) goes LOW t_{WFF} after the falling edge of $\overline{W}$ during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 512 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

A special case of write occurs when a write operation is initiated while the part is full. The next read will cause $\overline{FF}$ to go inactive, and data can then be latched into the FIFO T_{WPF} after the rising edge of $\overline{FF}$ (see Figure 9).

Reading Data From The FIFO

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO is ready to output data. The falling edge of Read ($\overline{R}$) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q0-Q8 t_A after the falling edge of R, and remains until t_{DV} after the rising edge of R. Q0-Q8 return to a high-impedance state when R is inactive, when the FIFO is empty, or when the FIFO is in Depth Expansion Mode but is not active.

The Full Flag ($\overline{FF}$) will go HIGH t_{RFF} after the rising edge of R during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag ($\overline{HF}$) will go HIGH t_{RHF} after the rising edge of $\overline{R}$ during the read operation, which eliminates the half-full condition. (See Figure 5). $\overline{HF}$ will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 255 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of $\overline{EF}$ occurs t_{REF} after the falling edge of $\overline{R}$ during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

A special case of read occurs when a read operation is initiated while the part is empty. The data latched in by the next write will be accessed t_A ns after the rising edge of $\overline{EF}$. Read is held active, and cannot be deasserted until T_{RPE} after the rising edge of $\overline{EF}$ (see Figure 8).

Half-Full Flag

The Half-Full ($\overline{HF}$) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 256 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 256 words, and Read and Write pulses are applied simultaneously, the $\overline{HF}$ flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$ will always settle to the correct state after the appropriate delay, t_{WHF} or t_{RHF}. This property of the Half-Full Flag is clearly a function of the dynamic relation between $\overline{W}$ and $\overline{R}$. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

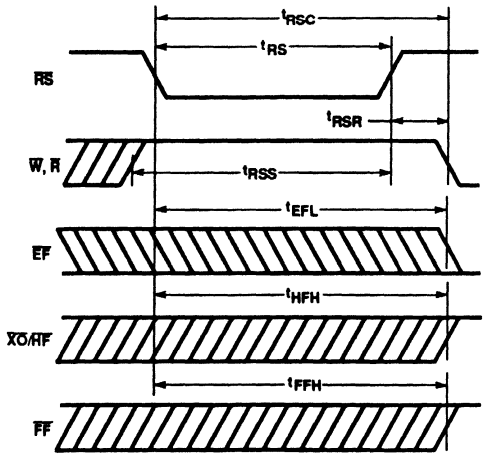


Figure 2. Reset Timing

RESET AND RETRANSMIT TRUTH TABLE Single-Device Configuration/Width-Expansion Mode

Mode	Input			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

Notes: 1. Flags will change to show correct state according to write pointer.
2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 1.

RESET AND FIRST LOAD TRUTH TABLE Depth-Expansion/Compound-Expansion Mode

Mode	Input			Internal Status		Outputs	
	RS	FL/RT	XI	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset–first device	0	0	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	$\overline{X}$ (Note 2)	$\overline{XO}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

Notes: 1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
2. Same as during Reset Cycle.
3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2.

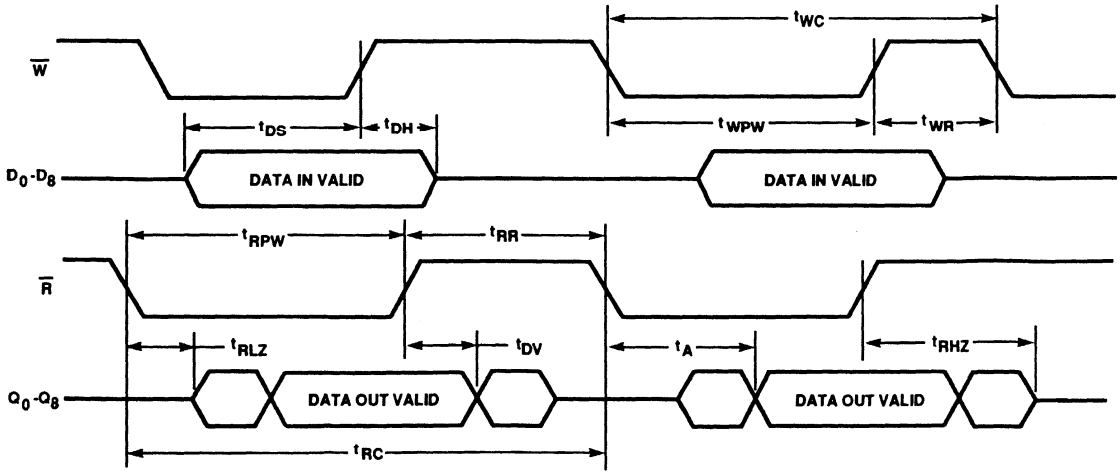


Figure 3. Asynchronous Write and Read Timing

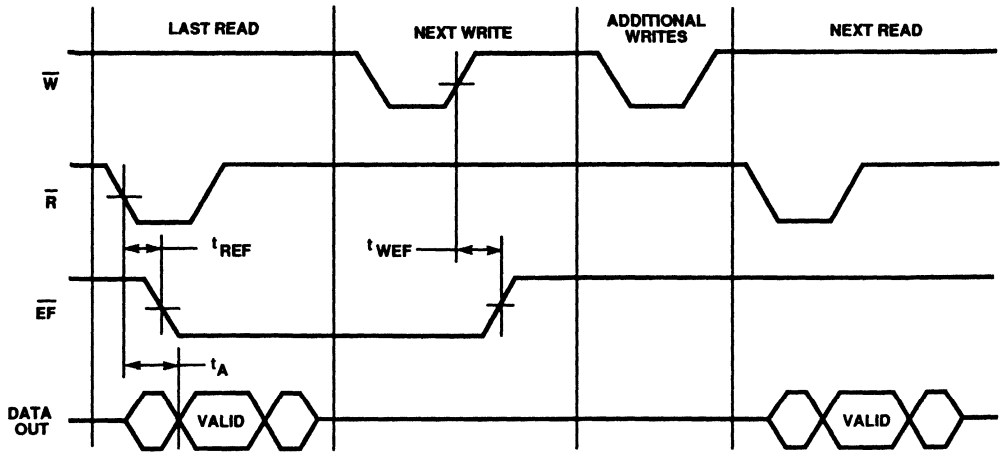
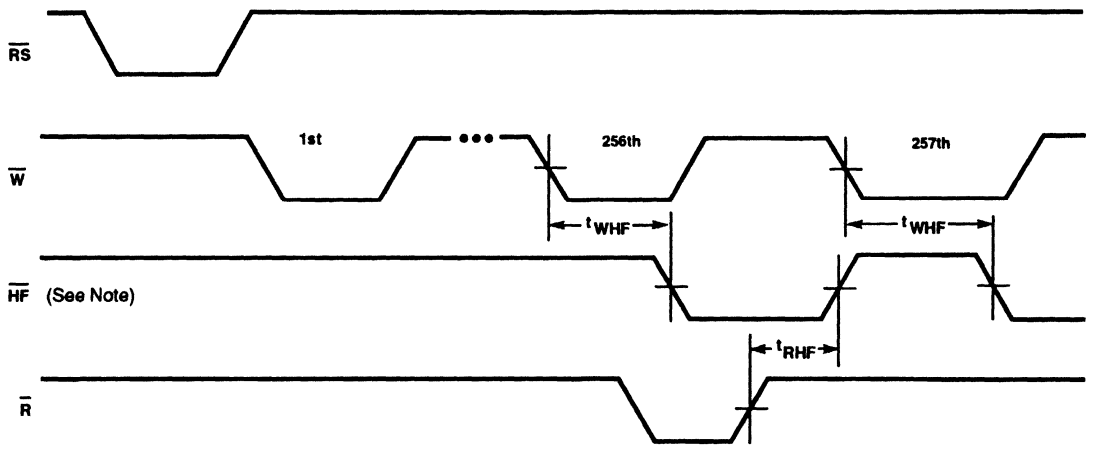


Figure 4. Empty Flag Timing



Note: Depending on the precise phase of $\overline{W}$ and $\overline{R}$, the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when $\overline{W}$ and $\overline{R}$ are operating asynchronously near half full.

Figure 5. Half-Full Flag Timing

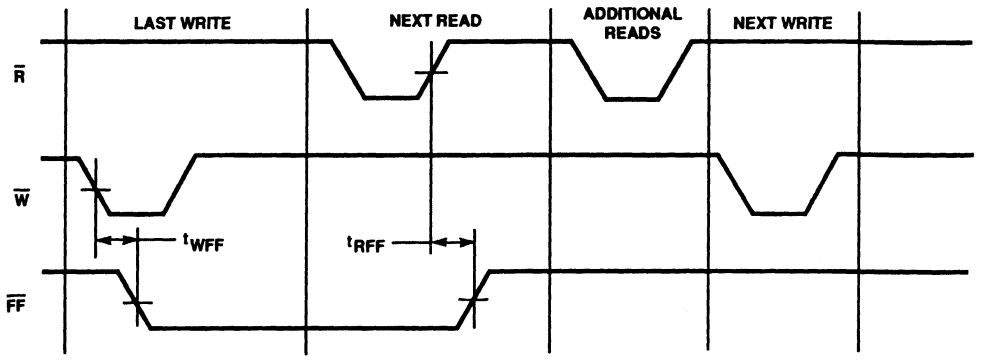


Figure 6. Full Flag Timing

Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 512 or less writes between reset cycles.

The $\overline{FL}/\overline{RT}$ is used as the Retransmit ($\overline{RT}$) input in Single-Device Mode. The retransmit capability is intended for use when there are 512 or less writes between reset cycles. $\overline{RT}$, an active LOW-going pulse of at least t_{RT} in duration, initializes the internal read pointer to address zero and leaves the write pointer unaffected. $\overline{R}$ must both be HIGH during the retransmit cycle. The first read cycle should not start until t_{RTR} after the rising edge of $\overline{RT}$. The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO t_{RTC} after the falling edge of $\overline{RT}$. (See Figure 7 and Table 1).

Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ($\overline{XI}$) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The Am7201 can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1.) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated due to the skew between devices. 2.) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one device's flags are used as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time (t_{WEF}, t_{WHF}, t_{WFF}, t_{REF}, t_{RHF}, and t_{RFF}) for each flag has elapsed.

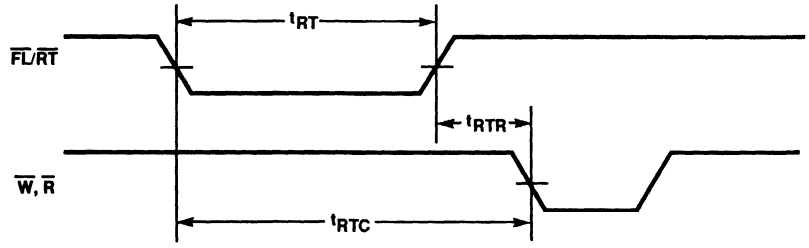
Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ($\overline{XO}$) of one device must be connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device being connected to XI of the first device. The device that is to receive data first has its First Load ($\overline{FL}$) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using $\overline{XO}$ and $\overline{XI}$. A LOW-going pulse on $\overline{XO}$ occurs when the last physical location of an active device, address 511, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the $\overline{FF}$ outputs together. Likewise, a composite Empty Flag is created by OR-ing all the $\overline{EF}$ outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

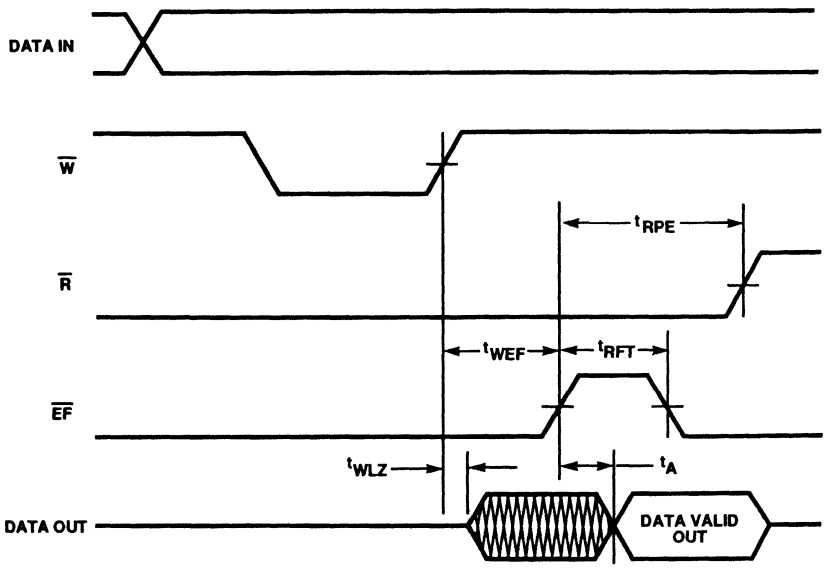
Compound Expansion

FIFOs of greater width and depth than the Am7201 can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)



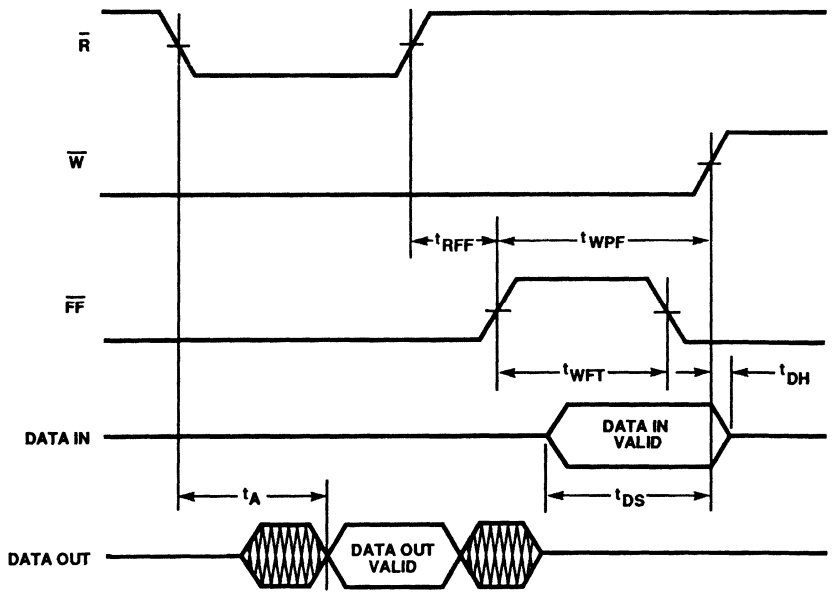
Note: $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at t_{RTC}.

Figure 7. Retransmit Timing



Note: ($t_{RPE} = t_{RPW}$, $t_{RFT} = t_{REF}$)

Figure 8. Read Data Flow-Through Mode



Note: ($t_{WPF} = t_{WPW}$, $t_{WFT} = t_{WFF}$)

Figure 9. Write Data Flow-Through Mode

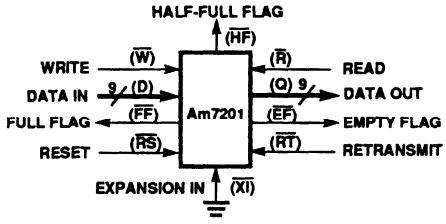


Figure 10. Single FIFO Configuration

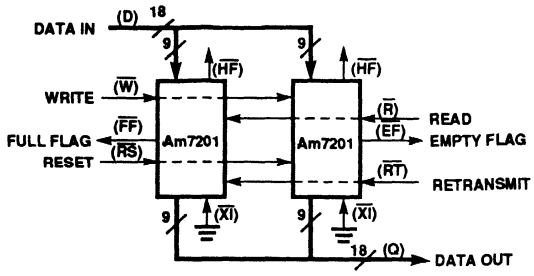


Figure 11. Width-Expansion to Form a 512x18 FIFO

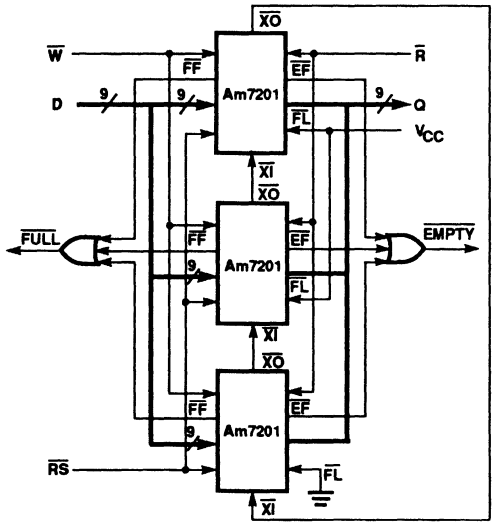


Figure 12. Depth-Expansion to Form a 1536x9 FIFO

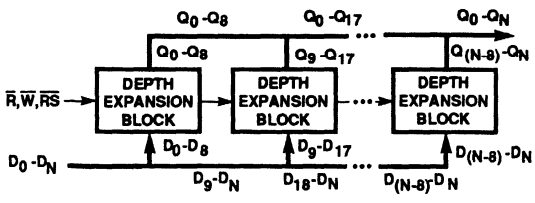


Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques

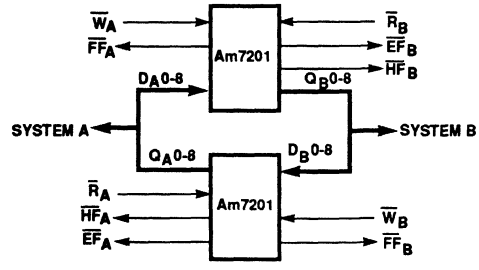


Figure 14. Bidirectional FIFO Mode

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	-0.5V to + 7.0V
Input Voltage	-0.5V to V_{CC} + 0.5V
Ambient Tempature with Power Applied	–55°C to +125°C
Storage Temperature	–55°C to + 150°C
Power Dissipation	1.0 W
DC Output Current	50 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

COMMERCIAL (C) DEVICES

Ambient Temperature (T_A)	0°C to 70°C
Supply Voltage, (V_{CC})	+4.5V to +5.5V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Am7201-25 t_A = 25 ns Min.	Max.	Am7201-35 t_A = 35 ns Min.	Max.	Am7201-50 t_A = 50 ns Min.	Max.	Am7201-65 t_A = 65 ns Min.	Max.	Am7201-80 t_A = 80 ns Min.	Max.	Unit
I_{IL}	Input Leakage Current (any input) (Note 1)	–1	1	–1	1	–1	1	–1	1	–1	1	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	–10	10	–10	10	–10	10	–10	10	–10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	–	0.8	–	0.8	–	0.8	–	0.8	–	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	–	3.5	–	3.5	–	3.5	–	3.5	–	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = –2 mA	2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	V
V_{OL}	Output Logic "0" voltage I_{OL} = 8 mA	–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	–	70	–	60	–	60	–	60	–	60	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (Note 4)	–	20	–	20	–	20	–	20	–	20	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} –0.2 V) (Note 4)	–	5	–	5	–	5	–	5	–	5	mA

Notes:
1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Figures	Am7201-25 Min.	Am7201-25 Max.	Am7201-35 Min.	Am7201-35 Max.	Am7201-50 Min.	Am7201-50 Max.	Am7201-65 Min.	Am7201-65 Max.	Am7201-80 Min.	Am7201-80 Max.	Unit
Write and Flag Timing													
t_{WC}	Write Cycle Time	3	35		45		65		80		100		ns
t_{WPW}	Write Pulse Width	3	25		35		50		65		80		ns
t_{WR}	Write Recovery Time	3	10		10		15		15		20		ns
t_{DS}	Data Setup Time	3,9	15		18		30		30		40		ns
t_{DH}	Data Hold Time	3,9	0		0		5		10		10		ns
t_{WFF}	Write LOW to Full Flag LOW	6,9		25		30		45		60		60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5		35		45		65		80		100	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8		25		30		45		60		60	ns
t_{WLZ}	Write pulse HIGH to data bus at LOW Z (Note 1)	8	5		10		15		15		20		ns
Read and Flag Timing													
t_{RC}	Read Cycle Time	3	35		45		65		80		100		ns
t_{A}	Access Time	3,4,8,9		25		35		50		65		80	ns
t_{RR}	Read Recovery Time	3	10		10		15		15		20		ns
t_{RPW}	Read Pulse Width	3	25		35		50		65		80		ns
t_{RLZ}	Read pulse LOW to data bus at LOW Z (Note 1)	3	5		5		10		10		10		ns
t_{DV}	Data Valid from read pulse HIGH	3	5		5		5		5		5		ns
t_{RHZ}	Read pulse HIGH to data bus at HIGH Z (Note 1)	3		18		20		30		30		30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9		25		30		45		60		60	ns
t_{RHF}	Read HIGH to Half Full-Flag HIGH	5		35		45		65		80		100	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8		25		30		45		60		60	ns
Reset Timing													
t_{RSC}	Reset Cycle Time	2	35		45		65		80		100		ns
t_{RS}	Reset Pulse Width	2	25		35		50		65		80		ns
t_{RSS}	Reset Setup Time	2	25		35		50		65		80		ns
t_{RSR}	Reset Recovery Time	2	10		10		15		15		20		ns
t_{EFL}	Reset to Empty Flag LOW	2		35		45		65		80		100	ns
t_{HFH}	Reset to Half-Full Flag High	2		35		45		65		80		100	ns
t_{FFH}	Reset to Full Flag HIGH	2		35		45		65		80		100	ns
Retransmit Timing													
t_{RTC}	Retransmit Cycle Time	7	35		45		65		80		100		ns
t_{RT}	Retransmit Pulse Width	7	25		35		50		65		80		ns
t_{RTR}	Retransmit Recovery Time	7	10		10		15		15		20		ns

Note: 1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	-0.5V to + 7.0V
Input Voltage	-0.5V to V_{CC} + 0.5V
Ambient Tempature with Power Applied	–55°C to +125°C
Storage Temperature	–65°C to + 155°C
Power Dissipation	1.0 W
DC Output Current	50 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) DEVICES*

Case Temperature (T_C)	-55 to 125°C
Supply Voltage, (V_{CC})	+4.5V to +5.5V

Operating ranges define those limits between which the functionality of the device is guaranteed.

**Military product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.*

DC CHARACTERISTICS over MILITARY operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Am7201-40 t_A = 40 ns Min.	Am7201-40 t_A = 40 ns Max.	Am7201-50 t_A = 50 ns Min.	Am7201-50 t_A = 50 ns Max.	Am7201-65 t_A = 65 ns Min.	Am7201-65 t_A = 65 ns Max.	Am7201-80 t_A = 80 ns Min.	Am7201-80 t_A = 80 ns Max.	Unit
I_{IL}	Input Leakage Current (any input) (Note 1)	–10	10	–10	10	–10	10	–10	10	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	–10	10	–10	10	–10	10	–10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.2	–	2.2	–	2.2	–	2.2	–	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	–	0.8	–	0.8	–	0.8	–	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	–	3.5	–	3.5	–	3.5	–	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	–	1.5	–	1.5	–	1.5	–	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = -2 mA	2.4	–	2.4	–	2.4	–	2.4	–	V
V_{OL}	Output Logic "0" voltage I_{OL} = 8 mA	–	0.4	–	0.4	–	0.4	–	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	–	100	–	90	–	90	–	90	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}) (Note 4)	–	25	–	25	–	25	–	25	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} -0.2 V) (Note 4)	–	5	–	5	–	5	–	5	mA

Notes:
1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

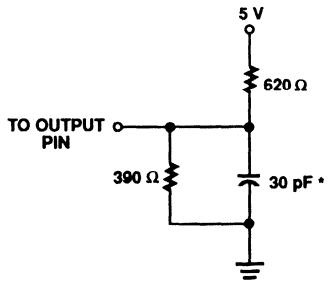
SWITCHING CHARACTERISTICS over MILITARY operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Figures	Am7201-40 Min.	Am7201-40 Max.	Am7201-50 Min.	Am7201-50 Max.	Am7201-65 Min.	Am7201-65 Max.	Am7201-80 Min.	Am7201-80 Max.	Unit
Write and Flag Timing											
t_{WC}	Write Cycle Time	3	50		65		80		100		ns
t_{WPW}	Write Pulse Width	3	40		50		65		80		ns
t_{WR}	Write Recovery Time	3	10		15		15		20		ns
t_{DS}	Data Setup Time	3,9	20		30		30		40		ns
t_{DH}	Data Hold Time	3,9	0		5		10		10		ns
t_{WFF}	Write LOW to Full Flag LOW	6,9		35		45		60		60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5		50		65		80		100	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8		35		45		60		60	ns
t_{WLZ}	Write pulse HIGH to data bus at LOW Z (Note 1)	8	10		15		15		15		ns
Read and Flag Timing											
t_{RC}	Read Cycle Time	3	50		65		80		100		ns
t_A	Access Time	3,4,8,9		40		50		65		80	ns
t_{RR}	Read Recovery Time	3	10		15		15		20		ns
t_{RPW}	Read Pulse Width	3	40		50		65		80		ns
t_{RLZ}	Read pulse LOW to data bus at LOW Z (Note 1)	3	5		10		10		10		ns
t_{DV}	Data Valid from read pulse HIGH	3	5		5		5		5		ns
t_{RHZ}	Read pulse HIGH to data bus at HIGH Z (Note 1)	3		25		30		30		30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9		35		45		60		60	ns
t_{RHF}	Read HIGH to Half Full-Flag HIGH	5		50		65		80		100	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8		30		45		60		60	ns
Reset Timing											
t_{RSC}	Reset Cycle Time	2	50		65		80		100		ns
t_{RS}	Reset Pulse Width	2	40		50		65		80		ns
t_{RSS}	Reset Setup Time	2	40		50		65		80		ns
t_{RSR}	Reset Recovery Time	2	10		15		15		20		ns
t_{EFL}	Reset to Empty Flag LOW	2		50		65		80		100	ns
t_{HFH}	Reset to Half-Full Flag High	2		50		65		80		100	ns
t_{FFH}	Reset to Full Flag HIGH	2		50		65		80		100	ns
Retransmit Timing											
t_{RTC}	Retransmit Cycle Time	7	50		65		80		100		ns
t_{RT}	Retransmit Pulse Width	7	40		50		65		80		ns
t_{RTR}	Retransmit Recovery Time	7	10		15		15		20		ns

Notes: These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See Figure 15



* Includes jig and scope capacitances.

Figure 15. A.C. Test Load

CAPACITANCE (V_{CC} = 5.0V, T_A = + 25°C, f = 1.0 MHz)

Symbol	Parameter (Note 1)	Conditions	Typ.	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V	5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	7	pF

Note: 1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

Am7202A

High Density First-In First-Out (FIFO) 1024x9-Bit CMOS Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 1024x9 organization
- Cycle times of 25/35/45/65 nanoseconds for Standard products
- Cycle times of 40/65 nanoseconds for APL products
- Asynchronous and simultaneous writes and reads
- Low power consumption
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for $\overline{XI}$ - CMOS threshold
- Functional and pin compatible with industry standard devices

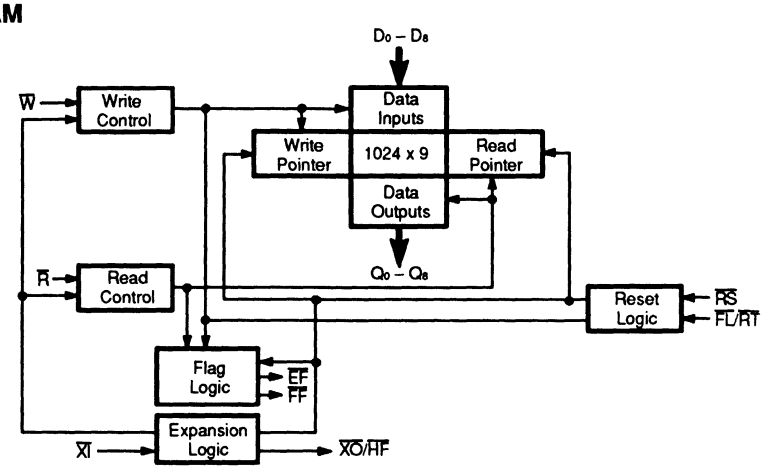
GENERAL DESCRIPTION

The Am7202A is a RAM-based CMOS FIFO that is 1024 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can input and output data asynchronously and simultaneously at data rates from 0 to 40 MHz for Standard Products and 0 to 25 MHz for APL products. Status flags are provided to signify empty, full and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7202A are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7202A useful in communication, image processing, mass storage, DSP, and printing systems.

BLOCK DIAGRAM



14430-001A

Figure 1.

PRODUCT SELECTOR GUIDE

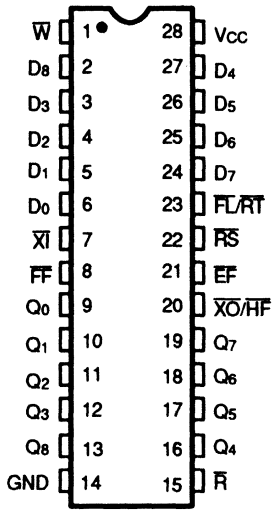
Part Number	Am7202A-15	Am7202A-25	Am7202A-35	Am7202A-50	Am7202A-30	Am7202A-50
Access Time	15 ns	25 ns	35 ns	50 ns	30 ns	50 ns
Maximum Power Supply Current	90 mA	70 mA	60 mA	60 mA	100 mA	90 mA
Operating Frequency	40 MHz	28.5 MHz	22.2 MHz	15.3 MHz	25 MHz	15.3 MHz
Operating Range	Com'l	Com'l	Com'l	Com'l	Mil	Mil

Publication# 15491 Rev. A Amendment/0
Issue Date: March 1991

CONNECTION DIAGRAMS

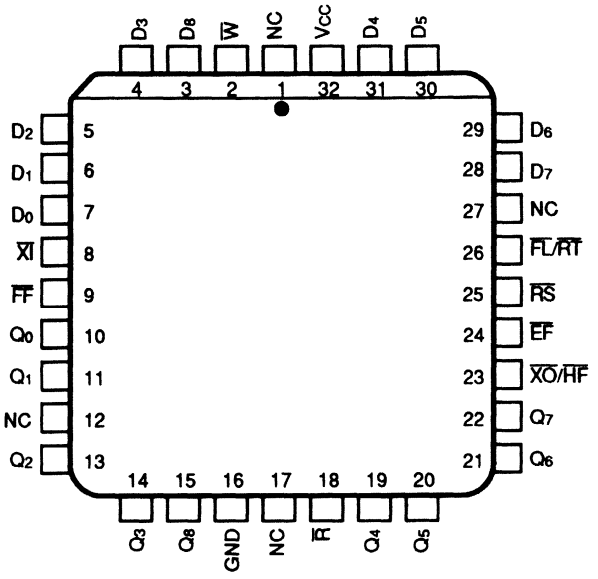
Top View

DIPs*



14430-002A

PLCC/LCC

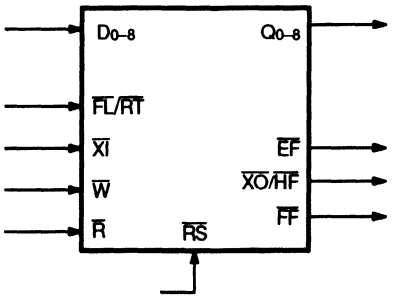


14430-003A

Note:
Pin 1 is marked for orientation for plastic packages.

*Pinout identical for both plastic and ceramic DIPs.

LOGIC SYMBOL

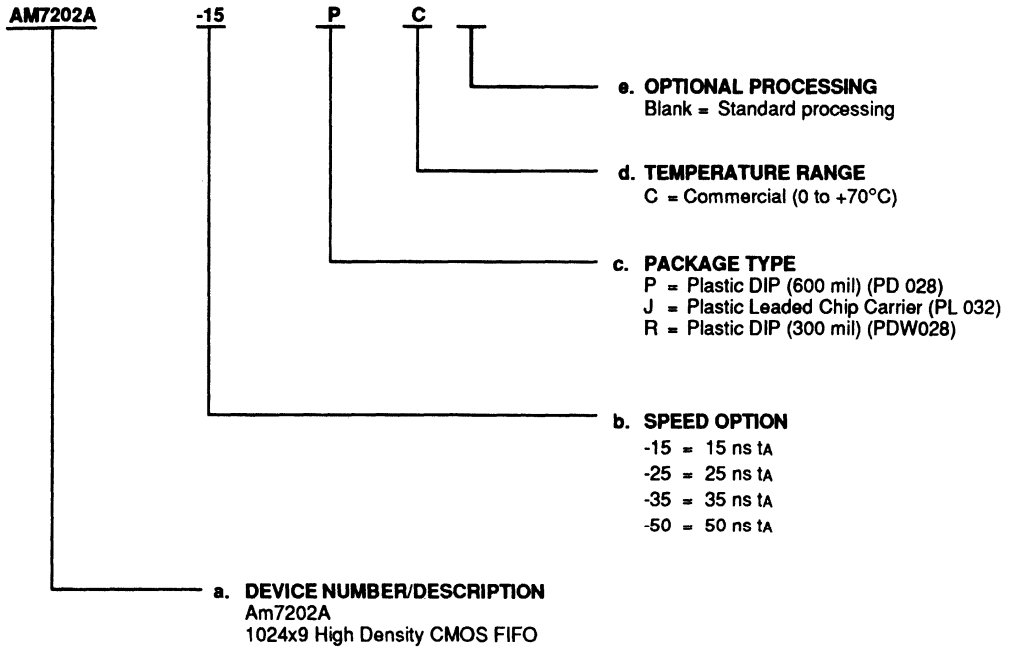


14430-004A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7202A-15	RC, JC
AM7202A-25	PC, RC, JC
AM7202A-35	
AM7202A-50	

Valid Combinations

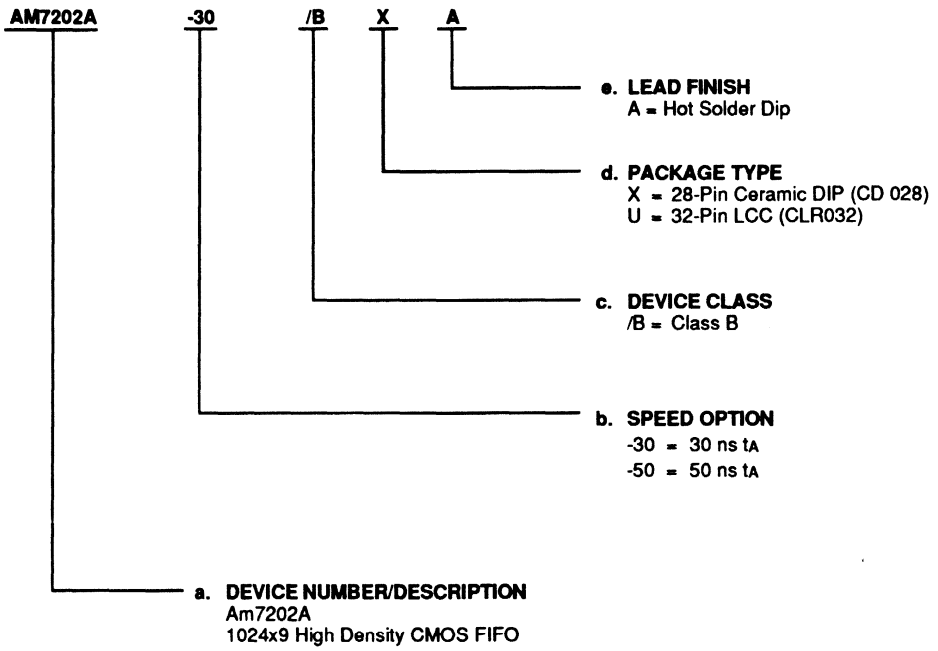
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM7202A-30	/BXA, /BUA
AM7202A-50	

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

D_{0-8}

Data In (Inputs (9))

These nine pins are the data inputs to the FIFO.

$\overline{EF}$

Empty Flag (Output; Active LOW)

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO contains data to be read. The $\overline{EF}$ goes LOW when the read pointer is equal to the write pointer, indicating that the device is empty. $\overline{EF}$ LOW inhibits further Read operations.

The $\overline{EF}$ goes HIGH after the rising edge of Write ($\overline{W}$) during the first write cycle for an empty FIFO (See Figure 4). The $\overline{EF}$ goes LOW after the falling edge of Read ($\overline{R}$) during the read cycle which creates the empty condition.

During a Reset cycle, the $\overline{EF}$ is driven LOW (active).

$\overline{FF}$

Full Flag (Output; Active LOW)

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The $\overline{FF}$ goes LOW when the write pointer is one location less than the read pointer, indicating that the device is full. $\overline{FF}$ LOW inhibits further Write operations.

The $\overline{FF}$ goes HIGH after the rising edge of Read ($\overline{R}$) during the first read cycle following a full condition (See Figure 6). The $\overline{FF}$ goes LOW after the falling edge of Write ($\overline{W}$) during the write cycle which creates the full condition.

During a Reset cycle, the $\overline{FF}$ is driven HIGH (inactive).

$\overline{FL}/\overline{RT}$

First Load/Retransmit (Input; Active LOW)

This is a dual purpose input, dependent upon whether the FIFO is in Single Device Mode or Depth-Expansion Mode.

This pin acts as a FIRST LOAD ($\overline{FL}$) pin when in the Depth-Expansion Mode. The device receiving data first will have the $\overline{FL}$ input tied LOW, while the remaining devices will have the $\overline{FL}$ pin tied HIGH. The states of the $\overline{FL}$ and Expansion In ($\overline{XI}$) pins are used to determine the FIFO's mode of operation, as shown in Tables 1 and 2.

This pin is used as the Retransmit ($\overline{RT}$) input during Single Device Mode. The device can be instructed to retransmit the previously written data when $\overline{RT}$ is pulsed LOW.

GND

Power Supply, Ground

This pin is the 0 V power supply for the FIFO.

NC

No Connect

These pins are not connected.

Q_{0-8}

Data Out (Outputs (9), Three State)

These nine pins are the data outputs for the FIFO. These pins are in a high impedance state whenever Read ($\overline{R}$) is HIGH.

$\overline{R}$

Read (Input; Active LOW)

The falling edge of Read ($\overline{R}$) initiates a read cycle, except when the device is empty, as indicated by the Empty Flag ($\overline{EF}$) being LOW. Valid data appears on the outputs (Q_{0-8}) after the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the Data Outputs (Q_{0-8}) will return to a high impedance condition.

$\overline{RS}$

Reset (Input; Active LOW)

The falling edge of Reset ($\overline{RS}$) is used to reset the FIFO. During Reset, both the read and write pointers are set to the first location in the FIFO. Since the reset cycle initializes the FIFO to an empty condition, the Empty Flag ($\overline{EF}$) is driven LOW (active), and both the Half-Full Flag ($\overline{HF}$) and Full Flag ($\overline{FF}$) are driven HIGH (inactive).

V_{CC}

Power Supply

This pin is the +5 V power supply for the FIFO.

$\overline{W}$

Write (Input; Active LOW)

The falling edge of Write ($\overline{W}$) initiates a write cycle, except when the device is full, as indicated by the Full Flag ($\overline{FF}$) being LOW. Data is latched into the FIFO on the rising edge of $\overline{W}$.

$\overline{XI}$

Expansion In (Input; Active LOW)

Expansion In ($\overline{XI}$) is grounded to indicate operation in the Single Device or Width-Expansion Modes. In Depth Expansion Mode, the $\overline{XI}$ pin is connected to the Expansion Out ($\overline{XO}$) pin of the previous device, except for the $\overline{XI}$ pin of the first device which is connected to the $\overline{XO}$ pin of the last FIFO.

This pin operates at CMOS logic levels, thus providing noise immunity between cascaded devices.

$\overline{XO}/\overline{HF}$

Expansion Out/Half-Full Flag (Output; Active LOW)

This is a dual purpose output, dependent upon whether the device is in Single Device Mode or Depth Expansion Mode.

This pin operates as an Expansion Out ($\overline{XO}$) signal during Depth Expansion Mode. In this mode, the $\overline{XO}$ pin is connected to the Expansion Input ($\overline{XI}$) pin of the following device, except for the $\overline{XO}$ pin of the last device which is connected to the $\overline{XI}$ pin of the first device.

When in Single Device Mode (Expansion In ($\overline{XI}$) pin grounded) this output operates as a Half-Full Flag ($\overline{HF}$). After half the FIFO has been filled, the $\overline{HF}$ will be set LOW at the falling edge of the next Write ($\overline{W}$) operation. The $\overline{HF}$ will remain LOW until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the FIFO. The $\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$ during the read operation which eliminates the half-full condition (See Figure 5).

During a Reset cycle, the $\overline{HF}$ is driven HIGH (inactive).

This pin operates at CMOS logic levels, thus providing noise immunity between cascaded devices.

FUNCTIONAL DESCRIPTION

The Am7202A CMOS FIFO is designed around a 1024x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 1023. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the Am7202A. The write, read, data-in and data-out lines of the Am7202A are connected in parallel, and the Expansion-Out ($\overline{XO}$) and the Expansion-In ($\overline{XI}$) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between $\overline{XO}$ and $\overline{XI}$.

Operational Description

Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of $\overline{XI}$ and $\overline{FL}$ are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ($\overline{R}$) and Write ($\overline{W}$) signals must be HIGH t_{RSS} prior to and t_{RSR} after the rising edge of Reset ($\overline{RS}$). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ($\overline{EF}$) being LOW, active, and both the Half-Full ($\overline{HF}$) and Full Flag ($\overline{FF}$) being HIGH, inactive.

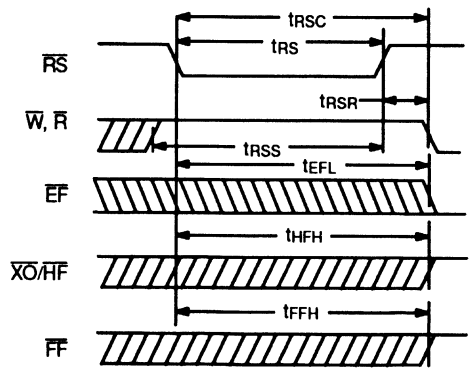


Figure 2. Reset Timing 14430-005A

Writing Data To The FIFO

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The falling edge of Write ($\overline{W}$) initiates a write cycle. (See Figure 3.) Data appearing at inputs D_0–D_8 t_{DS} prior to and t_{DH} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The LOW-to-HIGH transition of the Empty Flag ($\overline{EF}$) occurs t_{WEF} after the rising edge of $\overline{W}$ during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag ($\overline{HF}$) will go LOW t_{WHF} after the falling edge of $\overline{W}$ during the write operation which creates the half-full condition. (See Figure 5.) $\overline{HF}$ will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 513 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ($\overline{FF}$) goes LOW t_{WFF} after the falling edge of $\overline{W}$ during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 1024 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

A special case of write occurs when a write operation is initiated while the part is full. The next read will cause $\overline{FF}$ to go inactive, and data can then be latched into the FIFO T_{WPF} after the rising edge of $\overline{FF}$ (see Figure 9).

Reading Data From The FIFO

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO is ready to output data. The falling edge of Read ($\overline{R}$) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q_0–Q_8 t_A after the falling edge of $\overline{R}$, and remains until t_{DV} after the rising edge of $\overline{R}$. Q_0–Q_8 return to a high-impedance state when $\overline{R}$ is inactive, when the FIFO is empty, or when the FIFO is in Depth Expansion Mode but is not active.

The Full Flag ($\overline{FF}$) will go HIGH t_{RFF} after the rising edge of $\overline{R}$ during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag ($\overline{HF}$) will go HIGH t_{RHF} after the rising edge of $\overline{R}$ during the read operation, which eliminates the half-full condition. (See Figure 5). $\overline{HF}$ will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 512 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of $\overline{EF}$ occurs t_{REF} after the falling edge of $\overline{R}$ during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

A special case of read occurs when a read operation is initiated while the part is empty. The data latched in by the next write will be accessed t_A ns after the rising edge of $\overline{EF}$. Read is held active, and cannot be deasserted until T_{RPE} after the rising edge of $\overline{EF}$ (see Figure 8).

Table 1. Reset and Retransmit Truth Table
(Single-Device Configuration/Width-Expansion Mode)

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

Notes:

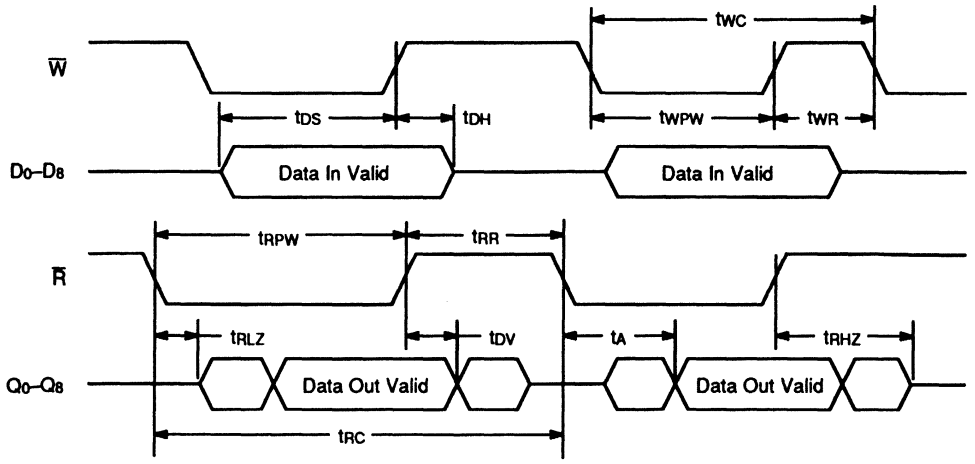
1. Flags will change to show correct state according to write pointer.
2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2. Reset and First Load Truth Table
(Depth-Expansion/Compound-Expansion Mode)

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-first device	0	0	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	$\overline{XO}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

Notes:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
2. Same as during Reset Cycle.
3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.



14430-006A

Figure 3. Asynchronous Write and Read Timing

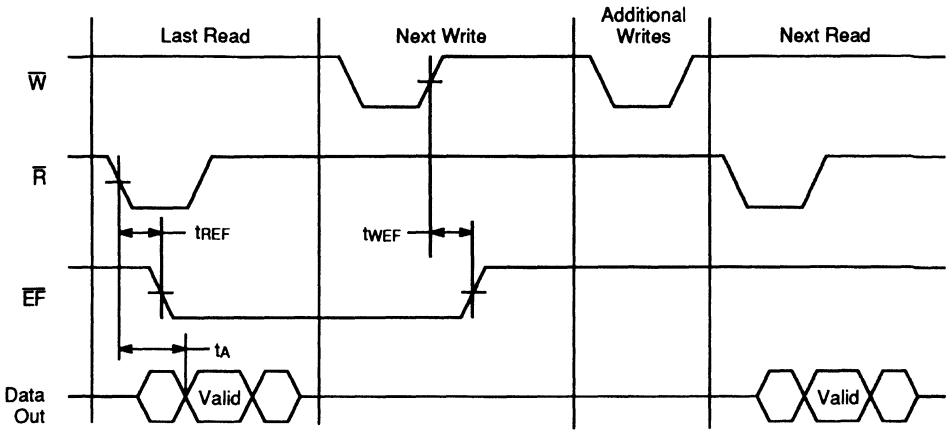


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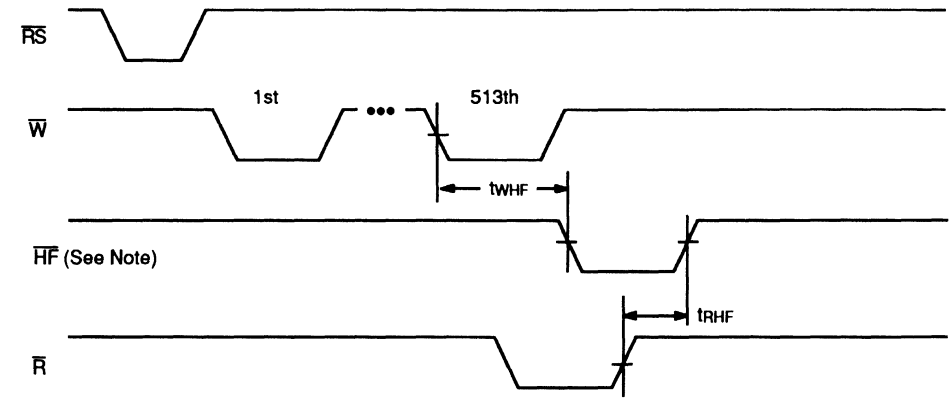
Figure 4. Empty Flag Timing

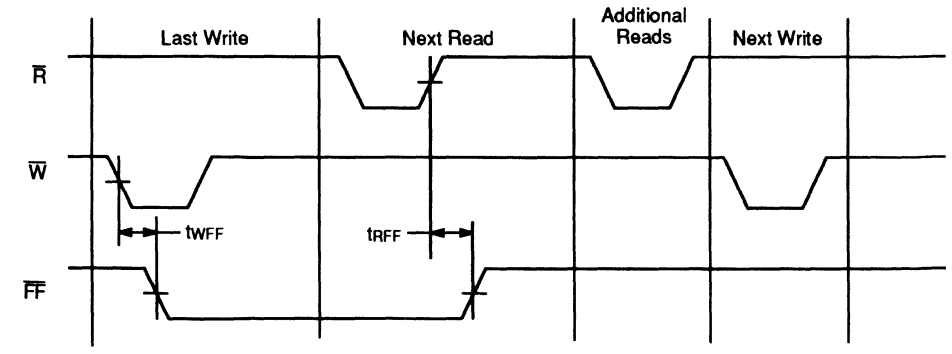


Note:

Depending on the precise phase of $\overline{W}$ and $\overline{R}$, the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when $\overline{W}$ and $\overline{R}$ are operating asynchronously near half full.

14430-008A

Figure 5. Half-Full Flag Timing



14430-009A

Figure 6. Full Flag Timing

Half-Full Flag

The Half-Full ($\overline{HF}$) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 513 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 513 words, and Read and Write pulses are applied simultaneously, the $\overline{HF}$ flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$ will always settle to the correct state after the appropriate delay, t_{WHF} or t_{RHF}. This property of the Half-Full Flag is clearly a function of the dynamic relation between $\overline{W}$ and $\overline{R}$. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 1024 or less writes between reset cycles.

The $\overline{FL}/\overline{RT}$ is used as the Retransmit ($\overline{RT}$) input in Single-Device Mode. The retransmit capability is intended for use when there are 1024 or less writes between reset cycles. $\overline{RT}$, an active LOW-going pulse of at least t_{RT} in duration, initializes the internal read pointer to address zero and leaves the write pointer unaffected. $\overline{R}$ must be HIGH during the retransmit cycle. The first read cycle should not start until t_{RTR} after the rising edge of $\overline{RT}$. The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO t_{RTC} after the falling edge of $\overline{RT}$. (See Figure 7 and Table 1).

Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ($\overline{XI}$) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The Am7202A can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated due to the skew between devices. 2) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one device's flags are used as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time (t_{WEF}, t_{WHF}, t_{WFF}, t_{REF}, t_{RHF}, and t_{RFF}) for each flag has elapsed.

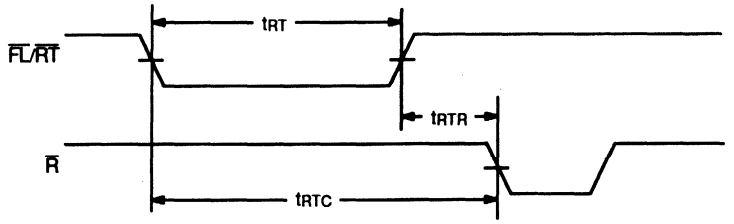
Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ($\overline{XO}$) of one device must be connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device being connected to $\overline{XI}$ of the first device. The device that is to receive data first has its First Load ($\overline{FL}$) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using $\overline{XO}$ and $\overline{XI}$. A LOW-going pulse on $\overline{XO}$ occurs when the last physical location of an active device, address 1024, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the $\overline{FF}$ outputs together. Likewise, a composite Empty Flag is created by OR-ing all the $\overline{EF}$ outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

Compound Expansion

FIFOs of greater width and depth than the Am7202A can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)



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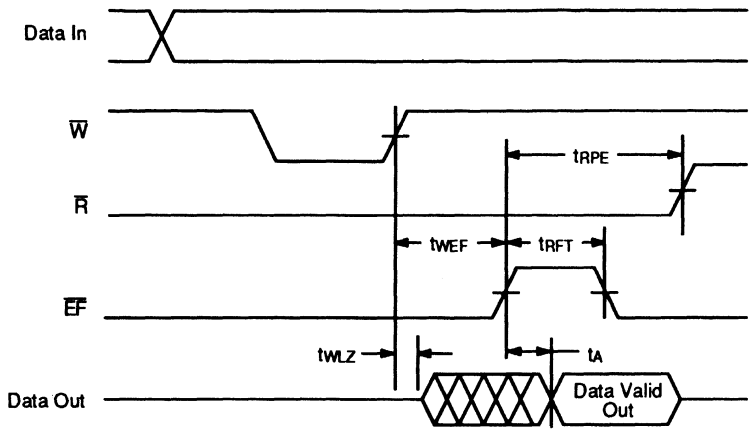
Note:

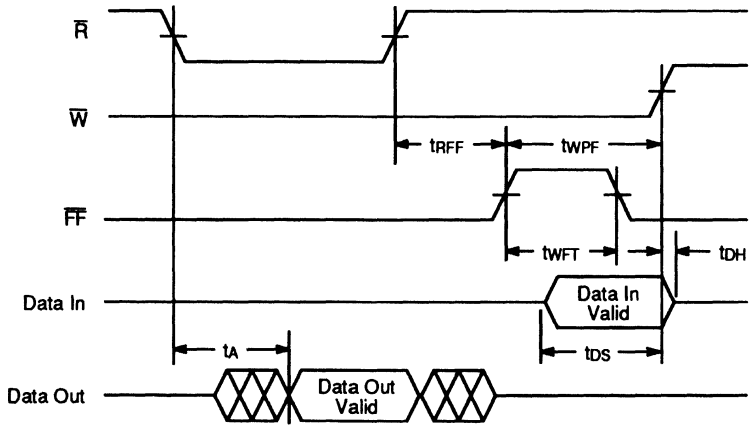
$\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at t_{RTC}.

Figure 7. Retransmit Timing



Note: ($t_{RPE} = t_{RPW}$, $t_{RFT} = t_{REF}$)

Figure 8. Read Data Flow-Through Mode



Note: ($t_{WPF} = t_{WPW}$, $t_{WFT} = t_{WFF}$)

Figure 9. Write Data Flow-Through Mode

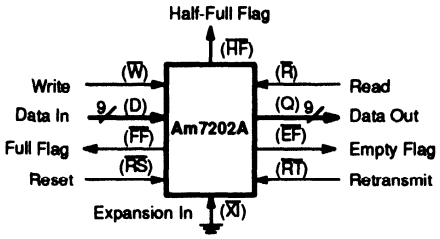


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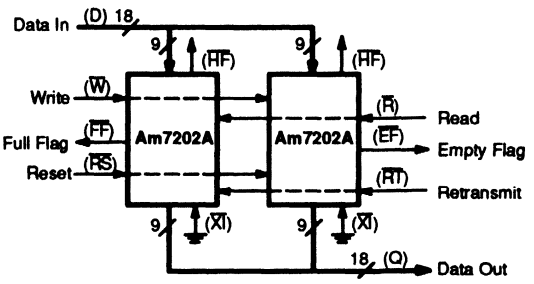
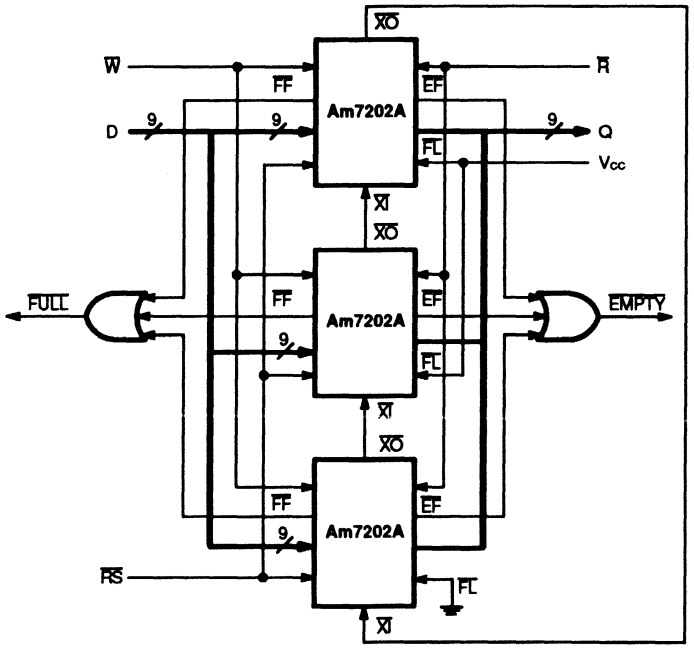
Figure 10. Single FIFO Configuration



14430-014A

Figure 11. Width-Expansion to Form a 1,024x18 FIFO



14430-015A

Figure 12. Depth-Expansion to Form 3,072x9 FIFO

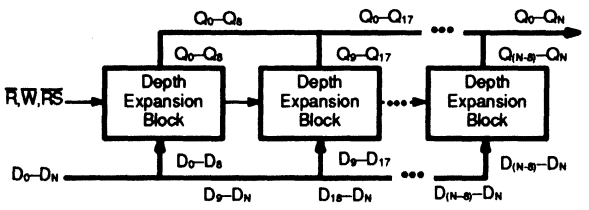


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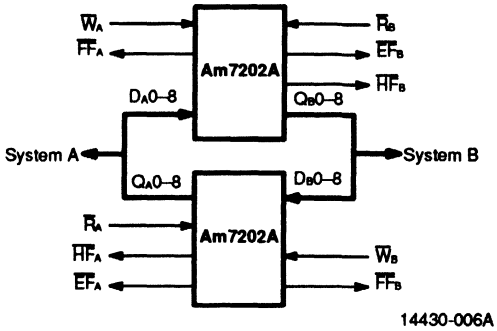
Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques



14430-006A

Figure 14. Bidirectional FIFO Configuration

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5V to +7.0 V
Input Voltage	−0.5V to V_{CC} +0.5 V
Ambient Temperature with Power Applied	−55°C to +125°C
Storage Temperature	−55°C to +150°C
Power Dissipation	1.0 W
DC Output Current	50 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0°C to 70°C
Supply Voltage, (V_{CC})	+4.5V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Am7202A-15 t_A = 15 ns		Am7202A-25 t_A = 25 ns		Am7202A-35 t_A = 35 ns		Am7202A-50 t_A = 50 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{IL}	Input Leakage Current (any input) (Note 1)	−1	1	−1	1	−1	1	−1	1	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	−10	10	−10	10	−10	10	−10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	—	1.5	—	1.5	—	1.5	—	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = −2 mA	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8 mA	—	0.4	—	0.4	—	0.4	—	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	—	90	—	70	—	60	—	60	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}) (Note 4)	—	15	—	15	—	15	—	15	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} −0.2 V) (Note 4)	—	2	—	2	—	2	—	2	mA

Notes:

1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Figures	Am7202A-15		Am7202A-25		Am7202A-35		Am7202A-50		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write and Flag Timing											
t_{WC}	Write Cycle Time	3	25	—	35	—	45	—	65	—	ns
t_{WPW}	Write Pulse Width	3	15	—	25	—	35	—	50	—	ns
t_{WR}	Write Recovery Time	3	10	—	10	—	10	—	15	—	ns
t_{DS}	Data Setup Time	3,9	12	—	15	—	18	—	30	—	ns
t_{DH}	Data Hold Time	3,9	0	—	0	—	0	—	5	—	ns
t_{WFF}	Write LOW to Full Flag LOW	6,9	—	22	—	25	—	30	—	45	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5	—	30	—	35	—	45	—	65	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8	—	22	—	25	—	30	—	45	ns
t_{WLZ}	Write Pulse HIGH to Data Bus at LOW Z (Note 1)	8	5	—	5	—	10	—	15	—	ns
Read and Flag Timing											
t_{RC}	Read Cycle Time	3	25	—	35	—	45	—	65	—	ns
t_A	Access Time	3,4,8,9	—	15	—	25	—	35	—	50	ns
t_{RR}	Read Recovery Time	3	10	—	10	—	10	—	15	—	ns
t_{RPW}	Read Pulse Width	3	15	—	25	—	35	—	50	—	ns
t_{RLZ}	Read Pulse LOW to Data Bus at LOW Z (Note 1)	3	5	—	5	—	5	—	10	—	ns
t_{DV}	Data Valid from Read Pulse HIGH	3	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse HIGH to Data Bus at HIGH Z (Note 1)	3	—	15	—	18	—	20	—	30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9	—	22	—	25	—	30	—	45	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	5	—	30	—	35	—	45	—	65	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8	—	22	—	25	—	30	—	45	ns
Reset Timing											
t_{RSC}	Reset Cycle Time	2	25	—	35	—	45	—	65	—	ns
t_{RS}	Reset Pulse Width	2	15	—	25	—	35	—	50	—	ns
t_{RSS}	Reset Setup Time	2	15	—	25	—	35	—	50	—	ns
t_{RSR}	Reset Recovery Time	2	10	—	10	—	10	—	15	—	ns
t_{EFL}	Reset to Empty Flag LOW	2	—	25	—	35	—	45	—	65	ns
t_{HFH}	Reset to Half-Full Flag High	2	—	25	—	35	—	45	—	65	ns
t_{FFH}	Reset to Full Flag HIGH	2	—	25	—	35	—	45	—	65	ns
Retransmit Timing											
t_{RTC}	Retransmit Cycle Time	7	30	—	35	—	45	—	65	—	ns
t_{RT}	Retransmit Pulse Width	7	20	—	25	—	35	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	7	10	—	10	—	10	—	15	—	ns

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5V to +7.0 V
Input Voltage	−0.5V to V_{CC} +0.5 V
Ambient Temperature with Power Applied	−55 to +125°C
Storage Temperature	−65 to +155°C
Power Dissipation	1.0 W
DC Output Current	50 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices*

Case Temperature (Tc)	−55 to 125°C
Supply Voltage, (V_{CC})	+4.5V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

**Military product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.*

DC CHARACTERISTICS over MILITARY operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Am7202A-30 t_A = 30 ns		Am7202A-50 t_A = 50 ns		Unit
		Min.	Max.	Min.	Max.	
I_{IL}	Input Leakage Current (any input) (Note 1)	−10	10	−10	10	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	−10	10	−10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.2	—	2.2	—	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	—	0.8	—	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	—	3.5	—	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	—	1.5	—	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = −2 mA	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8 mA	—	0.4	—	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	—	100	—	90	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}) (Note 4)	—	15	—	15	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} −0.2 V) (Note 4)	—	4	—	4	mA

Notes:

1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

SWITCHING CHARACTERISTICS over MILITARY operating range unless otherwise specified.

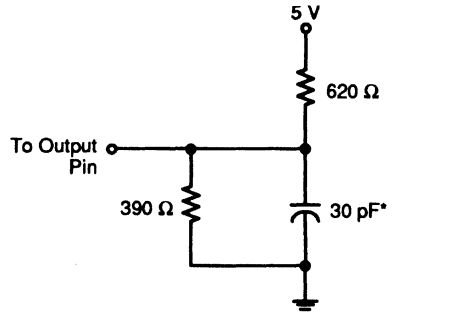
Parameter Symbol	Parameter Description	Figures	Am7202A-30		Am7202A-50		Unit
			Min.	Max.	Min.	Max.	
Write and Flag Timing							
t_{WC}	Write Cycle Time	3	40	—	65	—	ns
t_{WPW}	Write Pulse Width	3	30	—	50	—	ns
t_{WR}	Write Recovery Time	3	10	—	15	—	ns
t_{DS}	Data Setup Time	3,9	18	—	30	—	ns
t_{DH}	Data Hold Time	3,9	0	—	5	—	ns
t_{WFF}	Write LOW to Full Flag LOW	6,9	—	30	—	45	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5	—	40	—	65	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8	—	30	—	45	ns
t_{WLZ}	Write Pulse HIGH to Data Bus at LOW Z (Note 1)	8	5	—	15	—	ns
Read and Flag Timing							
t_{RC}	Read Cycle Time	3	40	—	65	—	ns
t_A	Access Time	3,4,8,9	—	30	—	50	ns
t_{RR}	Read Recovery Time	3	10	—	15	—	ns
t_{RPW}	Read Pulse Width	3	30	—	50	—	ns
t_{RLZ}	Read Pulse LOW to Data Bus at LOW Z (Note 1)	3	5	—	10	—	ns
t_{DV}	Data Valid from Read Pulse HIGH	3	5	—	5	—	ns
t_{RHZ}	Read Pulse HIGH to Data Bus at HIGH Z (Note 1)	3	—	20	—	30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9	—	30	—	45	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	5	—	40	—	65	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8	—	30	—	45	ns
Reset Timing							
t_{RSC}	Reset Cycle Time	2	40	—	65	—	ns
t_{RS}	Reset Pulse Width	2	30	—	50	—	ns
t_{RSS}	Reset Setup Time	2	30	—	50	—	ns
t_{RSR}	Reset Recovery Time	2	10	—	15	—	ns
t_{EFL}	Reset to Empty Flag LOW	2	—	40	—	65	ns
t_{HFH}	Reset to Half-Full Flag High	2	—	40	—	65	ns
t_{FFH}	Reset to Full Flag HIGH	2	—	40	—	65	ns
Retransmit Timing							
t_{RTC}	Retransmit Cycle Time	7	40	—	65	—	ns
t_{RT}	Retransmit Pulse Width	7	30	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	7	10	—	15	—	ns

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See Figure 15



* Includes jig and scope capacitances.

Figure 15. AC Test Load

CAPACITANCE (V_{CC} = 5.0 V, T_A = +25°C, f = 1.0 MHz)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V	5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	7	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

Am7203A

High Density First-In First-Out (FIFO) 2048x9-Bit CMOS Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 2048x9 organization
- Cycle times of 25/35/45/65 nanoseconds for Standard products
- Cycle times of 40/65 nanoseconds for APL products
- Asynchronous and simultaneous writes and reads
- Low power consumption
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for $\overline{XI}$ - CMOS threshold
- Functional and pin compatible with industry standard devices

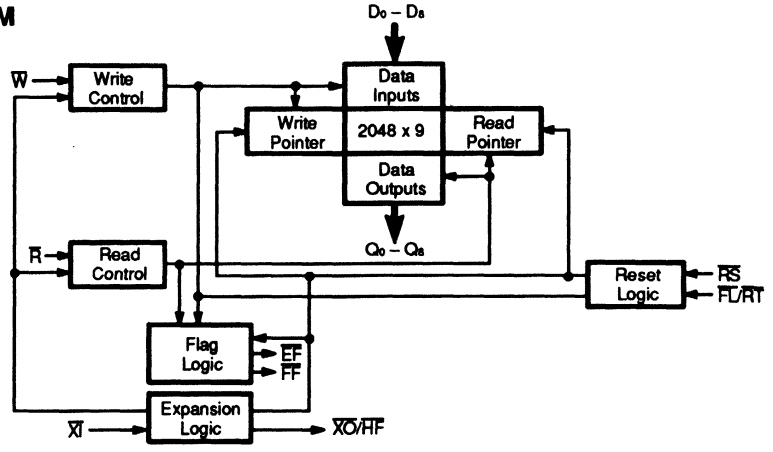
GENERAL DESCRIPTION

The Am7203A is a RAM-based CMOS FIFO that is 2048 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can input and output data asynchronously and simultaneously at data rates from 0 to 40 MHz for Standard Products and 0 to 25 MHz for APL products. Status flags are provided to signify empty, full and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7203A are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7203A useful in communication, image processing, mass storage, DSP, and printing systems.

BLOCK DIAGRAM



14430-001A

Figure 1.

PRODUCT SELECTOR GUIDE

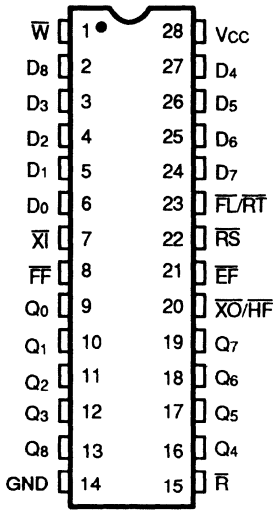
Part Number	Am7203A-15	Am7203A-25	Am7203A-35	Am7203A-50	Am7203A-30	Am7203A-50
Access Time	15 ns	25 ns	35 ns	50 ns	30 ns	50 ns
Maximum Power Supply Current	90 mA	70 mA	60 mA	60 mA	100 mA	90 mA
Operating Frequency	40 MHz	28.5 MHz	22.2 MHz	15.3 MHz	25 MHz	15.3 MHz
Operating Range	Com'l	Com'l	Com'l	Com'l	Mil	Mil

Publication# 15492 Rev. A Amendment/0
Issue Date: March 1991

CONNECTION DIAGRAMS

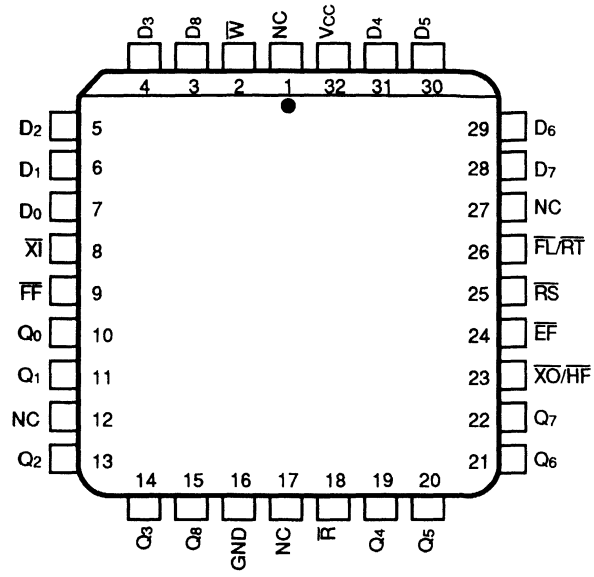
Top View

DIPs*



14430-002A

PLCC/LCC



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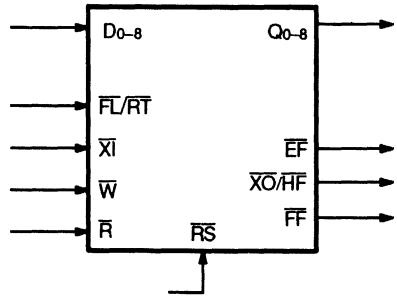
Note:
Pin 1 is marked for orientation for plastic packages.

*Pinout identical for both plastic and ceramic DIPs.

LOGIC SYMBOL

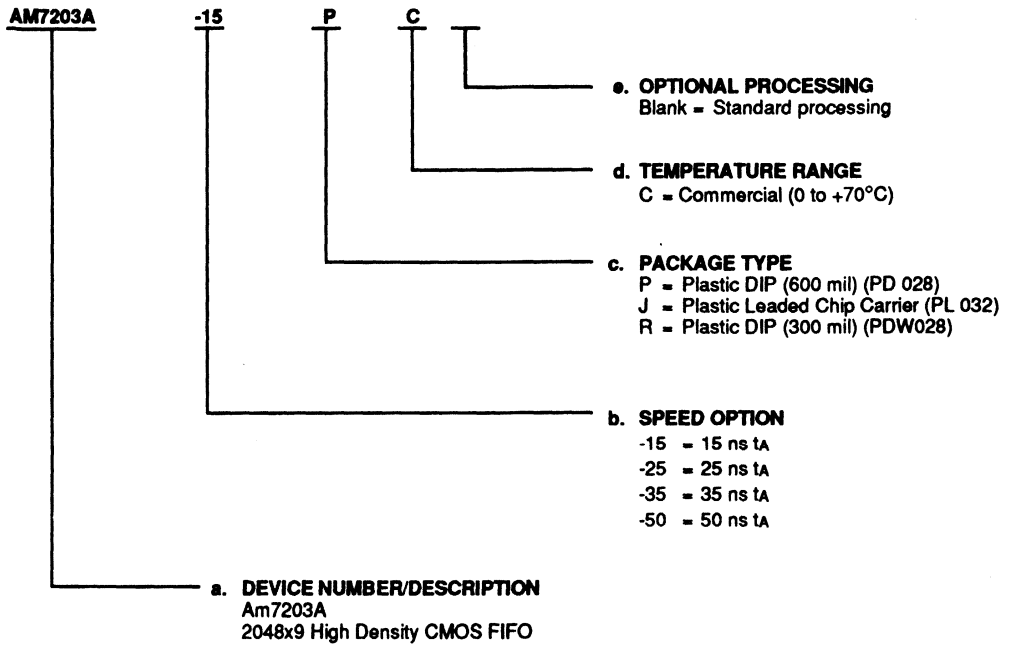


14430-004A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Package Type**
d. **Temperature Range**
e. **Optional Processing**



Valid Combinations	
AM7203A-15	RC, JC
AM7203A-25	PC, RC, JC
AM7203A-35	
AM7203A-50	

Valid Combinations

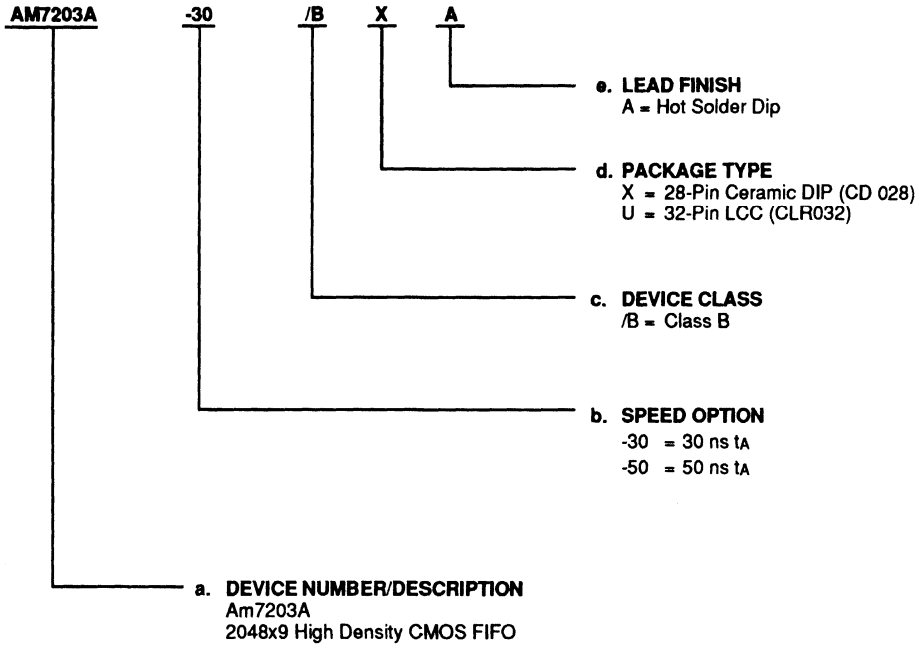
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Device Class**
d. **Package Type**
e. **Lead Finish**



Valid Combinations	
AM7203A-30	/BXA, /BUA
AM7203A-50	

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

D_{0-8}

Data In (Inputs (9))

These nine pins are the data inputs to the FIFO.

$\overline{EF}$

Empty Flag (Output; Active LOW)

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO contains data to be read. The $\overline{EF}$ goes LOW when the read pointer is equal to the write pointer, indicating that the device is empty. $\overline{EF}$ LOW inhibits further Read operations.

The $\overline{EF}$ goes HIGH after the rising edge of Write ($\overline{W}$) during the first write cycle for an empty FIFO (See Figure 4). The $\overline{EF}$ goes LOW after the falling edge of Read ($\overline{R}$) during the read cycle which creates the empty condition.

During a Reset cycle, the $\overline{EF}$ is driven LOW (active).

$\overline{FF}$

Full Flag (Output; Active LOW)

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The $\overline{FF}$ goes LOW when the write pointer is one location less than the read pointer, indicating that the device is full. $\overline{FF}$ LOW inhibits further Write operations.

The $\overline{FF}$ goes HIGH after the rising edge of Read ($\overline{R}$) during the first read cycle following a full condition (See Figure 6). The $\overline{FF}$ goes LOW after the falling edge of Write ($\overline{W}$) during the write cycle which creates the full condition.

During a Reset cycle, the $\overline{FF}$ is driven HIGH (inactive).

$\overline{FL}/\overline{RT}$

First Load/Retransmit (Input; Active LOW)

This is a dual purpose input, dependent upon whether the FIFO is in Single Device Mode or Depth-Expansion Mode.

This pin acts as a FIRST LOAD ($\overline{FL}$) pin when in the Depth-Expansion Mode. The device receiving data first will have the $\overline{FL}$ input tied LOW, while the remaining devices will have the $\overline{FL}$ pin tied HIGH. The states of the $\overline{FL}$ and Expansion In ($\overline{XI}$) pins are used to determine the FIFO's mode of operation, as shown in Tables 1 and 2.

This pin is used as the Retransmit ($\overline{RT}$) input during Single Device Mode. The device can be instructed to retransmit the previously written data when $\overline{RT}$ is pulsed LOW.

GND

Power Supply, Ground

This pin is the 0 V power supply for the FIFO.

NC

No Connect

These pins are not connected.

Q_{0-8}

Data Out (Outputs (9), Three State)

These nine pins are the data outputs for the FIFO. These pins are in a high impedance state whenever Read ($\overline{R}$) is HIGH.

$\overline{R}$

Read (Input; Active LOW)

The falling edge of Read ($\overline{R}$) initiates a read cycle, except when the device is empty, as indicated by the Empty Flag ($\overline{EF}$) being LOW. Valid data appears on the outputs (Q_{0-8}) after the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the Data Outputs (Q_{0-8}) will return to a high impedance condition.

$\overline{RS}$

Reset (Input; Active LOW)

The falling edge of Reset ($\overline{RS}$) is used to reset the FIFO. During Reset, both the read and write pointers are set to the first location in the FIFO. Since the reset cycle initializes the FIFO to an empty condition, the Empty Flag ($\overline{EF}$) is driven LOW (active), and both the Half-Full Flag ($\overline{HF}$) and Full Flag ($\overline{FF}$) are driven HIGH (inactive).

V_{CC}

Power Supply

This pin is the +5 V power supply for the FIFO.

$\overline{W}$

Write (Input; Active LOW)

The falling edge of Write ($\overline{W}$) initiates a write cycle, except when the device is full, as indicated by the Full Flag ($\overline{FF}$) being LOW. Data is latched into the FIFO on the rising edge of $\overline{W}$.

$\overline{XI}$

Expansion In (Input; Active LOW)

Expansion In ($\overline{XI}$) is grounded to indicate operation in the Single Device or Width-Expansion Modes. In Depth Expansion Mode, the $\overline{XI}$ pin is connected to the Expansion Out ($\overline{XO}$) pin of the previous device, except for the $\overline{XI}$ pin of the first device which is connected to the $\overline{XO}$ pin of the last FIFO.

This pin operates at CMOS logic levels, thus providing noise immunity between cascaded devices.

$\overline{XO}/\overline{HF}$

Expansion Out/Half-Full Flag (Output; Active LOW)

This is a dual purpose output, dependent upon whether the device is in Single Device Mode or Depth Expansion Mode.

This pin operates as an Expansion Out ($\overline{XO}$) signal during Depth Expansion Mode. In this mode, the $\overline{XO}$ pin is connected to the Expansion Input ($\overline{XI}$) pin of the following device, except for the $\overline{XO}$ pin of the last device which is connected to the $\overline{XI}$ pin of the first device.

When in Single Device Mode (Expansion In ($\overline{XI}$) pin grounded) this output operates as a Half-Full Flag ($\overline{HF}$). After half the FIFO has been filled, the $\overline{HF}$ will be set LOW at the falling edge of the next Write ($\overline{W}$) operation. The $\overline{HF}$ will remain LOW until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the FIFO. The $\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$ during the read operation which eliminates the half-full condition (See Figure 5).

During a Reset cycle, the $\overline{HF}$ is driven HIGH (inactive).

This pin operates at CMOS logic levels, thus providing noise immunity between cascaded devices.

FUNCTIONAL DESCRIPTION

The Am7203A CMOS FIFO is designed around a 2048x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 2047. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the Am7203A. The write, read, data-in and data-out lines of the Am7203A are connected in parallel, and the Expansion-Out ($\overline{XO}$) and the Expansion-In ($\overline{XI}$) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between $\overline{XO}$ and $\overline{XI}$.

Operational Description

Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of $\overline{XI}$ and $\overline{FL}$ are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ($\overline{R}$) and Write ($\overline{W}$) signals must be HIGH t_{RSS} prior to and t_{RSR} after the rising edge of Reset ($\overline{RS}$). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ($\overline{EF}$) being LOW, active, and both the Half-Full ($\overline{HF}$) and Full Flag ($\overline{FF}$) being HIGH, inactive.

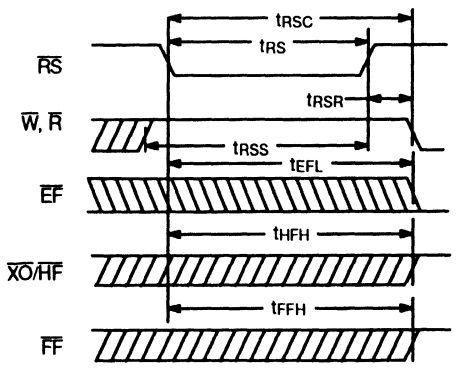


Figure 2. Reset Timing 14430-005A

Writing Data To The FIFO

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The falling edge of Write ($\overline{W}$) initiates a write cycle. (See Figure 3.) Data appearing at inputs D_0–D_8 t_{DS} prior to and t_{DH} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The LOW-to-HIGH transition of the Empty Flag ($\overline{EF}$) occurs t_{WEF} after the rising edge of $\overline{W}$ during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag ($\overline{HF}$) will go LOW t_{WHF} after the falling edge of $\overline{W}$ during the write operation which creates the half-full condition. (See Figure 5.) $\overline{HF}$ will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 1025 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ($\overline{FF}$) goes LOW t_{WFF} after the falling edge of $\overline{W}$ during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 2048 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

A special case of write occurs when a write operation is initiated while the part is full. The next read will cause $\overline{FF}$ to go inactive, and data can then be latched into the FIFO T_{WPF} after the rising edge of $\overline{FF}$ (see Figure 9).

Reading Data From The FIFO

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO is ready to output data. The falling edge of Read ($\overline{R}$) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q_0–Q_8 t_A after the falling edge of $\overline{R}$, and remains until t_{DV} after the rising edge of $\overline{R}$. Q_0–Q_8 return to a high-impedance state when $\overline{R}$ is inactive, when the FIFO is empty, or when the FIFO is in Depth Expansion Mode but is not active.

The Full Flag ($\overline{FF}$) will go HIGH t_{RFF} after the rising edge of $\overline{R}$ during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag ($\overline{HF}$) will go HIGH t_{RHF} after the rising edge of $\overline{R}$ during the read operation, which eliminates the half-full condition. (See Figure 5). $\overline{HF}$ will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 1024 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of $\overline{EF}$ occurs t_{REF} after the falling edge of $\overline{R}$ during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

A special case of read occurs when a read operation is initiated while the part is empty. The data latched in by the next write will be accessed t_A ns after the rising edge of $\overline{EF}$. Read is held active, and cannot be deasserted until T_{RPE} after the rising edge of $\overline{EF}$ (see Figure 8).

Table 1. Reset and Retransmit Truth Table
(Single-Device Configuration/Width-Expansion Mode)

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

Notes:

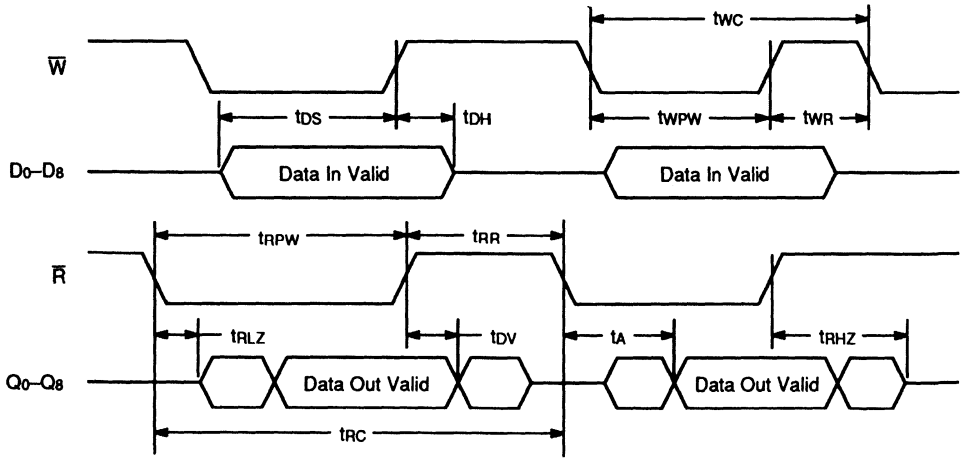
1. Flags will change to show correct state according to write pointer.
2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2. Reset and First Load Truth Table
(Depth-Expansion/Compound-Expansion Mode)

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-first device	0	0	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	$\overline{XO}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

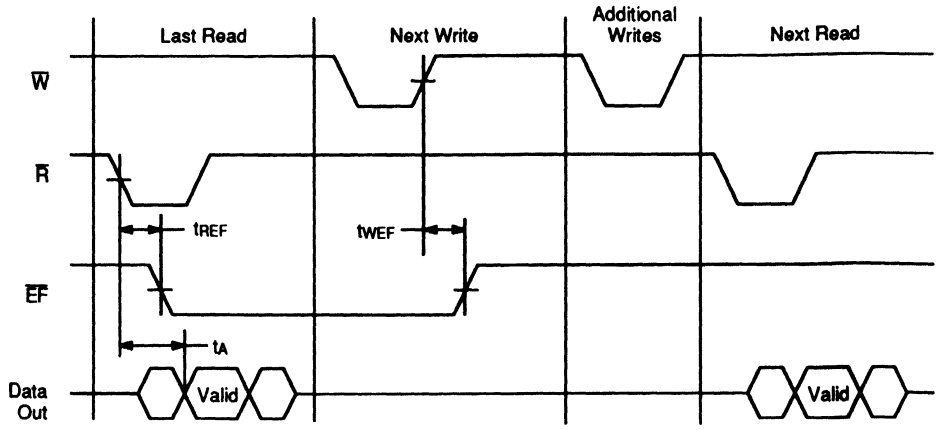
Notes:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
2. Same as during Reset Cycle.
3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.



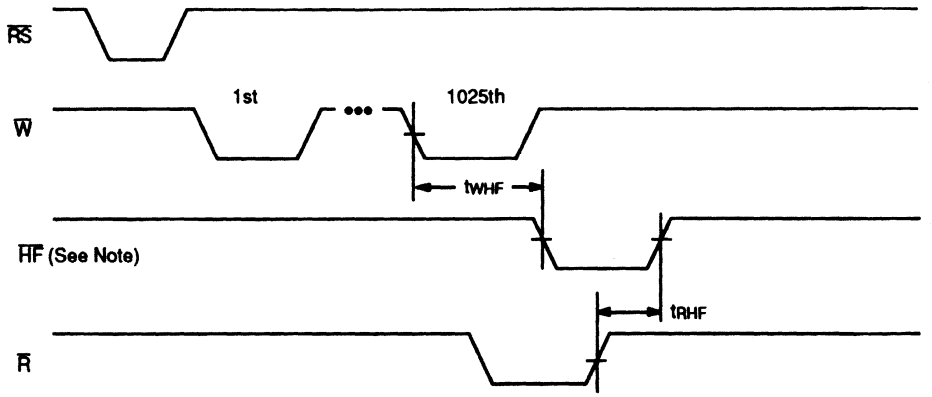
14430-006A

Figure 3. Asynchronous Write and Read Timing



14430-007A

Figure 4. Empty Flag Timing

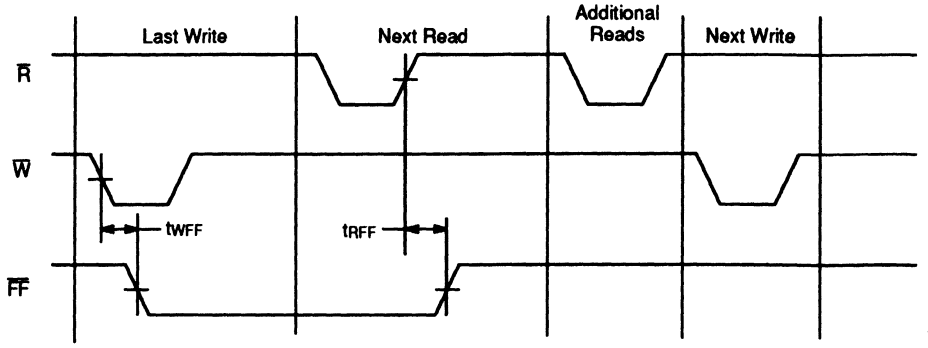


Note:

Depending on the precise phase of W and R, the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when W and R are operating asynchronously near half full.

14430-008A

Figure 5. Half-Full Flag Timing



14430-009A

Figure 6. Full Flag Timing

Half-Full Flag

The Half-Full ($\overline{HF}$) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 1025 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 1025 words, and Read and Write pulses are applied simultaneously, the $\overline{HF}$ flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$ will always settle to the correct state after the appropriate delay, t_{WHF} or t_{RHF}. This property of the Half-Full Flag is clearly a function of the dynamic relation between $\overline{W}$ and $\overline{R}$. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 2048 or less writes between reset cycles.

The $\overline{FL}/\overline{RT}$ is used as the Retransmit ($\overline{RT}$) input in Single-Device Mode. The retransmit capability is intended for use when there are 2048 or less writes between reset cycles. $\overline{RT}$, an active LOW-going pulse of at least t_{RT} in duration, initializes the internal read pointer to address zero and leaves the write pointer unaffected. $\overline{R}$ must be HIGH during the retransmit cycle. The first read cycle should not start until t_{RTR} after the rising edge of $\overline{RT}$. The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO t_{RTC} after the falling edge of $\overline{RT}$. (See Figure 7 and Table 1).

Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ($\overline{XI}$) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The Am7203A can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated due to the skew between devices. 2) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one device's flags are used as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time (t_{WEF}, t_{WHF}, t_{WFF}, t_{REF}, t_{RHF}, and t_{RFF}) for each flag has elapsed.

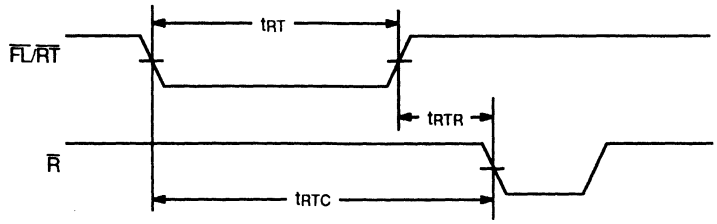
Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ($\overline{XO}$) of one device must be connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device being connected to $\overline{XI}$ of the first device. The device that is to receive data first has its First Load ($\overline{FL}$) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using $\overline{XO}$ and $\overline{XI}$. A LOW-going pulse on $\overline{XO}$ occurs when the last physical location of an active device, address 2048, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the $\overline{FF}$ outputs together. Likewise, a composite Empty Flag is created by OR-ing all the $\overline{EF}$ outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

Compound Expansion

FIFOs of greater width and depth than the Am7203A can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)

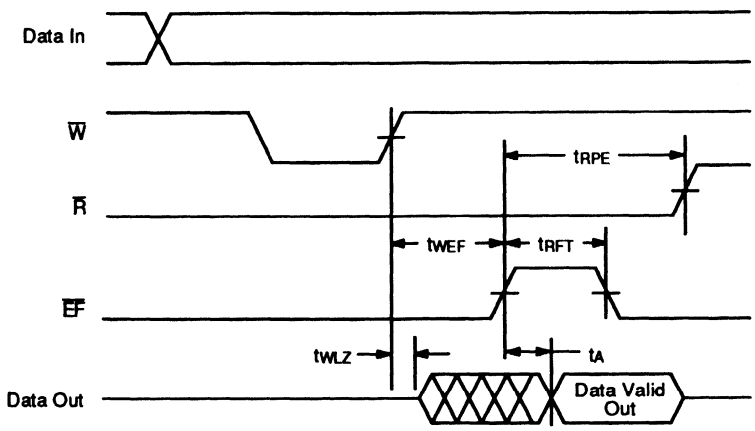


14430-010A

Note:

$\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at t_{RTC}.

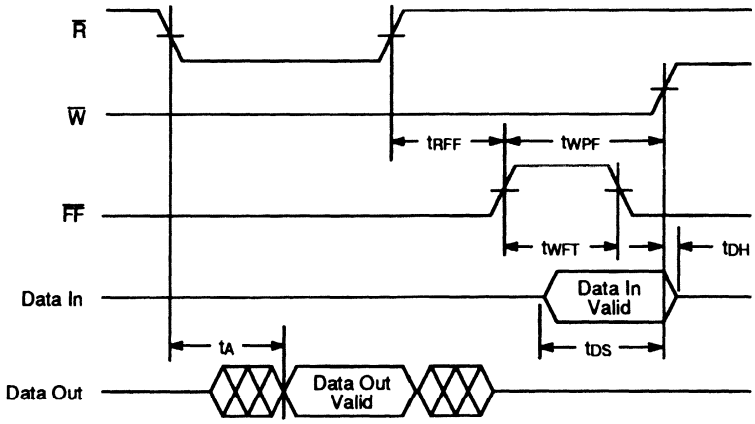
Figure 7. Retransmit Timing



14430-011A

Note: ($t_{RPE} = t_{RPW}$, $t_{RFT} = t_{REF}$)

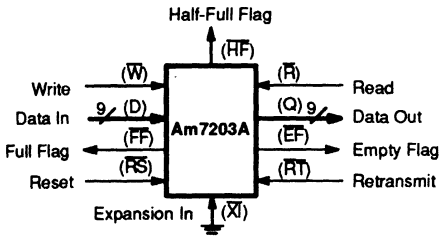
Figure 8. Read Data Flow-Through Mode



Note: ($t_{WPF} = t_{WPW}$, $t_{WFT} = t_{WFF}$)

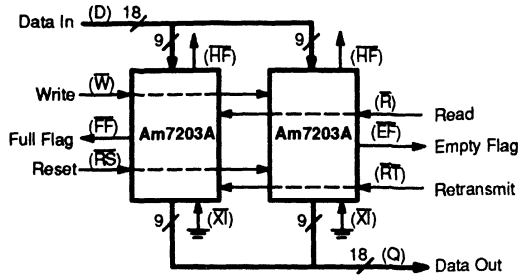
14430-012A

Figure 9. Write Data Flow-Through Mode



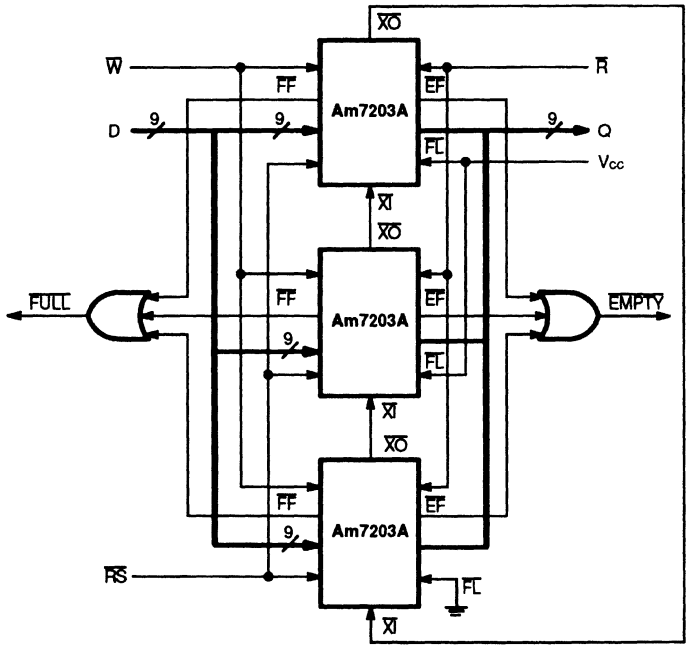
14430-013A

Figure 10. Single FIFO Configuration



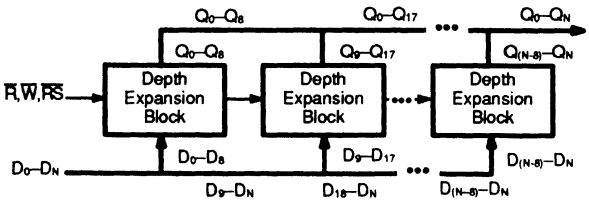
14430-014A

Figure 11. Width-Expansion to Form a 2048x18 FIFO



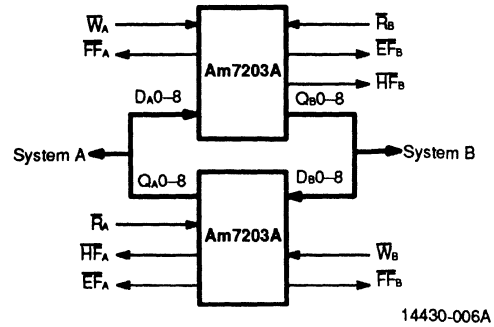
14430-015A

Figure 12. Depth-Expansion to Form 6,144x9 FIFO



14191-016A

Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques



14430-006A

Figure 14. Bidirectional FIFO Configuration

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5V to +7.0 V
Input Voltage	−0.5V to V_{CC} +0.5 V
Ambient Temperature with Power Applied	−55°C to +125°C
Storage Temperature	−55°C to +150°C
Power Dissipation	1.0 W
DC Output Current	50 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0°C to 70°C
Supply Voltage, (V_{CC})	+4.5V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Am7203A-15 t_A = 15 ns		Am7203A-25 t_A = 25 ns		Am7203A-35 t_A = 35 ns		Am7203A-50 t_A = 50 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{IL}	Input Leakage Current (any input) (Note 1)	−1	1	−1	1	−1	1	−1	1	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	−10	10	−10	10	−10	10	−10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	—	1.5	—	1.5	—	1.5	—	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = −2 mA	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8 mA	—	0.4	—	0.4	—	0.4	—	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	—	90	—	70	—	60	—	60	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (Note 4)	—	15	—	15	—	15	—	15	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} −0.2 V) (Note 4)	—	2	—	2	—	2	—	2	mA

Notes:

1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Figures	Am7203A-15		Am7203A-25		Am7203A-35		Am7203A-50		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write and Flag Timing											
t_{WC}	Write Cycle Time	3	25	—	35	—	45	—	65	—	ns
t_{WPW}	Write Pulse Width	3	15	—	25	—	35	—	50	—	ns
t_{WR}	Write Recovery Time	3	10	—	10	—	10	—	15	—	ns
t_{DS}	Data Setup Time	3,9	12	—	15	—	18	—	30	—	ns
t_{DH}	Data Hold Time	3,9	0	—	0	—	0	—	5	—	ns
t_{WFF}	Write LOW to Full Flag LOW	6,9	—	22	—	25	—	30	—	45	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5	—	30	—	35	—	45	—	65	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8	—	22	—	25	—	30	—	45	ns
t_{WLZ}	Write Pulse HIGH to Data Bus at LOW Z (Note 1)	8	5	—	5	—	10	—	15	—	ns
Read and Flag Timing											
t_{RC}	Read Cycle Time	3	25	—	35	—	45	—	65	—	ns
t_A	Access Time	3,4,8,9	—	15	—	25	—	35	—	50	ns
t_{RR}	Read Recovery Time	3	10	—	10	—	10	—	15	—	ns
t_{RPW}	Read Pulse Width	3	15	—	25	—	35	—	50	—	ns
t_{RLZ}	Read Pulse LOW to Data Bus at LOW Z (Note 1)	3	5	—	5	—	5	—	10	—	ns
t_{DV}	Data Valid from Read Pulse HIGH	3	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse HIGH to Data Bus at HIGH Z (Note 1)	3	—	15	—	18	—	20	—	30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9	—	22	—	25	—	30	—	45	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	5	—	30	—	35	—	45	—	65	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8	—	22	—	25	—	30	—	45	ns
Reset Timing											
t_{RSC}	Reset Cycle Time	2	25	—	35	—	45	—	65	—	ns
t_{RS}	Reset Pulse Width	2	15	—	25	—	35	—	50	—	ns
t_{RSS}	Reset Setup Time	2	15	—	25	—	35	—	50	—	ns
t_{RSR}	Reset Recovery Time	2	10	—	10	—	10	—	15	—	ns
t_{EFL}	Reset to Empty Flag LOW	2	—	25	—	35	—	45	—	65	ns
t_{HFH}	Reset to Half-Full Flag High	2	—	25	—	35	—	45	—	65	ns
t_{FFH}	Reset to Full Flag HIGH	2	—	25	—	35	—	45	—	65	ns
Retransmit Timing											
t_{RTC}	Retransmit Cycle Time	7	30	—	35	—	45	—	65	—	ns
t_{RT}	Retransmit Pulse Width	7	20	—	25	—	35	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	7	10	—	10	—	10	—	15	—	ns

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5V to +7.0 V
Input Voltage	−0.5V to V_{CC} +0.5 V
Ambient Temperature with Power Applied	−55 to +125°C
Storage Temperature	−65 to +155°C
Power Dissipation	1.0 W
DC Output Current	50 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices*

Case Temperature (T_C)	−55 to 125°C
Supply Voltage, (V_{CC})	+4.5V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

**Military product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.*

DC CHARACTERISTICS over MILITARY operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Am7203A-30 t_A = 30 ns		Am7203A-50 t_A = 50 ns		Unit
		Min.	Max.	Min.	Max.	
I_{IL}	Input Leakage Current (any input) (Note 1)	−10	10	−10	10	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	−10	10	−10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.2	—	2.2	—	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	—	0.8	—	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	—	3.5	—	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	—	1.5	—	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = −2 mA	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8 mA	—	0.4	—	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	—	100	—	90	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}) (Note 4)	—	15	—	15	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} −0.2 V) (Note 4)	—	4	—	4	mA

Notes:

1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

SWITCHING CHARACTERISTICS over MILITARY operating range unless otherwise specified.

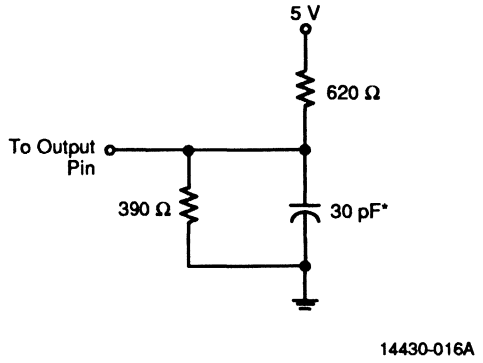
Parameter Symbol	Parameter Description	Figures	Am7203A-30		Am7203A-50		Unit
			Min.	Max.	Min.	Max.	
Write and Flag Timing							
t_{WC}	Write Cycle Time	3	40	—	65	—	ns
t_{WPW}	Write Pulse Width	3	30	—	50	—	ns
t_{WR}	Write Recovery Time	3	10	—	15	—	ns
t_{DS}	Data Setup Time	3,9	18	—	30	—	ns
t_{DH}	Data Hold Time	3,9	0	—	5	—	ns
t_{WFF}	Write LOW to Full Flag LOW	6,9	—	30	—	45	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5	—	40	—	65	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8	—	30	—	45	ns
t_{WLZ}	Write Pulse HIGH to Data Bus at LOW Z (Note 1)	8	5	—	15	—	ns
Read and Flag Timing							
t_{RC}	Read Cycle Time	3	40	—	65	—	ns
t_A	Access Time	3,4,8,9	—	30	—	50	ns
t_{RR}	Read Recovery Time	3	10	—	15	—	ns
t_{RPW}	Read Pulse Width	3	30	—	50	—	ns
t_{RLZ}	Read Pulse LOW to Data Bus at LOW Z (Note 1)	3	5	—	10	—	ns
t_{DV}	Data Valid from Read Pulse HIGH	3	5	—	5	—	ns
t_{RHZ}	Read Pulse HIGH to Data Bus at HIGH Z (Note 1)	3	—	20	—	30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9	—	30	—	45	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	5	—	40	—	65	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8	—	30	—	45	ns
Reset Timing							
t_{RSC}	Reset Cycle Time	2	40	—	65	—	ns
t_{RS}	Reset Pulse Width	2	30	—	50	—	ns
t_{RSS}	Reset Setup Time	2	30	—	50	—	ns
t_{RSR}	Reset Recovery Time	2	10	—	15	—	ns
t_{EFL}	Reset to Empty Flag LOW	2	—	40	—	65	ns
t_{HFH}	Reset to Half-Full Flag High	2	—	40	—	65	ns
t_{FFH}	Reset to Full Flag HIGH	2	—	40	—	65	ns
Retransmit Timing							
t_{RTC}	Retransmit Cycle Time	7	40	—	65	—	ns
t_{RT}	Retransmit Pulse Width	7	30	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	7	10	—	15	—	ns

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See Figure 15



* Includes jig and scope capacitances.

Figure 15. AC Test Load

CAPACITANCE (V_{CC} = 5.0 V, T_A = +25°C, f = 1.0 MHz)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V	5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	7	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

Am7204A

High Density First-In First-Out (FIFO) 4096x9-Bit CMOS Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 4096x9 organization
- Cycle times of 25/35/45/65 nanoseconds for Standard products
- Cycle times of 40/65 nanoseconds for APL products
- Asynchronous and simultaneous writes and reads
- Low power consumption
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for $\overline{XI}$ - CMOS threshold
- Functional and pin compatible with industry standard devices

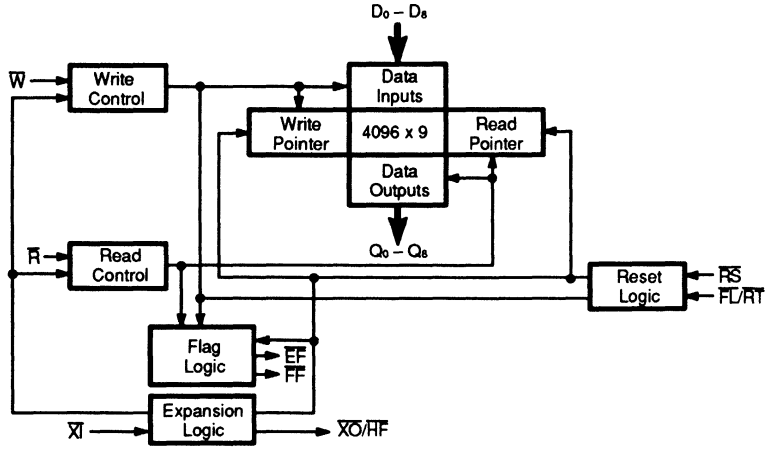
GENERAL DESCRIPTION

The Am7204A is a RAM-based CMOS FIFO that is 4096 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can input and output data asynchronously and simultaneously at data rates from 0 to 40 MHz for Standard Products and 0 to 25 MHz for APL products. Status flags are provided to signify empty, full and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7204A are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7204A useful in communication, image processing, mass storage, DSP, and printing systems.

BLOCK DIAGRAM



14430-001A

Figure 1.

PRODUCT SELECTOR GUIDE

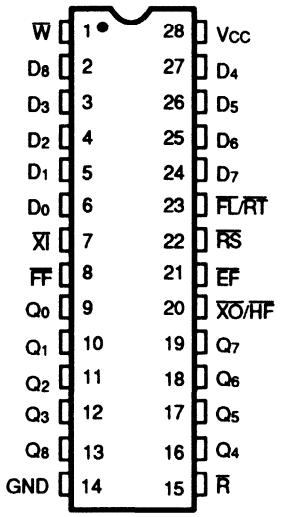
Part Number	Am7204A-15	Am7204A-25	Am7204A-35	Am7204A-50	Am7204A-30	Am7204A-50
Access Time	15 ns	25 ns	35 ns	50 ns	30 ns	50 ns
Maximum Power Supply Current	90 mA	70 mA	60 mA	60 mA	100 mA	90 mA
Operating Frequency	40 MHz	28.5 MHz	22.2 MHz	15.3 MHz	25 MHz	15.3 MHz
Operating Range	Com'l	Com'l	Com'l	Com'l	Mil	Mil

Publication# 14430 Rev. B Amendment/0
Issue Date: March 1991

CONNECTION DIAGRAMS

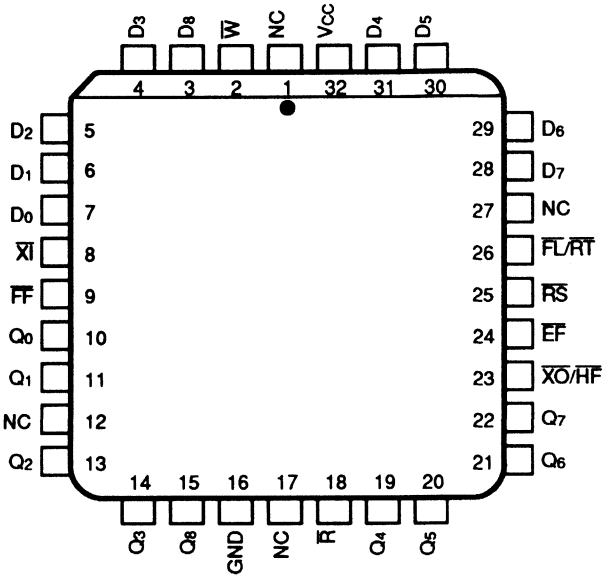
Top View

DIPs*



14430-002A

PLCC/LCC



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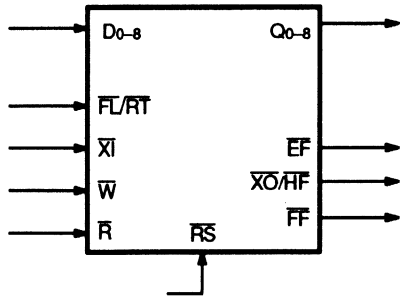
Note:
Pin 1 is marked for orientation for plastic packages.

*Pinout identical for both plastic and ceramic DIPs.

LOGIC SYMBOL

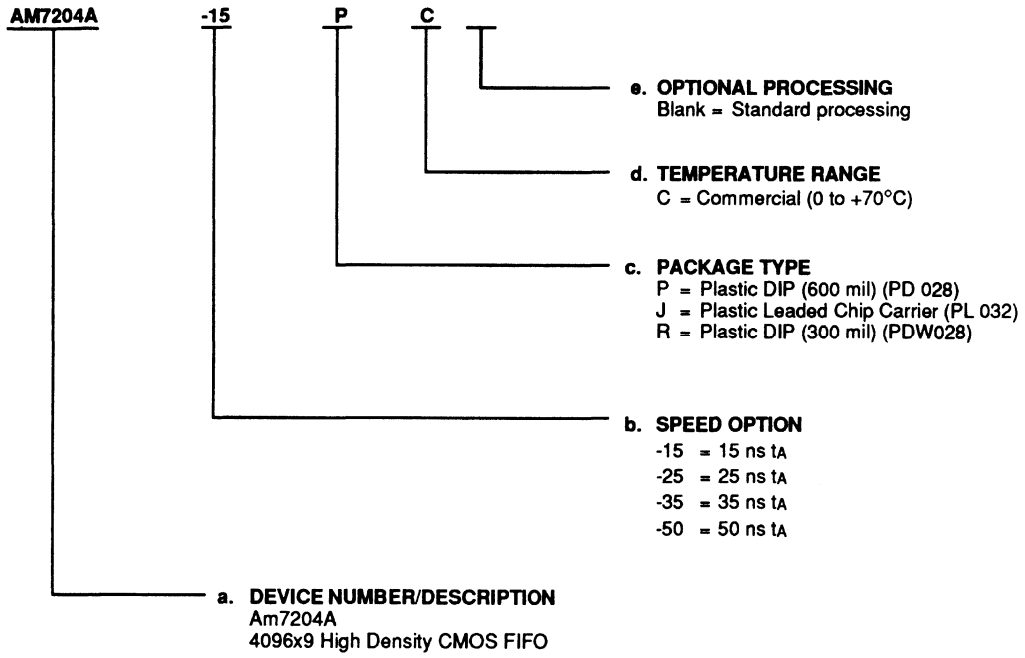


14430-004A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7204A-15	RC, JC
AM7204A-25	PC, RC, JC
AM7204A-35	
AM7204A-50	

Valid Combinations

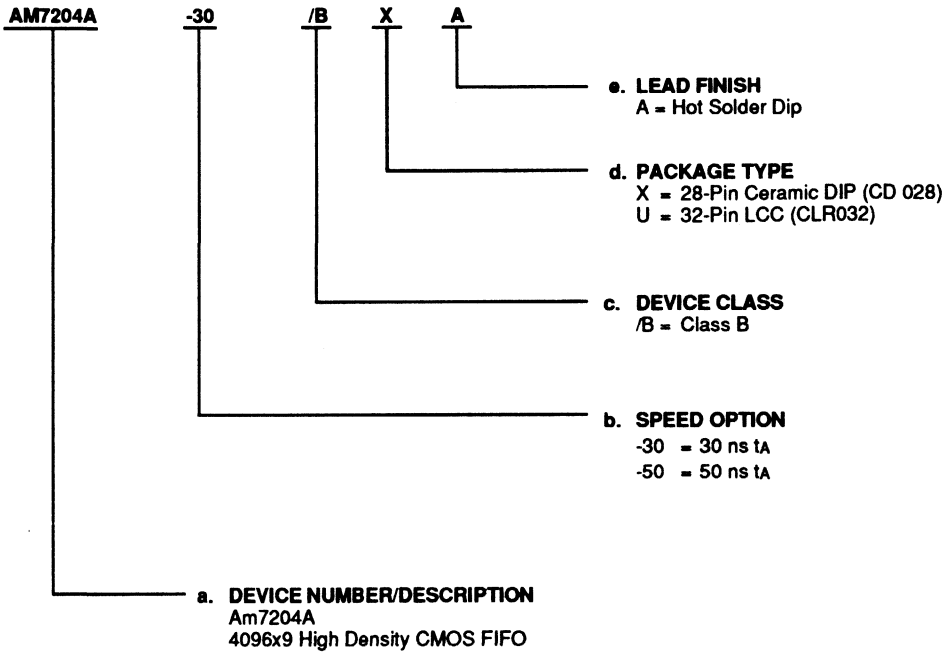
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM7204A-30	/BXA, /BUA
AM7204A-50	

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

D_{0-8}

Data In (Inputs (9))

These nine pins are the data inputs to the FIFO.

$\overline{EF}$

Empty Flag (Output; Active LOW)

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO contains data to be read. The $\overline{EF}$ goes LOW when the read pointer is equal to the write pointer, indicating that the device is empty. $\overline{EF}$ LOW inhibits further Read operations.

The $\overline{EF}$ goes HIGH after the rising edge of Write ($\overline{W}$) during the first write cycle for an empty FIFO (See Figure 4). The $\overline{EF}$ goes LOW after the falling edge of Read ($\overline{R}$) during the read cycle which creates the empty condition.

During a Reset cycle, the $\overline{EF}$ is driven LOW (active).

$\overline{FF}$

Full Flag (Output; Active LOW)

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The $\overline{FF}$ goes LOW when the write pointer is one location less than the read pointer, indicating that the device is full. $\overline{FF}$ LOW inhibits further Write operations.

The $\overline{FF}$ goes HIGH after the rising edge of Read ($\overline{R}$) during the first read cycle following a full condition (See Figure 6). The $\overline{FF}$ goes LOW after the falling edge of Write ($\overline{W}$) during the write cycle which creates the full condition.

During a Reset cycle, the $\overline{FF}$ is driven HIGH (inactive).

$\overline{FL}/\overline{RT}$

First Load/Retransmit (Input; Active LOW)

This is a dual purpose input, dependent upon whether the FIFO is in Single Device Mode or Depth-Expansion Mode.

This pin acts as a FIRST LOAD ($\overline{FL}$) pin when in the Depth-Expansion Mode. The device receiving data first will have the $\overline{FL}$ input tied LOW, while the remaining devices will have the $\overline{FL}$ pin tied HIGH. The states of the $\overline{FL}$ and Expansion In ($\overline{XI}$) pins are used to determine the FIFO's mode of operation, as shown in Tables 1 and 2.

This pin is used as the Retransmit ($\overline{RT}$) input during Single Device Mode. The device can be instructed to retransmit the previously written data when $\overline{RT}$ is pulsed LOW.

GND

Power Supply, Ground

This pin is the 0 V power supply for the FIFO.

NC

No Connect

These pins are not connected.

Q_{0-8}

Data Out (Outputs (9), Three State)

These nine pins are the data outputs for the FIFO. These pins are in a high impedance state whenever Read ($\overline{R}$) is HIGH.

$\overline{R}$

Read (Input; Active LOW)

The falling edge of Read ($\overline{R}$) initiates a read cycle, except when the device is empty, as indicated by the Empty Flag ($\overline{EF}$) being LOW. Valid data appears on the outputs (Q_{0-8}) after the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the Data Outputs (Q_{0-8}) will return to a high impedance condition.

$\overline{RS}$

Reset (Input; Active LOW)

The falling edge of Reset ($\overline{RS}$) is used to reset the FIFO. During Reset, both the read and write pointers are set to the first location in the FIFO. Since the reset cycle initializes the FIFO to an empty condition, the Empty Flag ($\overline{EF}$) is driven LOW (active), and both the Half-Full Flag ($\overline{HF}$) and Full Flag ($\overline{FF}$) are driven HIGH (inactive).

V_{CC}

Power Supply

This pin is the +5 V power supply for the FIFO.

$\overline{W}$

Write (Input; Active LOW)

The falling edge of Write ($\overline{W}$) initiates a write cycle, except when the device is full, as indicated by the Full Flag ($\overline{FF}$) being LOW. Data is latched into the FIFO on the rising edge of $\overline{W}$.

$\overline{XI}$

Expansion In (Input; Active LOW)

Expansion In ($\overline{XI}$) is grounded to indicate operation in the Single Device or Width-Expansion Modes. In Depth Expansion Mode, the $\overline{XI}$ pin is connected to the Expansion Out ($\overline{XO}$) pin of the previous device, except for the $\overline{XI}$ pin of the first device which is connected to the $\overline{XO}$ pin of the last FIFO.

This pin operates at CMOS logic levels, thus providing noise immunity between cascaded devices.

$\overline{XO}/\overline{HF}$

Expansion Out/Half-Full Flag (Output; Active LOW)

This is a dual purpose output, dependent upon whether the device is in Single Device Mode or Depth Expansion Mode.

This pin operates as an Expansion Out ($\overline{XO}$) signal during Depth Expansion Mode. In this mode, the $\overline{XO}$ pin is connected to the Expansion Input ($\overline{XI}$) pin of the following device, except for the $\overline{XO}$ pin of the last device which is connected to the $\overline{XI}$ pin of the first device.

When in Single Device Mode (Expansion In ($\overline{XI}$) pin grounded) this output operates as a Half-Full Flag ($\overline{HF}$). After half the FIFO has been filled, the $\overline{HF}$ will be set LOW at the falling edge of the next Write ($\overline{W}$) operation. The $\overline{HF}$ will remain LOW until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the FIFO. The $\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$ during the read operation which eliminates the half-full condition (See Figure 5).

During a Reset cycle, the $\overline{HF}$ is driven HIGH (inactive).

This pin operates at CMOS logic levels, thus providing noise immunity between cascaded devices.

FUNCTIONAL DESCRIPTION

The Am7204A CMOS FIFO is designed around a 4096x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 4095. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the Am7204A. The write, read, data-in and data-out lines of the Am7204A are connected in parallel, and the Expansion-Out ($\overline{XO}$) and the Expansion-In ($\overline{XI}$) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between $\overline{XO}$ and $\overline{XI}$.

Operational Description

Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of $\overline{XI}$ and $\overline{FL}$ are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ($\overline{R}$) and Write ($\overline{W}$) signals must be HIGH t_{RSS} prior to and t_{RSR} after the rising edge of Reset ($\overline{RS}$). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ($\overline{EF}$) being LOW, active, and both the Half-Full ($\overline{HF}$) and Full Flag ($\overline{FF}$) being HIGH, inactive.

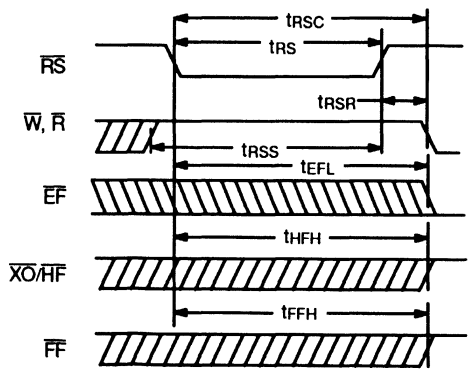


Figure 2. Reset Timing 14430-005A

Writing Data To The FIFO

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The falling edge of Write ($\overline{W}$) initiates a write cycle. (See Figure 3.) Data appearing at inputs D_0–D_8 t_{DS} prior to and t_{DH} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The LOW-to-HIGH transition of the Empty Flag ($\overline{EF}$) occurs t_{WEF} after the rising edge of $\overline{W}$ during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag ($\overline{HF}$) will go LOW t_{WHF} after the falling edge of $\overline{W}$ during the write operation which creates the half-full condition. (See Figure 5.) $\overline{HF}$ will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 2049 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ($\overline{FF}$) goes LOW t_{WFF} after the falling edge of $\overline{W}$ during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 4096 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

A special case of write occurs when a write operation is initiated while the part is full. The next read will cause $\overline{FF}$ to go inactive, and data can then be latched into the FIFO T_{WPF} after the rising edge of $\overline{FF}$ (see Figure 9).

Reading Data From The FIFO

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO is ready to output data. The falling edge of Read ($\overline{R}$) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q_0–Q_8 t_A after the falling edge of $\overline{R}$, and remains until t_{DV} after the rising edge of $\overline{R}$. Q_0–Q_8 return to a high-impedance state when $\overline{R}$ is inactive, when the FIFO is empty, or when the FIFO is in Depth Expansion Mode but is not active.

The Full Flag ($\overline{FF}$) will go HIGH t_{RFF} after the rising edge of $\overline{R}$ during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag ($\overline{HF}$) will go HIGH t_{RHF} after the rising edge of $\overline{R}$ during the read operation, which eliminates the half-full condition. (See Figure 5). $\overline{HF}$ will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 2048 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of $\overline{EF}$ occurs t_{REF} after the falling edge of $\overline{R}$ during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

A special case of read occurs when a read operation is initiated while the part is empty. The data latched in by the next write will be accessed t_A ns after the rising edge of $\overline{EF}$. Read is held active, and cannot be deasserted until T_{RPE} after the rising edge of $\overline{EF}$ (see Figure 8).

Table 1. Reset and Retransmit Truth Table
(Single-Device Configuration/Width-Expansion Mode)

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

Notes:

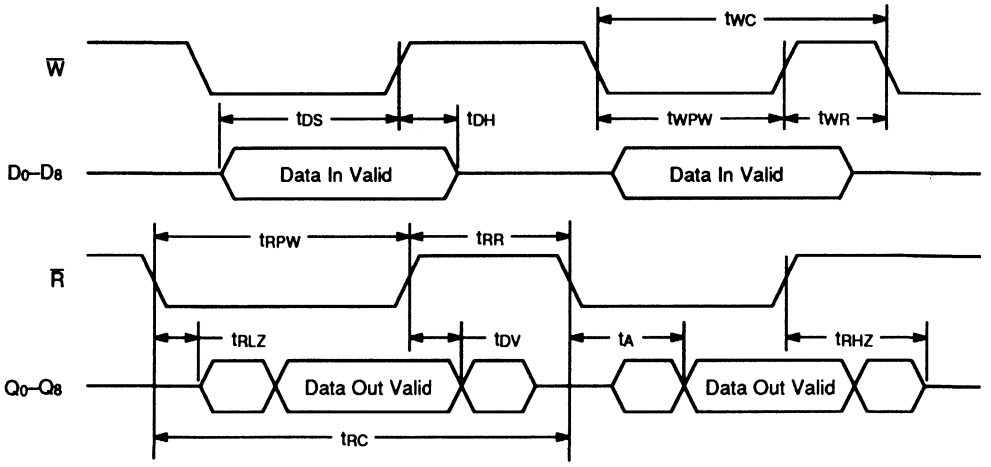
1. Flags will change to show correct state according to write pointer.
2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2. Reset and First Load Truth Table
(Depth-Expansion/Compound-Expansion Mode)

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-first device	0	0	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	$\overline{XO}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

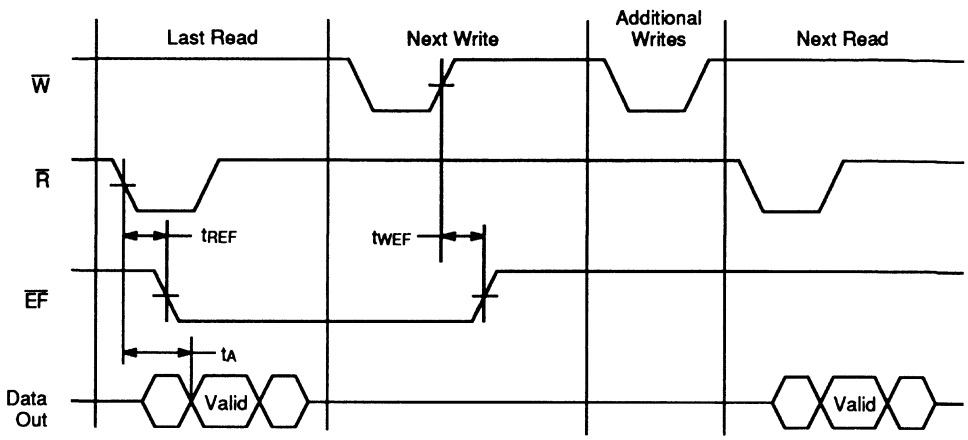
Notes:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
2. Same as during Reset Cycle.
3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.



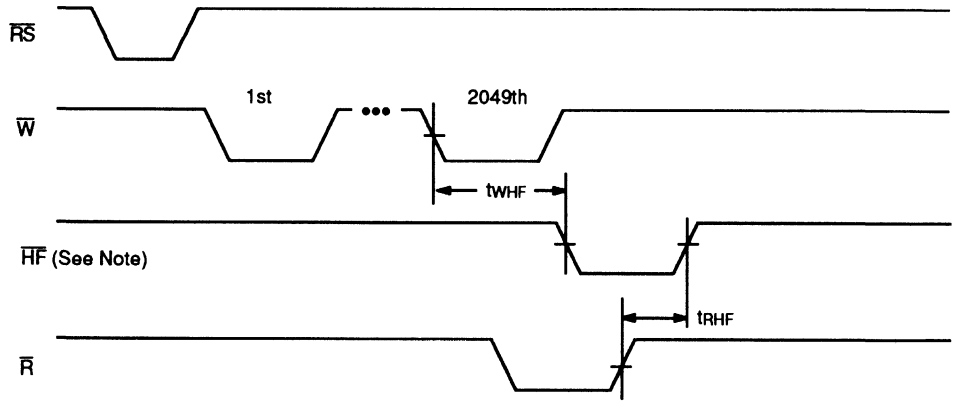
14430-006A

Figure 3. Asynchronous Write and Read Timing



14430-007A

Figure 4. Empty Flag Timing

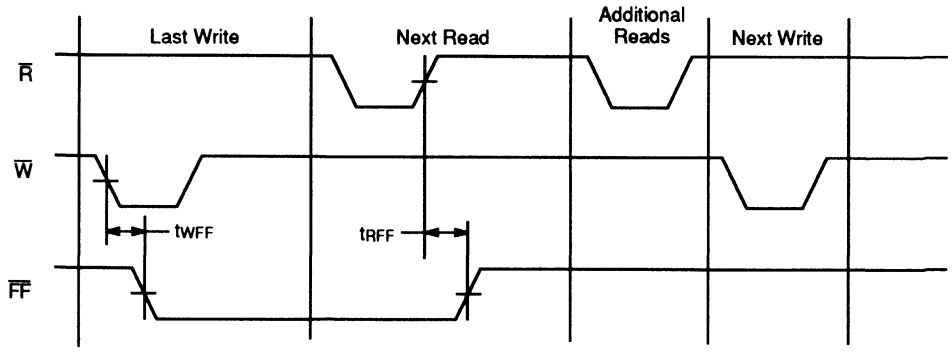


Note:

Depending on the precise phase of W and R, the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when W and R are operating asynchronously near half full.

14430-008A

Figure 5. Half-Full Flag Timing



14430-009A

Figure 6. Full Flag Timing

Half-Full Flag

The Half-Full ($\overline{HF}$) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 2049 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 2049 words, and Read and Write pulses are applied simultaneously, the $\overline{HF}$ flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$ will always settle to the correct state after the appropriate delay, t_{WHF} or t_{RHF}. This property of the Half-Full Flag is clearly a function of the dynamic relation between $\overline{W}$ and $\overline{R}$. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 4096 or less writes between reset cycles.

The $\overline{FL}/\overline{RT}$ is used as the Retransmit ($\overline{RT}$) input in Single-Device Mode. The retransmit capability is intended for use when there are 4096 or less writes between reset cycles. $\overline{RT}$, an active LOW-going pulse of at least t_{RT} in duration, initializes the internal read pointer to address zero and leaves the write pointer unaffected. $\overline{R}$ must be HIGH during the retransmit cycle. The first read cycle should not start until t_{RTR} after the rising edge of $\overline{RT}$. The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO t_{RTC} after the falling edge of $\overline{RT}$. (See Figure 7 and Table 1).

Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ($\overline{XI}$) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The Am7204A can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated due to the skew between devices. 2) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one device's flags are used as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time (t_{WEF}, t_{WHF}, t_{WFF}, t_{REF}, t_{RHF}, and t_{RFF}) for each flag has elapsed.

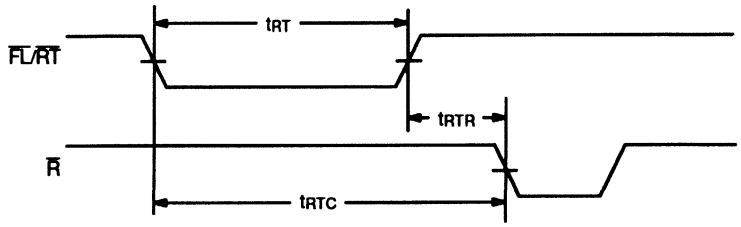
Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ($\overline{XO}$) of one device must be connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device being connected to $\overline{XI}$ of the first device. The device that is to receive data first has its First Load ($\overline{FL}$) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using $\overline{XO}$ and $\overline{XI}$. A LOW-going pulse on $\overline{XO}$ occurs when the last physical location of an active device, address 4096, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the $\overline{FF}$ outputs together. Likewise, a composite Empty Flag is created by OR-ing all the $\overline{EF}$ outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

Compound Expansion

FIFOs of greater width and depth than the Am7204A can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)

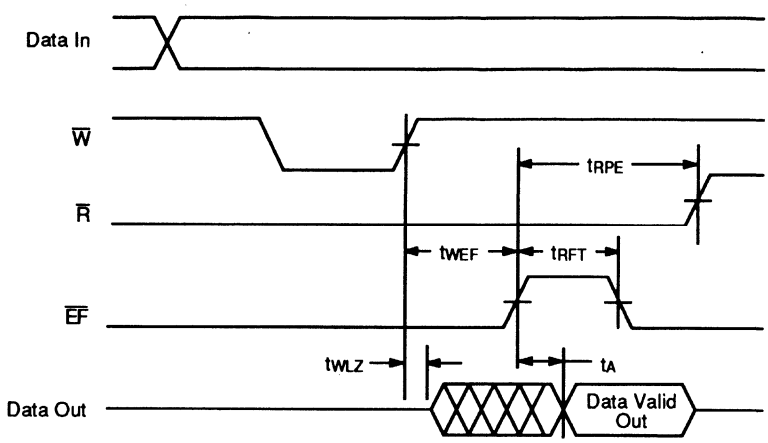


14430-010A

Note:

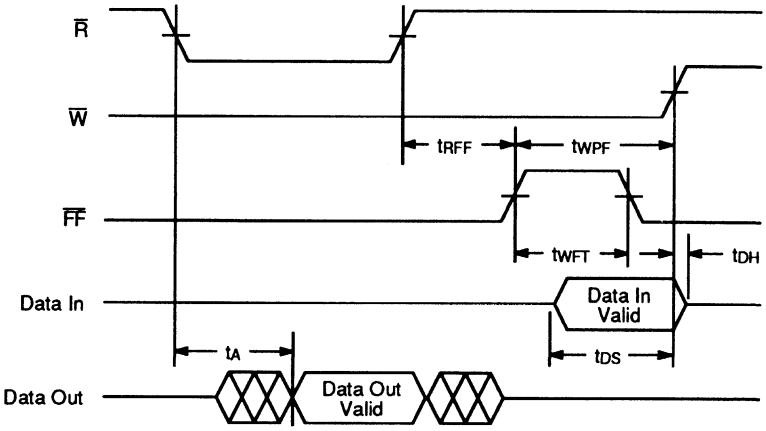
$\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at t_{RTC}.

Figure 7. Retransmit Timing



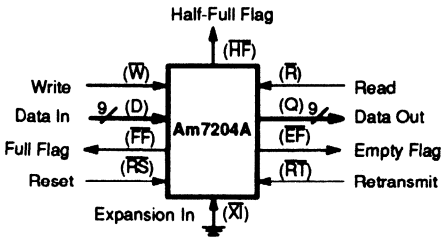
Note: ($t_{RPE} = t_{RPW}$, $t_{RFT} = t_{REF}$)

Figure 8. Read Data Flow-Through Mode



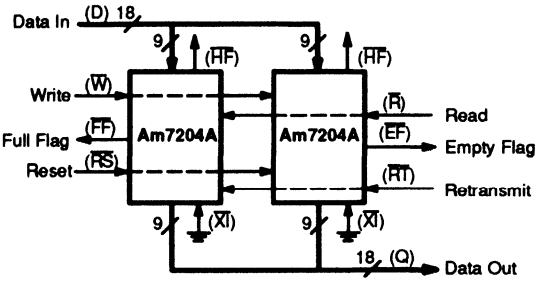
Note: ($t_{WPF} = t_{WPW}$, $t_{WFT} = t_{WFF}$)

Figure 9. Write Data Flow-Through Mode



14430-013A

Figure 10. Single FIFO Configuration



14430-014A

Figure 11. Width-Expansion to Form a 4096x18 FIFO

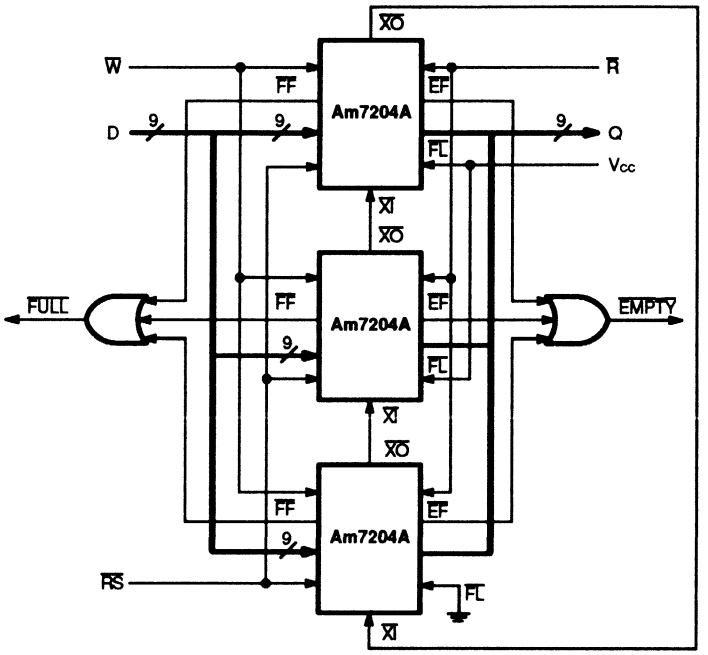


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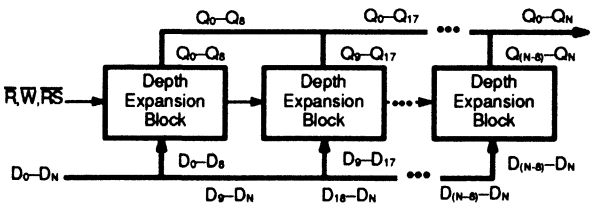
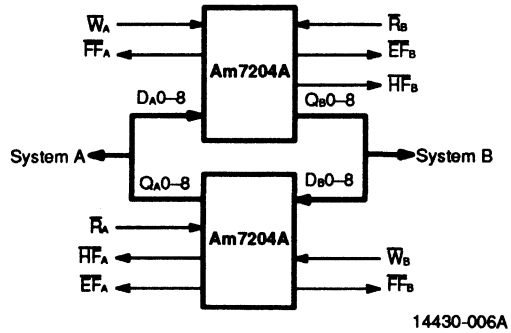
Figure 12. Depth-Expansion to Form 12,288x9 FIFO



14191-016A

Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques



14430-006A

Figure 14. Bidirectional FIFO Configuration

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5V to +7.0 V
Input Voltage	−0.5V to V_{CC} +0.5 V
Ambient Temperature with Power Applied	−55°C to +125°C
Storage Temperature	−55°C to +150°C
Power Dissipation	1.0 W
DC Output Current	50 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0°C to 70°C
Supply Voltage, (V_{CC})	+4.5V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Am7204A-15 t_A = 15 ns		Am7204A-25 t_A = 25 ns		Am7204A-35 t_A = 35 ns		Am7204A-50 t_A = 50 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{IL}	Input Leakage Current (any input) (Note 1)	−1	1	−1	1	−1	1	−1	1	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	−10	10	−10	10	−10	10	−10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	—	1.5	—	1.5	—	1.5	—	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = −2 mA	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8 mA	—	0.4	—	0.4	—	0.4	—	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	—	90	—	70	—	60	—	60	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}) (Note 4)	—	15	—	15	—	15	—	15	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} −0.2 V) (Note 4)	—	2	—	2	—	2	—	2	mA

Notes:

1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Figures	Am7204A-15		Am7204A-25		Am7204A-35		Am7204A-50		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write and Flag Timing											
t_{WC}	Write Cycle Time	3	25	—	35	—	45	—	65	—	ns
t_{WPW}	Write Pulse Width	3	15	—	25	—	35	—	50	—	ns
t_{WR}	Write Recovery Time	3	10	—	10	—	10	—	15	—	ns
t_{DS}	Data Setup Time	3,9	12	—	15	—	18	—	30	—	ns
t_{DH}	Data Hold Time	3,9	0	—	0	—	0	—	5	—	ns
t_{WFF}	Write LOW to Full Flag LOW	6,9	—	22	—	25	—	30	—	45	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5	—	30	—	35	—	45	—	65	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8	—	22	—	25	—	30	—	45	ns
t_{WLZ}	Write Pulse HIGH to Data Bus at LOW Z (Note 1)	8	5	—	5	—	10	—	15	—	ns
Read and Flag Timing											
t_{RC}	Read Cycle Time	3	25	—	35	—	45	—	65	—	ns
t_A	Access Time	3,4,8,9	—	15	—	25	—	35	—	50	ns
t_{RR}	Read Recovery Time	3	10	—	10	—	10	—	15	—	ns
t_{RPW}	Read Pulse Width	3	15	—	25	—	35	—	50	—	ns
t_{RLZ}	Read Pulse LOW to Data Bus at LOW Z (Note 1)	3	5	—	5	—	5	—	10	—	ns
t_{DV}	Data Valid from Read Pulse HIGH	3	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse HIGH to Data Bus at HIGH Z (Note 1)	3	—	15	—	18	—	20	—	30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9	—	22	—	25	—	30	—	45	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	5	—	30	—	35	—	45	—	65	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8	—	22	—	25	—	30	—	45	ns
Reset Timing											
t_{RSC}	Reset Cycle Time	2	25	—	35	—	45	—	65	—	ns
t_{RS}	Reset Pulse Width	2	15	—	25	—	35	—	50	—	ns
t_{RSS}	Reset Setup Time	2	15	—	25	—	35	—	50	—	ns
t_{RSR}	Reset Recovery Time	2	10	—	10	—	10	—	15	—	ns
t_{EFL}	Reset to Empty Flag LOW	2	—	25	—	35	—	45	—	65	ns
t_{HFH}	Reset to Half-Full Flag High	2	—	25	—	35	—	45	—	65	ns
t_{FFH}	Reset to Full Flag HIGH	2	—	25	—	35	—	45	—	65	ns
Retransmit Timing											
t_{RTC}	Retransmit Cycle Time	7	30	—	35	—	45	—	65	—	ns
t_{RT}	Retransmit Pulse Width	7	20	—	25	—	35	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	7	10	—	10	—	10	—	15	—	ns

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5V to +7.0 V
Input Voltage	−0.5V to V_{CC} +0.5 V
Ambient Temperature with Power Applied	−55 to +125°C
Storage Temperature	−65 to +155°C
Power Dissipation	1.0 W
DC Output Current	50 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices*

Case Temperature (T_C)	−55 to 125°C
Supply Voltage, (V_{CC})	+4.5V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

**Military product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.*

DC CHARACTERISTICS over MILITARY operating range unless otherwise specified.

Parameter Symbol	Parameter Description	Am7204A-30 t_A = 30 ns		Am7204A-50 t_A = 50 ns		Unit
		Min.	Max.	Min.	Max.	
I_{IL}	Input Leakage Current (any input) (Note 1)	−10	10	−10	10	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	−10	10	−10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.2	—	2.2	—	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	—	0.8	—	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	—	3.5	—	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	—	1.5	—	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = −2 mA	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8 mA	—	0.4	—	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	—	100	—	90	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}) (Note 4)	—	15	—	15	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} −0.2 V) (Note 4)	—	4	—	4	mA

Notes:

1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

SWITCHING CHARACTERISTICS over MILITARY operating range unless otherwise specified.

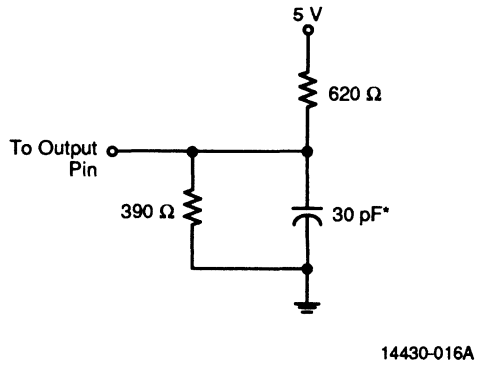
Parameter Symbol	Parameter Description	Figures	Am7204A-30		Am7204A-50		Unit
			Min.	Max.	Min.	Max.	
Write and Flag Timing							
t_{WC}	Write Cycle Time	3	40	—	65	—	ns
t_{WPW}	Write Pulse Width	3	30	—	50	—	ns
t_{WR}	Write Recovery Time	3	10	—	15	—	ns
t_{DS}	Data Setup Time	3,9	18	—	30	—	ns
t_{DH}	Data Hold Time	3,9	0	—	5	—	ns
t_{WFF}	Write LOW to Full Flag LOW	6,9	—	30	—	45	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5	—	40	—	65	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8	—	30	—	45	ns
t_{WLZ}	Write Pulse HIGH to Data Bus at LOW Z (Note 1)	8	5	—	15	—	ns
Read and Flag Timing							
t_{RC}	Read Cycle Time	3	40	—	65	—	ns
t_A	Access Time	3,4,8,9	—	30	—	50	ns
t_{RR}	Read Recovery Time	3	10	—	15	—	ns
t_{RPW}	Read Pulse Width	3	30	—	50	—	ns
t_{RLZ}	Read Pulse LOW to Data Bus at LOW Z (Note 1)	3	5	—	10	—	ns
t_{DV}	Data Valid from Read Pulse HIGH	3	5	—	5	—	ns
t_{RHZ}	Read Pulse HIGH to Data Bus at HIGH Z (Note 1)	3	—	20	—	30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9	—	30	—	45	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	5	—	40	—	65	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8	—	30	—	45	ns
Reset Timing							
t_{RSC}	Reset Cycle Time	2	40	—	65	—	ns
t_{RS}	Reset Pulse Width	2	30	—	50	—	ns
t_{RSS}	Reset Setup Time	2	30	—	50	—	ns
t_{RSR}	Reset Recovery Time	2	10	—	15	—	ns
t_{EFL}	Reset to Empty Flag LOW	2	—	40	—	65	ns
t_{HFH}	Reset to Half-Full Flag High	2	—	40	—	65	ns
t_{FFH}	Reset to Full Flag HIGH	2	—	40	—	65	ns
Retransmit Timing							
t_{RTC}	Retransmit Cycle Time	7	40	—	65	—	ns
t_{RT}	Retransmit Pulse Width	7	30	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	7	10	—	15	—	ns

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See Figure 15



* Includes jig and scope capacitances.

Figure 15. AC Test Load

CAPACITANCE (V_{CC} = 5.0 V, T_A = +25°C, f = 1.0 MHz)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V	5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	7	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

Am7205A

High Density First-In First-Out (FIFO) 8192x9-Bit CMOS Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 8192x9 organization
- Cycle times of 25/35/45 nanoseconds for standard products
- Asynchronous and simultaneous writes and reads
- Low power consumption
- Status flags – full, half-full, empty
- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for $\overline{XI}$-CMOS threshold
- Functional and pin compatible with industry standard devices

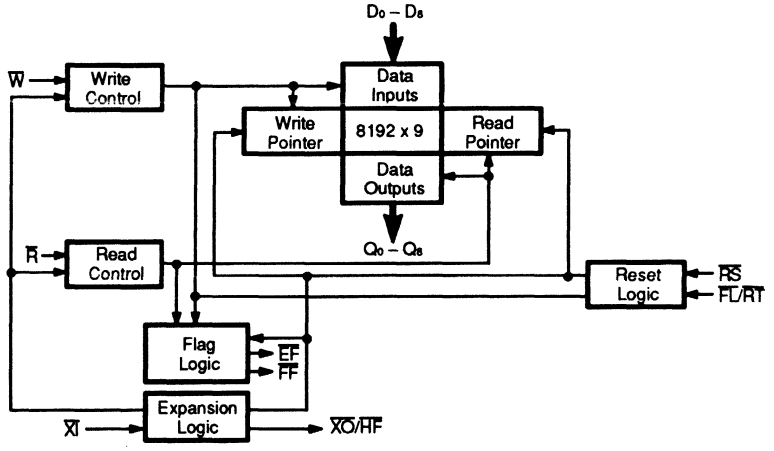
GENERAL DESCRIPTION

The Am7205A is a RAM-based CMOS FIFO that is 8192 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can input and output data asynchronously and simultaneously at data rates from 0 to 40 MHz. Status flags are provided to signify empty, full and half-full conditions. The capability also exists to retransmit data from the FIFO.

High-density FIFOs such as the Am7205A are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the Am7205A useful in communication, image processing, mass storage, DSP, and printing systems.

BLOCK DIAGRAM



14430-001A

Figure 1.

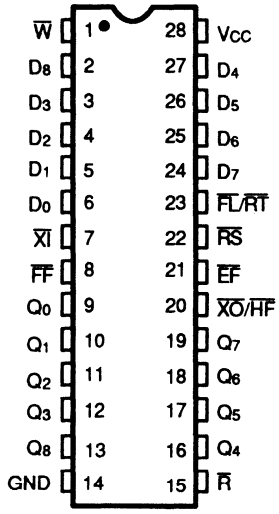
PRODUCT SELECTOR GUIDE

Part Number	Am7205A-15	Am7205A-25	Am7205A-35
Access Time	15 ns	25 ns	35 ns
Maximum Power Supply Current	100 mA	90 mA	80 mA
Operating Frequency	40 MHz	28.5 MHz	22.2 MHz
Operating Range	Com'l	Com'l	Com'l

Publication# 14191 Rev. B Amendment/0
Issue Date: March 1991

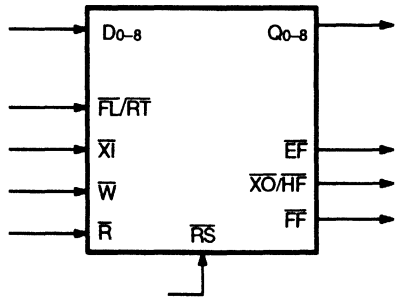
CONNECTION DIAGRAM
Top View

Plastic DIP



14430-002A

LOGIC SYMBOL

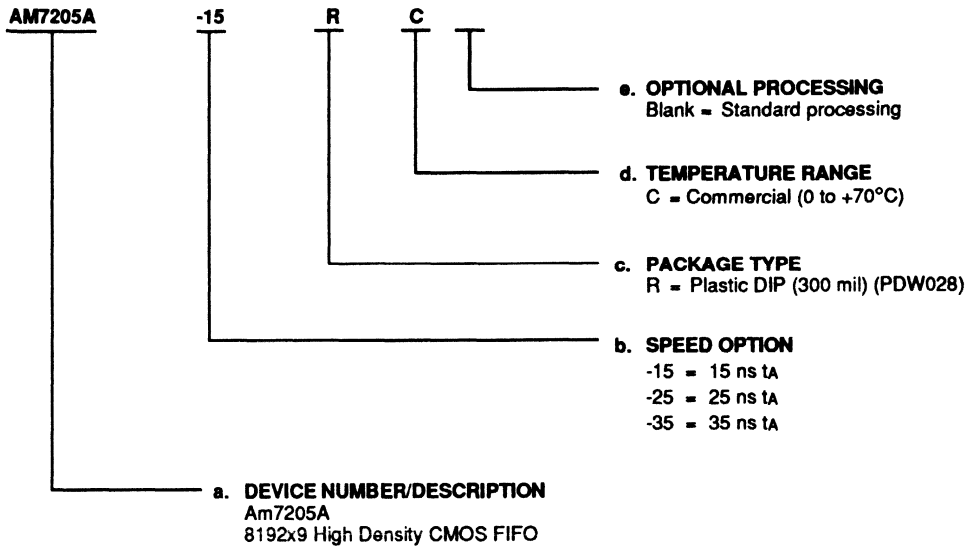


14430-004A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7205A-15	RC
AM7205A-25	
AM7205A-35	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

PIN DESCRIPTION

D_{0-8}

Data In (Inputs (9))

These nine pins are the data inputs to the FIFO.

$\overline{EF}$

$\overline{\text{Empty Flag}}$ (Output; Active LOW)

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO contains data to be read. The $\overline{EF}$ goes LOW when the read pointer is equal to the write pointer, indicating that the device is empty. $\overline{EF}$ LOW inhibits further Read operations.

The $\overline{EF}$ goes HIGH after the rising edge of Write ($\overline{W}$) during the first write cycle for an empty FIFO (See Figure 4). The $\overline{EF}$ goes LOW after the falling edge of Read ($\overline{R}$) during the read cycle which creates the empty condition.

During a Reset cycle, the $\overline{EF}$ is driven LOW (active).

$\overline{FF}$

$\overline{\text{Full Flag}}$ (Output; Active LOW)

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The $\overline{FF}$ goes LOW when the write pointer is one location less than the read pointer, indicating that the device is full. $\overline{FF}$ LOW inhibits further Write operations.

The $\overline{FF}$ goes HIGH after the rising edge of Read ($\overline{R}$) during the first read cycle following a full condition (See Figure 6). The $\overline{FF}$ goes LOW after the falling edge of Write ($\overline{W}$) during the write cycle which creates the full condition.

During a Reset cycle, the $\overline{FF}$ is driven HIGH (inactive).

$\overline{FL}/\overline{RT}$

$\overline{\text{First Load}}/\overline{\text{Retransmit}}$ (Input; Active LOW)

This is a dual purpose input, dependent upon whether the FIFO is in Single Device Mode or Depth-Expansion Mode.

This pin acts as a FIRST LOAD ($\overline{FL}$) pin when in the Depth-Expansion Mode. The device receiving data first will have the $\overline{FL}$ input tied LOW, while the remaining devices will have the $\overline{FL}$ pin tied HIGH. The states of the $\overline{FL}$ and Expansion In ($\overline{XI}$) pins are used to determine the FIFO's mode of operation, as shown in Tables 1 and 2.

This pin is used as the Retransmit ($\overline{RT}$) input during Single Device Mode. The device can be instructed to retransmit the previously written data when $\overline{RT}$ is pulsed LOW.

GND

Power Supply, Ground

This pin is the 0 V power supply for the FIFO.

NC

No Connect

These pins are not connected.

Q_{0-8}

Data Out (Outputs (9), Three State)

These nine pins are the data outputs for the FIFO. These pins are in a high impedance state whenever Read ($\overline{R}$) is HIGH.

$\overline{R}$

$\overline{\text{Read}}$ (Input; Active LOW)

The falling edge of Read ($\overline{R}$) initiates a read cycle, except when the device is empty, as indicated by the Empty Flag ($\overline{EF}$) being LOW. Valid data appears on the outputs (Q_{0-8}) after the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the Data Outputs (Q_{0-8}) will return to a high impedance condition.

$\overline{RS}$

$\overline{\text{Reset}}$ (Input; Active LOW)

The falling edge of Reset ($\overline{RS}$) is used to reset the FIFO. During Reset, both the read and write pointers are set to the first location in the FIFO. Since the reset cycle initializes the FIFO to an empty condition, the Empty Flag ($\overline{EF}$) is driven LOW (active), and both the Half-Full Flag ($\overline{HF}$) and Full Flag ($\overline{FF}$) are driven HIGH (inactive).

V_{cc}

Power Supply

This pin is the +5 V power supply for the FIFO.

$\overline{W}$

$\overline{\text{Write}}$ (Input; Active LOW)

The falling edge of Write ($\overline{W}$) initiates a write cycle, except when the device is full, as indicated by the Full Flag ($\overline{FF}$) being LOW. Data is latched into the FIFO on the rising edge of $\overline{W}$.

$\overline{XI}$

$\overline{\text{Expansion In}}$ (Input; Active LOW)

Expansion In ($\overline{XI}$) is grounded to indicate operation in the Single Device or Width-Expansion Modes. In Depth Expansion Mode, the $\overline{XI}$ pin is connected to the Expansion Out ($\overline{XO}$) pin of the previous device, except for the $\overline{XI}$ pin of the first device which is connected to the $\overline{XO}$ pin of the last FIFO.

This pin operates at CMOS logic levels, thus providing improved noise immunity between cascaded devices.

$\overline{XO}/\overline{HF}$

$\overline{\text{Expansion Out}}/\overline{\text{Half-Full Flag}}$ (Output; Active LOW)

This is a dual purpose output, dependent upon whether the device is in Single Device Mode or Depth Expansion Mode.

This pin operates as an Expansion Out ($\overline{XO}$) signal during Depth Expansion Mode. In this mode, the $\overline{XO}$ pin is connected to the Expansion Input ($\overline{XI}$) pin of the following device, except for the $\overline{XO}$ pin of the last device which is connected to the $\overline{XI}$ pin of the first device.

When in Single Device Mode (Expansion In ($\overline{XI}$) pin grounded) this output operates as a Half-Full Flag ($\overline{HF}$). After half the FIFO has been filled, the $\overline{HF}$ will be set LOW at the falling edge of the next Write ($\overline{W}$) operation. The $\overline{HF}$ will remain LOW until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the FIFO. The $\overline{HF}$ will go HIGH after the rising edge of $\overline{R}$ during the read operation which eliminates the half-full condition (See Figure 5).

During a Reset cycle, the $\overline{HF}$ is driven HIGH (inactive).

This pin operates at CMOS logic levels, thus providing improved noise immunity between cascaded devices.

FUNCTIONAL DESCRIPTION

The Am7205A CMOS FIFO is designed around a 8192x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 8191. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the Am7205A. The write, read, data-in and data-out lines of the Am7205A are connected in parallel, and the Expansion-Out ($\overline{XO}$) and the Expansion-In ($\overline{XI}$) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between $\overline{XO}$ and $\overline{XI}$.

Operational Description

Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of $\overline{XI}$ and $\overline{FL}$ are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ($\overline{R}$) and Write ($\overline{W}$) signals must be HIGH t_{RSS} prior to and t_{RSR} after the rising edge of Reset ($\overline{RS}$). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ($\overline{EF}$) being LOW, active, and both the Half-Full ($\overline{HF}$) and Full Flag ($\overline{FF}$) being HIGH, inactive.

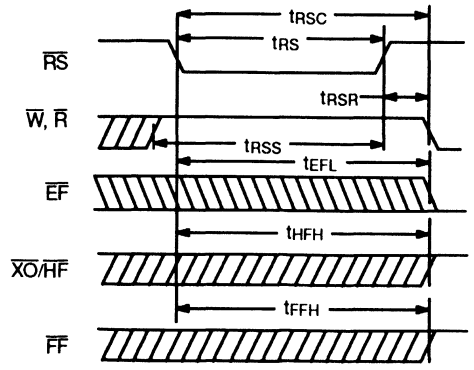


Figure 2. Reset Timing 14430-005A

Writing Data To The FIFO

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The falling edge of Write ($\overline{W}$) initiates a write cycle. (See Figure 3.) Data appearing at inputs D_0–D_8 t_{DS} prior to and t_{DH} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The LOW-to-HIGH transition of the Empty Flag ($\overline{EF}$) occurs t_{WEF} after the rising edge of $\overline{W}$ during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag ($\overline{HF}$) will go LOW t_{WHF} after the falling edge of $\overline{W}$ during the write operation which creates the half-full condition. (See Figure 5.) $\overline{HF}$ will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 4097 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ($\overline{FF}$) goes LOW t_{WFF} after the falling edge of $\overline{W}$ during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 8192 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

A special case of write occurs when a write operation is initiated while the part is full. The next read will cause $\overline{FF}$ to go inactive, and data can then be latched into the FIFO T_{WPF} after the rising edge of $\overline{FF}$ (see Figure 9).

Reading Data From The FIFO

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO is ready to output data. The falling edge of Read ($\overline{R}$) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q_0–Q_8 t_A after the falling edge of $\overline{R}$, and remains until t_{DV} after the rising edge of $\overline{R}$. Q_0–Q_8 return to a high-impedance state when $\overline{R}$ is inactive, when the FIFO is empty, or when the FIFO is in Depth Expansion Mode but is not active.

The Full Flag ($\overline{FF}$) will go HIGH t_{RFF} after the rising edge of $\overline{R}$ during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag ($\overline{HF}$) will go HIGH t_{RHF} after the rising edge of $\overline{R}$ during the read operation, which eliminates the half-full condition. (See Figure 5). $\overline{HF}$ will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 4096 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of $\overline{EF}$ occurs t_{REF} after the falling edge of $\overline{R}$ during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

A special case of read occurs when a read operation is initiated while the part is empty. The data latched in by the next write will be accessed t_A ns after the rising edge of $\overline{EF}$. Read is held active, and cannot be deasserted until T_{RPE} after the rising edge of $\overline{EF}$ (see Figure 8).

Table 1. Reset and Retransmit Truth Table
(Single-Device Configuration/Width-Expansion Mode)

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

Notes:

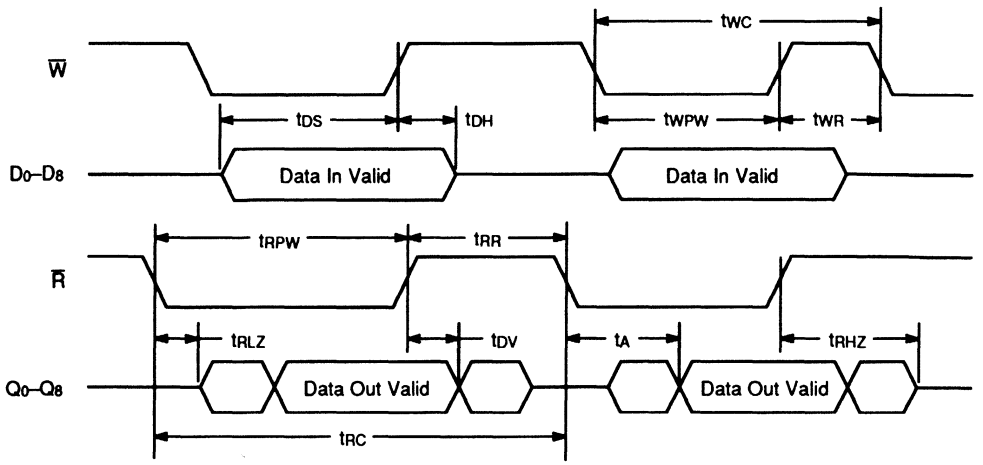
1. Flags will change to show correct state according to write pointer.
2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2. Reset and First Load Truth Table
(Depth-Expansion/Compound-Expansion Mode)

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-first device	0	0	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	$\overline{XO}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

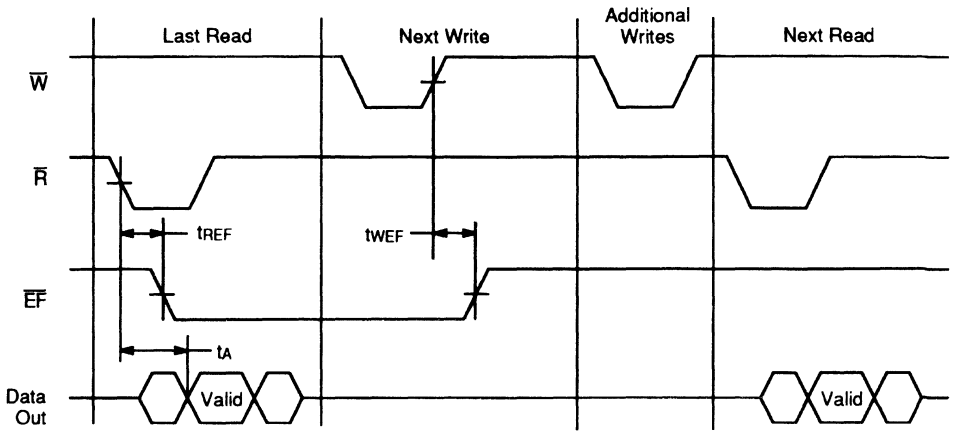
Notes:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
2. Same as during Reset Cycle.
3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.



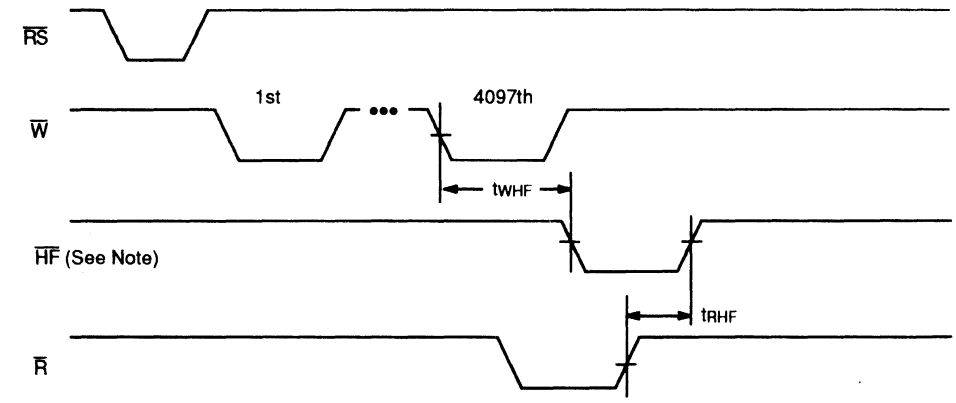
14430-006A

Figure 3. Asynchronous Write and Read Timing



14430-007A

Figure 4. Empty Flag Timing

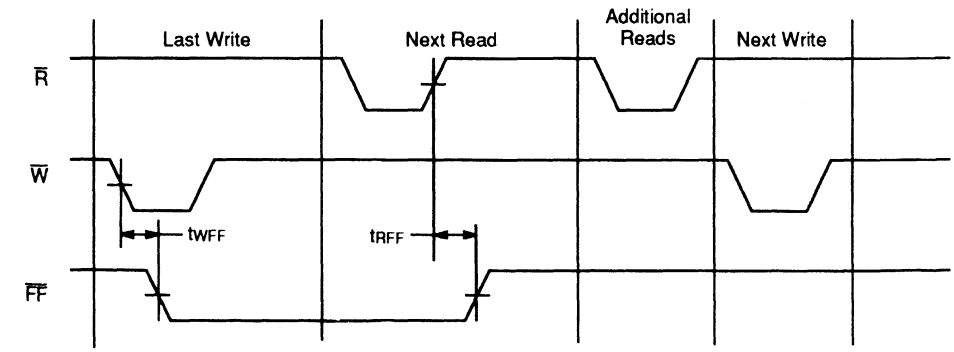


Note:

Depending on the precise phase of $\overline{W}$ and $\overline{R}$, the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when $\overline{W}$ and $\overline{R}$ are operating asynchronously near half full.

14430-008A

Figure 5. Half-Full Flag Timing



14430-009A

Figure 6. Full Flag Timing

Half-Full Flag

The Half-Full ($\overline{HF}$) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 4097 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 4097 words, and Read and Write pulses are applied simultaneously, the $\overline{HF}$ flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$ will always settle to the correct state after the appropriate delay, t_{WHF} or t_{RHF}. This property of the Half-Full Flag is clearly a function of the dynamic relation between $\overline{W}$ and $\overline{R}$. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 8192 or less writes between reset cycles.

The $\overline{FL}/\overline{RT}$ is used as the Retransmit ($\overline{RT}$) input in Single-Device Mode. The retransmit capability is intended for use when there are 8192 or less writes between reset cycles. $\overline{RT}$, an active LOW-going pulse of at least t_{RT} in duration, initializes the internal read pointer to address zero and leaves the write pointer unaffected. $\overline{R}$ must be HIGH during the retransmit cycle. The first read cycle should not start until t_{RTR} after the rising edge of $\overline{RT}$. The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO t_{RTC} after the falling edge of $\overline{RT}$. (See Figure 7 and Table 1).

Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ($\overline{XI}$) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The Am7205A can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated due to the skew between devices. 2) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one device's flags are used as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time (t_{WEF}, t_{WHF}, t_{WFF}, t_{REF}, t_{RHF}, and t_{RFF}) for each flag has elapsed.

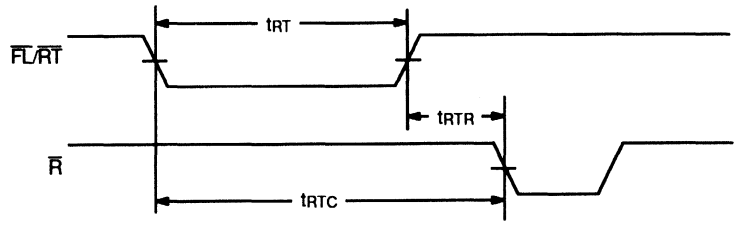
Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ($\overline{XO}$) of one device must be connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device being connected to $\overline{XI}$ of the first device. The device that is to receive data first has its First Load ($\overline{FL}$) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using $\overline{XO}$ and $\overline{XI}$. A LOW-going pulse on $\overline{XO}$ occurs when the last physical location of an active device, address 8192, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the $\overline{FF}$ outputs together. Likewise, a composite Empty Flag is created by OR-ing all the $\overline{EF}$ outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

Compound Expansion

FIFOs of greater width and depth than the Am7205A can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)

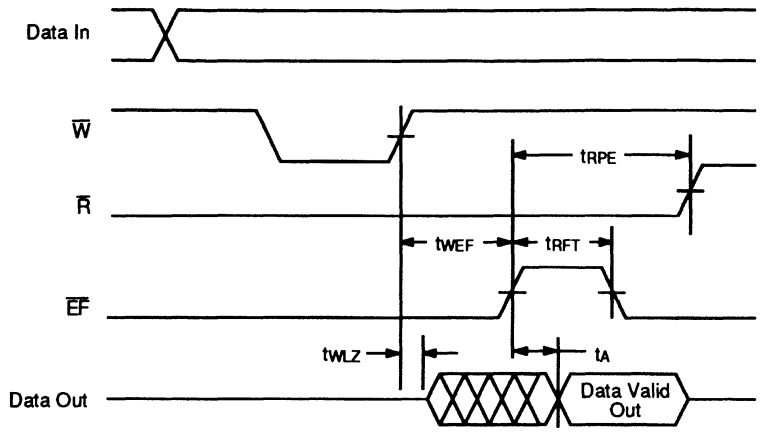


14430-010A

Note:

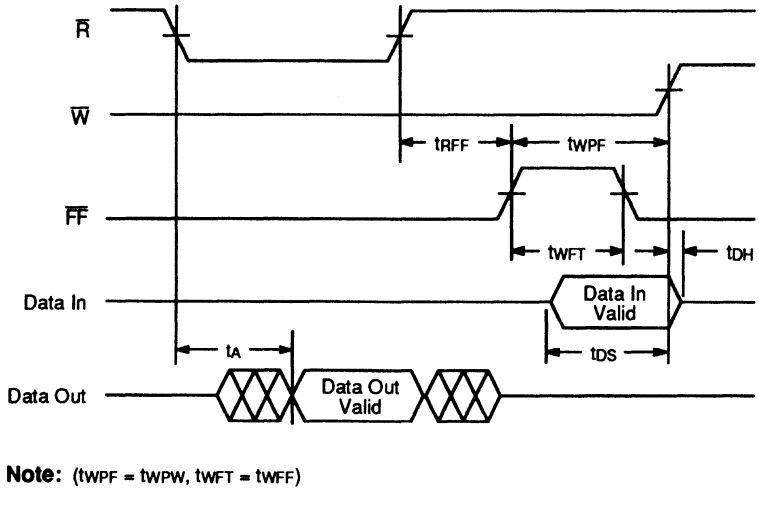
$\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at t_{RTC}.

Figure 7. Retransmit Timing



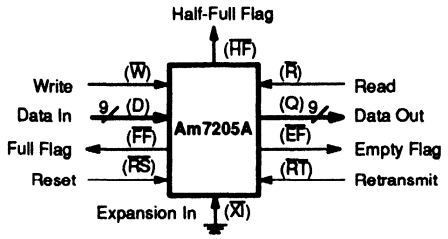
Note: ($t_{RPE} = t_{RPW}$, $t_{RFT} = t_{REF}$)

Figure 8. Read Data Flow-Through Mode



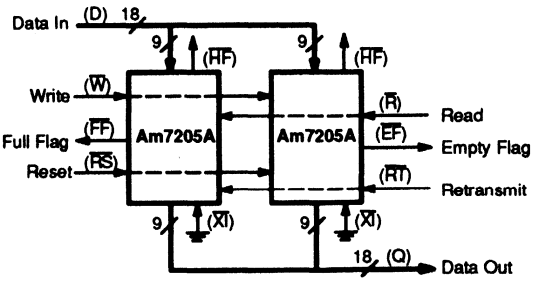
Note: ($t_{WPF} = t_{WPW}$, $t_{WFT} = t_{WFF}$)

Figure 9. Write Data Flow-Through Mode



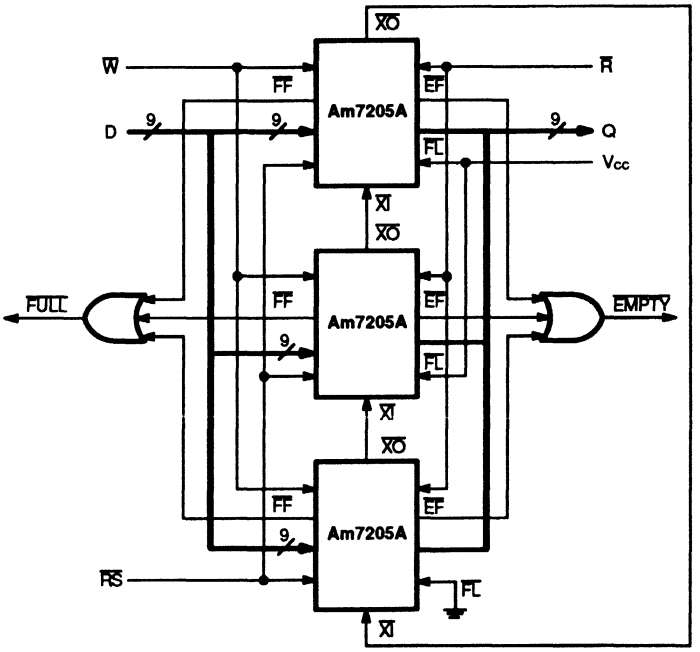
14430-013A

Figure 10. Single FIFO Configuration



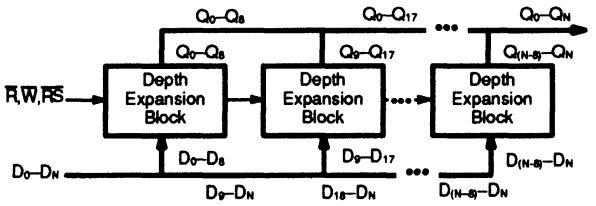
14430-014A

Figure 11. Width-Expansion to Form a 8192x18 FIFO



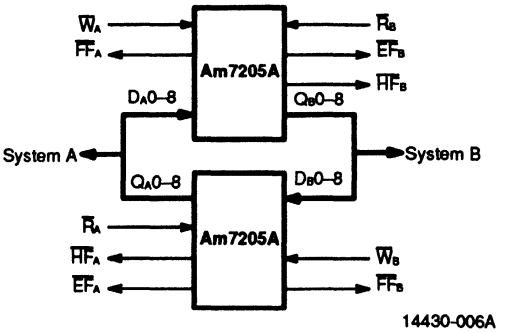
14430-015A

Figure 12. Depth-Expansion to Form 24,576x9 FIFO



14191-016A

Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques



14430-006A

Figure 14. Bidirectional FIFO Configuration

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.5V to +7.0 V
Input Voltage	−0.5V to V_{CC} +0.5 V
Ambient Temperature with Power Applied	−55°C to +125°C
Storage Temperature	−55°C to +150°C
Power Dissipation	1.0 W
DC Output Current	50 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0°C to 70°C
Supply Voltage, (V_{CC})	+4.5V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Am7205A-15 t_A = 15 ns		Am7205A-25 t_A = 25 ns		Am7205A-35 t_A = 35 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
I_{IL}	Input Leakage Current (any input) (Note 1)	−1	1	−1	1	−1	1	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	−10	10	−10	10	−10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	—	0.8	—	0.8	—	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	—	3.5	—	3.5	—	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	—	1.5	—	1.5	—	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = −2 mA	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8 mA	—	0.4	—	0.4	—	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	—	100	—	90	—	80	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}) (Note 4)	—	15	—	15	—	15	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} −0.2 V) (Note 4)	—	2	—	2	—	2	mA

Notes:

1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified.

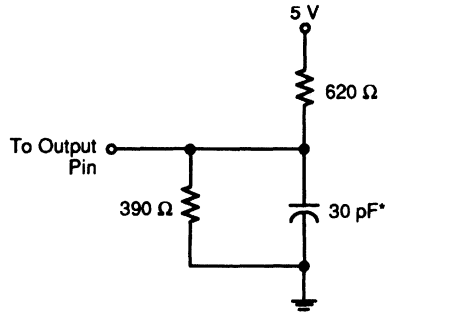
Parameter Symbol	Parameter Description	Figures	Am7205A-15		Am7205A-25		Am7205A-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write and Flag Timing									
t_{WC}	Write Cycle Time	3	25	—	35	—	45	—	ns
t_{WPW}	Write Pulse Width	3	15	—	25	—	35	—	ns
t_{WR}	Write Recovery Time	3	10	—	10	—	10	—	ns
t_{DS}	Data Setup Time	3,9	12	—	15	—	18	—	ns
t_{DH}	Data Hold Time	3,9	0	—	0	—	0	—	ns
t_{WFF}	Write LOW to Full Flag LOW	6,9	—	22	—	25	—	30	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5	—	30	—	35	—	45	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8	—	22	—	25	—	30	ns
t_{WLZ}	Write Pulse HIGH to Data Bus at LOW Z (Note 1)	8	5	—	5	—	10	—	ns
Read and Flag Timing									
t_{RC}	Read Cycle Time	3	25	—	35	—	45	—	ns
t_A	Access Time	3,4,8,9	—	15	—	25	—	35	ns
t_{RR}	Read Recovery Time	3	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width	3	15	—	25	—	35	—	ns
t_{RLZ}	Read Pulse LOW to Data Bus at LOW Z (Note 1)	3	5	—	5	—	5	—	ns
t_{DV}	Data Valid from Read Pulse HIGH	3	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse HIGH to Data Bus at HIGH Z (Note 1)	3	—	15	—	18	—	20	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9	—	22	—	25	—	30	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	5	—	30	—	35	—	45	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8	—	22	—	25	—	30	ns
Reset Timing									
t_{RSC}	Reset Cycle Time	2	25	—	35	—	45	—	ns
t_{RS}	Reset Pulse Width	2	15	—	25	—	35	—	ns
t_{RSS}	Reset Setup Time	2	15	—	25	—	35	—	ns
t_{RSR}	Reset Recovery Time	2	10	—	10	—	10	—	ns
t_{EFL}	Reset to Empty Flag LOW	2	—	25	—	35	—	45	ns
t_{HFH}	Reset to Half-Full Flag High	2	—	25	—	35	—	45	ns
t_{FFH}	Reset to Full Flag HIGH	2	—	25	—	35	—	45	ns
Retransmit Timing									
t_{RTC}	Retransmit Cycle Time	7	40	—	45	—	55	—	ns
t_{RT}	Retransmit Pulse Width	7	20	—	25	—	35	—	ns
t_{RTR}	Retransmit Recovery Time	7	20	—	20	—	20	—	ns

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See Figure 15



* Includes jig and scope capacitances.

Figure 15. AC Test Load

CAPACITANCE (V_{CC} = 5.0 V, T_A = +25°C, f = 1.0 MHz)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V	5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	7	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

67C401/13 67C402/23

First-In First-Out (FIFO)
64 x 4, 64 x 5 CMOS MEMORY (Cascadable)

Advanced Micro Devices

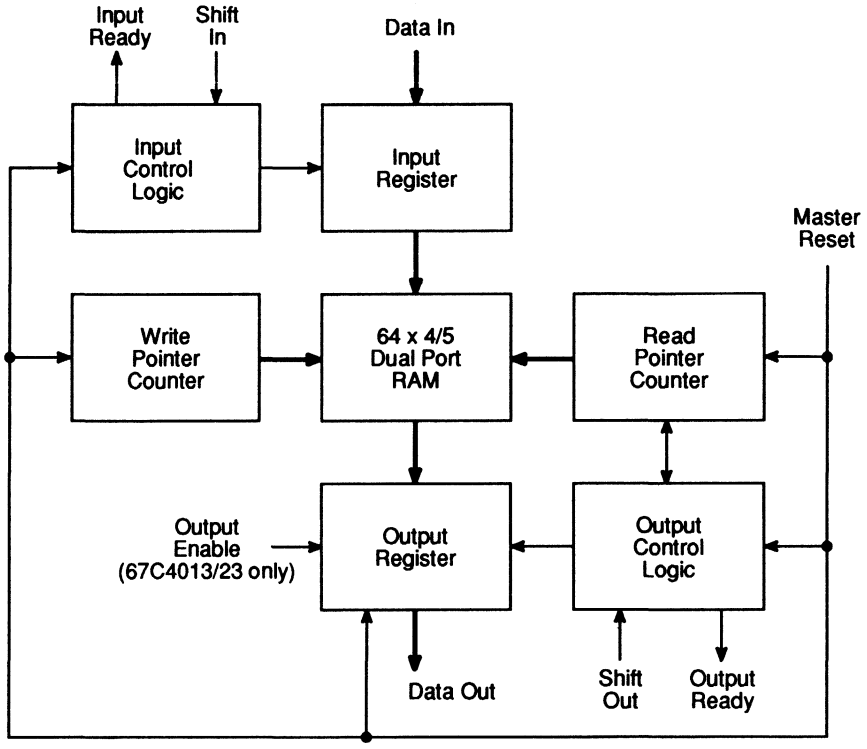
DISTINCTIVE CHARACTERISTICS

- Zero standby power
- High-speed 35-MHz shift-in/shift-out rates
- Very low active power consumption
- TTL-compatible inputs and outputs
- Readily expandable in word width and depth
- RAM-based architecture for short fall-through delay
- Full CMOS cell for maximum noise immunity
- Asynchronous operation
- Output Enable feature (67C4013/23)

GENERAL DESCRIPTION

The 67C40X/XX series devices are high-performance CMOS RAM-based First-In First-Out (FIFO) buffer memory products organized as 64 words by 4 or by 5, bits wide. These devices use Advanced Micro Devices latest CMOS process technology and meet the demands for high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, thus improving overall system performance. By using both Read and Write pointers for addressing each memory location, the data can propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well for high-speed disc controllers, graphics, and communication network systems. The 550-µwatt standby power specification makes these devices ideal for ultra-low power and battery-powered systems.

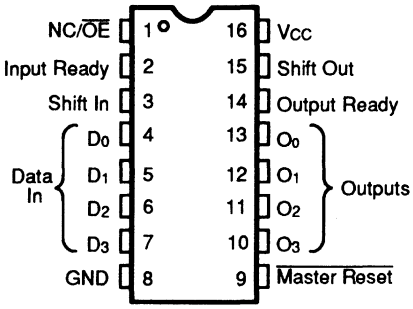
BLOCK DIAGRAM



Publication# 10998 Rev. C Amendment/0
Issue Date: March 1991

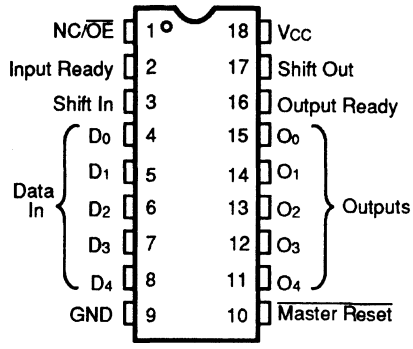
CONNECTION DIAGRAMS

67C401/13



DIP

67C402/23



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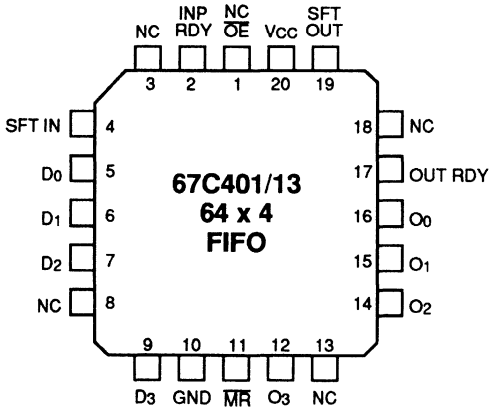
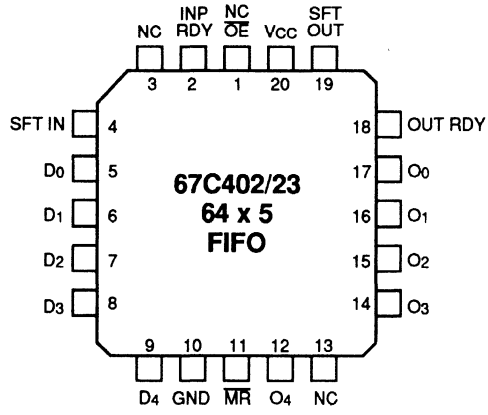


Plastic Leaded Chip Carrier

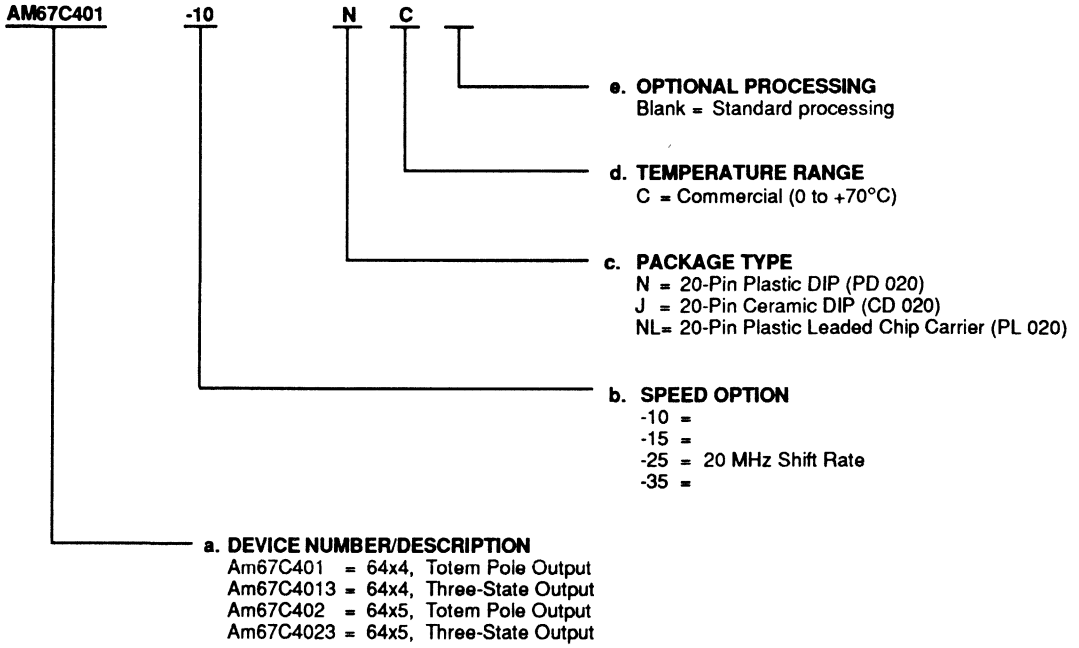


Plastic Leaded Chip Carrier

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM67C401-10	N, J, NL
AM67C401-15	
AM67C4013-10	
AM67C4013-15	
AM67C402-10	
AM67C402-15	
AM67C4023-10	
AM67C4023-15	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

* Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	−0.5 V to +7.0 V
Input Voltage	−1.5 V to +7.0 V
Off-state Output Voltage	−0.5 to V_{CC} +0.5 V
Storage Temperature	−65°C to +150°C
Power Dissipation	1.0 W

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. This is a stress rating only; functional operation of the device at these limits or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) With Respect to Ground	+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

OPERATING CONDITIONS Commercial: V_{CC} = 5 V ±10%, T_A = 0°C to +70°C

Parameter Symbol	Parameter Description	Figure	-10 Min.	-10 Max.	-15 Min.	-15 Max.	-25 Min.	-25 Max.	-35 Min.	-35 Max.	Unit
f_{IN}	Shift in rate	1		10		15		25		35	MHz
t_{SIH}*	Shift in HIGH time	1	14		14		8		8		ns
t_{SIL}*	Shift in LOW time	1	25		25		8		8		ns
t_{IDS}	Input data setup to SI (Shift In)	1	0		0		0		0		ns
t_{IDH}	Input data hold time from SI (Shift In)	1	40		40		20		15		ns
t_{RIDS}	Input data setup to IR (Input Ready)	3	0		0		5		2		ns
t_{RIDH}	Input data hold time from IR (Input Ready)	3	30		30		20		15		ns
f_{OUT}	Shift out rate	4		10		15		25		35	MHz
t_{SOH}*	Shift out HIGH time	4	24		21		8		8		ns
t_{SOL}*	Shift out LOW time	4	25		25		8		8		ns
t_{MRW}	Master Reset pulse	8	35		35		25		18		ns
t_{MRS}	Master Reset to SI	8	65		65		10		7		ns

*See AC test and high-speed application note.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Condition		-10 Min.	-10 Max.	-15 Min.	-15 Max.	-25 Min.	-25 Max.	-35 Min.	-35 Max.	Unit
V_{IL}*	Low-level input voltage				0.8		0.8		0.8		0.8	V
V_{IH}*	High-level input voltage			2		2		2		2		V
I_{IN}	Input Current	V_{CC} = Max., GND <V_{IN} <V_{CC}		−1	1	−1	1	−1	1	−1	1	µA
I_{OZ}	Off-state output current	V_{CC} = Max., GND <V_{OUT} <V_{CC}		−5	5	−5	5	−5	5	−5	5	µA
V_{OL}	Low-level output voltage	V_{CC} = Min.	I_{OL} = 20 µA		0.1		0.1		0.1		0.1	V
			I_{OL} = 8 mA		0.4		0.4		0.4		0.4	
V_{OH}	High-level output voltage	V_{CC} = Min.	I_{OH} = −20 µA	V_{CC} − 0.1		V_{CC} − 0.1		V_{CC} − 0.1		V_{CC} − 0.1		V
			I_{OH} = −4 mA	2.4		2.4		2.4		2.4		
I_{OS}**	Output short-circuit current	V_{CC} = Max.	V_O = 0 V	−90	−20	−90	−20	−90	−20	−90	−20	mA
I_{CC}	Standby supply current	V_{CC} = Max. I_{OUT} = 0	V_{IH} = V_{CC} V_{IL} = GND		100		100		100		100	µA
	Operating supply current		V_{IH} = Min., V_{IL} = Max. f_{IN} = f_{OUT} = Max.		35		45		50		60	mA

*These are absolute voltages with respect to GND and include all overshoots due to system and/or tester noise.
**Not more than one output should be shortened at a time, and duration of the short circuit should not exceed one second.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Figure	-10 Min.	-10 Max.	-15 Min.	-15 Max.	-25 Min.	-25 Max.	-35 Min.	-35 Max.	Unit
t_{IRL}*	Shift in ↑ to Input Ready Low	1		60		55		21		18	ns
t_{IRH}*	Shift in ↓ to Input Ready HIGH			50		50		28		20	ns
t_{ORL}*	Shift Out ↑ to Output Ready LOW	4		55		45		19		18	ns
t_{ORH}*	Shift Out ↓ to Output Ready HIGH			50		41		34		20	ns
t_{ODH}	Output Data Hold (previous word)		5		5		5		5		ns
t_{ODS}	Output Data Shift (next word)			35		30		34		20	ns
t_{PT}	Data throughput	3,6		100		90		40		34	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8		100		100		35		28	ns
t_{MRIRH}	Master Reset ↓ to Input Ready HIGH			100		100		35		28	ns
t_{MRO}	Master Reset ↓ to Outputs LOW			35		35		25		22	ns
t_{IPH}	Input Ready pulse HIGH	3	19		16		8		8		ns
t_{OPH}	Output Ready pulse HIGH	6	14		14		8		8		ns
t_{ORD}	Output Ready ↑ to Data Valid	4		−3		−3		0		0	ns
t_{PHZ}**	Output Disable Delay	A		25		25		15		12	ns
t_{PLZ}**				25		25		15		12	
t_{PZL}**	Output Enable Delay			30		30		20		15	ns
t_{PZH}**				30		30		20		15	

*See AC test and high-speed application note.
**Enable/Disable delays refer to 67C4013/23 only.

CAPACITANCES*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 4.5 V		10	pF
C_{OUT}	Output capacitance			7	

*Not tested in production.

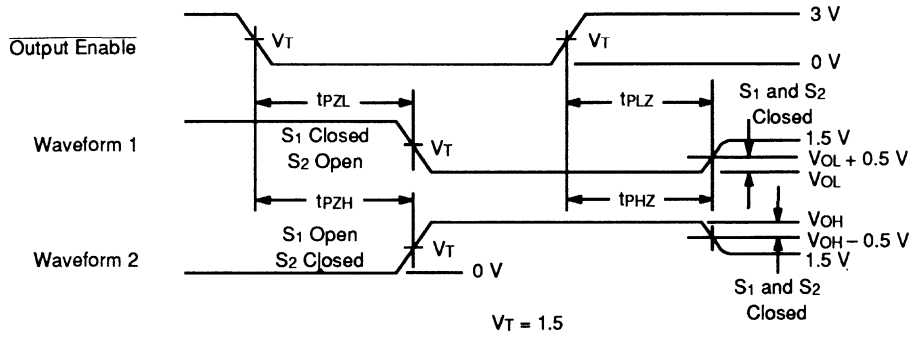
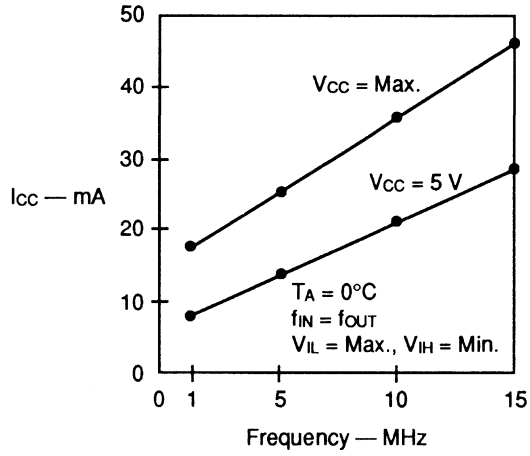


Figure A. Enable and Disable

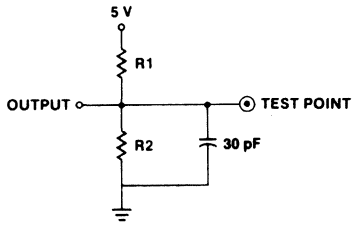
Notes:

1. Waveform 1 is for a data output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for a data output with internal conditions such that the output is high except when disabled by the output control.

ICC vs. Frequency



STANDARD AC TEST LOAD

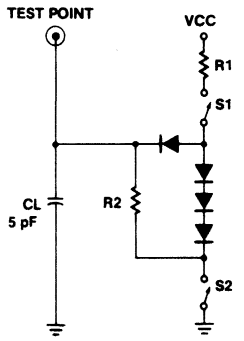


Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V
All Diodes are 1N916 or 1N3064

RESISTOR VALUES

I_{OL}	R1	R2
8 mA	600 Ω	1200 Ω

THREE-STATE TEST LOAD



FUNCTIONAL DESCRIPTION

Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally resets both the read and write counters. When the Input Ready (IR) is HIGH, the FIFO is ready to accept DATA from the D_X inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then the IR will remain LOW.

Data Output

Data is read from the O_X outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e., data does not change if the FIFO is empty). A dual-port RAM inside the chip provides the capability of simultaneous and asynchronous writes (Shift-Ins) and reads (Shift-Outs).

AC TEST AND HIGH-SPEED APP. NOTES

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Advanced Micro Devices recommends a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading; i.e., a rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not HIGH due to (a) too high a frequency, or (b) FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going HIGH. This same type of problem also relates to t_{IRH}, t_{ORL}, and t_{ORH}. For high-speed applications, proper grounding technique is essential. In order to diminish timing ambiguities between the Shift-In-Input-Ready or Shift-Out-Output-Ready pairs when operating at high frequencies, it is recommended that the t_{SIH} and t_{SOH} pulse widths be as short as possible within the specified limits.

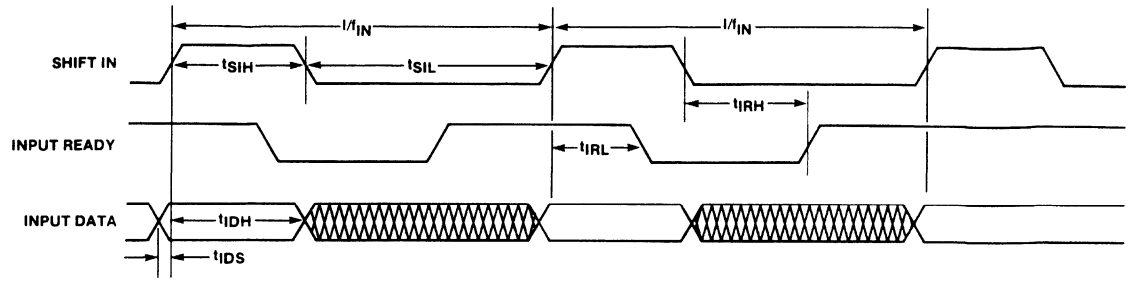


Figure 1. Input Timing

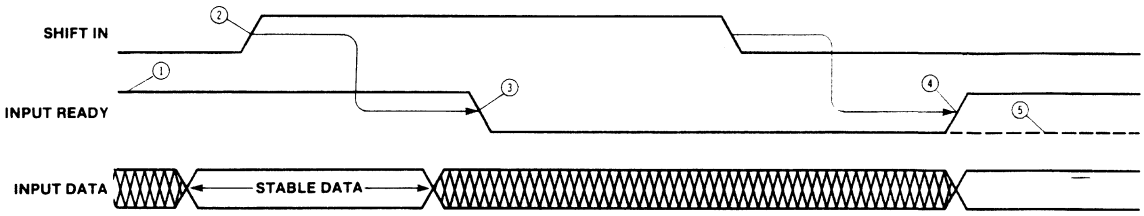


Figure 2. The Mechanism of Shifting Data into the FIFO

① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
② Input Data is loaded into the first available memory location.
③ Input Ready goes LOW indicating this memory location is full.
④ Shift-In going LOW allows Input Ready to sense the status of the next memory location. The next memory location is empty as indicated by Input Ready HIGH.
⑤ If the FIFO is already full then the Input Ready remains LOW.
Note: Shift-In pulses applied while Input Ready is LOW will be ignored.

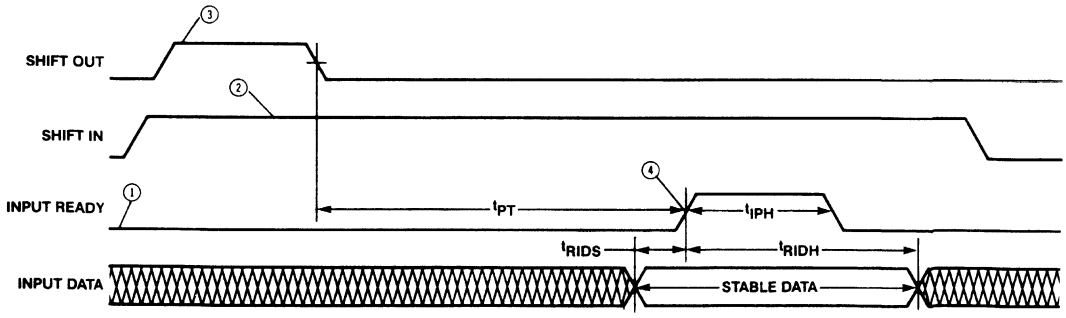


Figure 3. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.
② Shift In is held HIGH.
③ Shift Out pulse is applied. An empty location is detected by the internal pointers on the falling edge of SO.
④ As soon as Input Ready becomes HIGH the Input Data is loaded into this location.

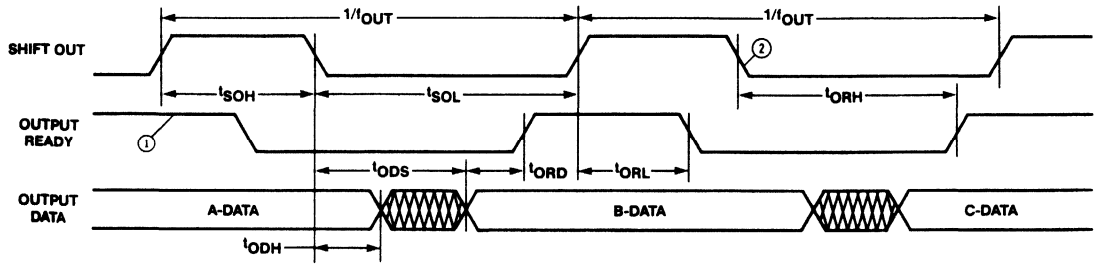


Figure 4. Output Timing

① The diagram assumes that the FIFO contains at least three words: A-Data (first input word), B-Data (second input word), and C-Data (third input word).
② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

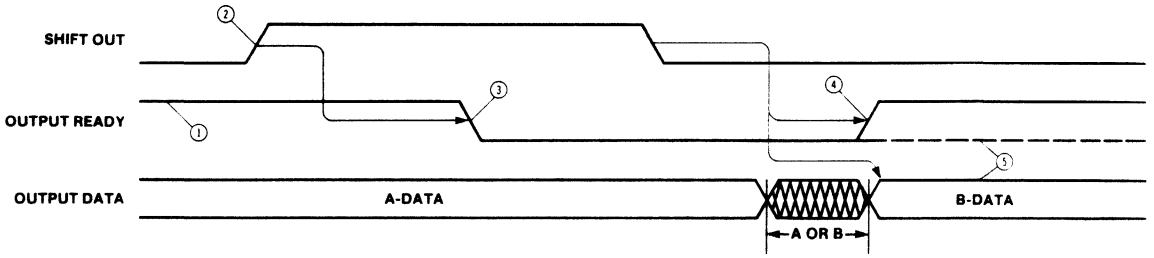


Figure 5. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
② Shift-Out goes HIGH causing B-Data (second input word) to advance to the output register. Output data remains as valid A-Data while Shift-Out is HIGH.
③ Output Ready goes LOW.
④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data remains the same (A-Data).

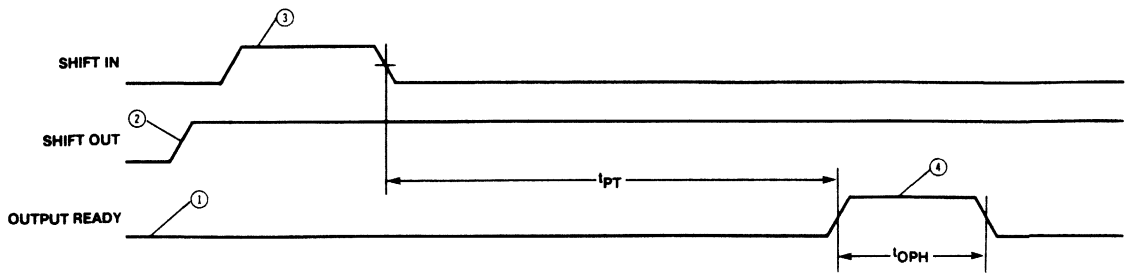


Figure 6. t_{PT} and t_{OPH} Specification

① FIFO initially empty.
② Shift-Out held HIGH.
③ Shift-In pulse applied. A full location is detected by the internal pointers on the falling edge of Shift-In.
④ As soon as Output Ready becomes HIGH, the word is shifted out.

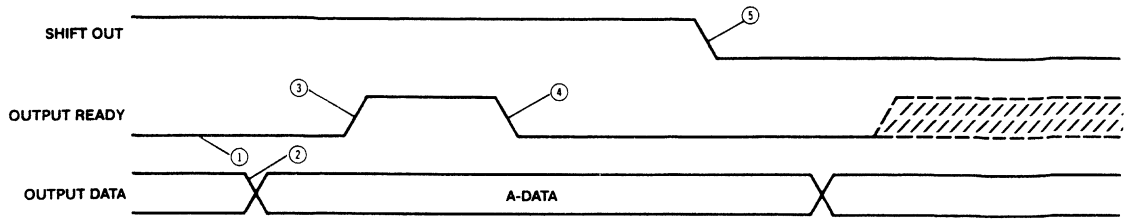
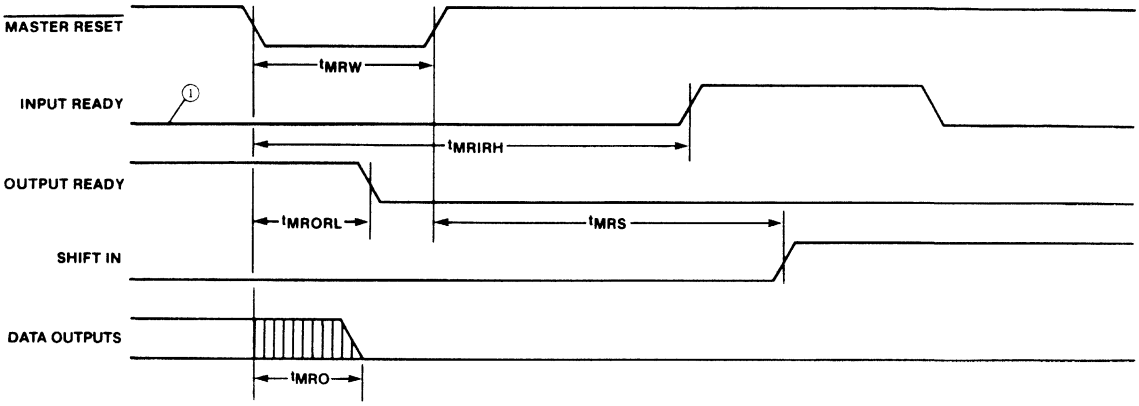


Figure 7. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

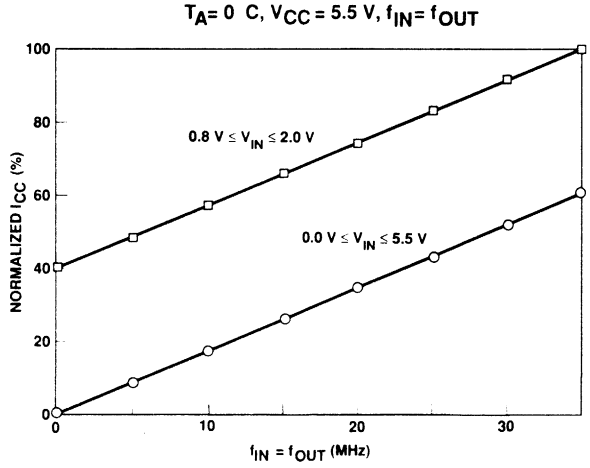
① The internal logic does not detect the presence of any words in the FIFO.
② New data (A) arrives at the outputs.
③ Output Ready goes HIGH indicating arrival of the new data.
④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or remain LOW depending on whether there are any additional words in the FIFO.



① FIFO is initially full

Figure 8. Master Reset Timing

NORMALIZED I_{CC} vs FREQUENCY



67C4033

First-In First-Out (FIFO)
64x5 Memory 10/15 MHz (Cascadable) CMOS

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Zero standby power**
- **High-speed 15-MHz shift-in/shift-out rates**
- **Very low active power consumption**
- **TTL-compatible inputs and outputs**
- **Readily expandable in word width and depth**
- **Half-Full and Almost-Full/Empty status flags**
- **RAM-based architecture for short fall-through delay**
- **Full CMOS 8-transistor cell for maximum noise immunity**
- **Asynchronous operation**
- **Output enable**

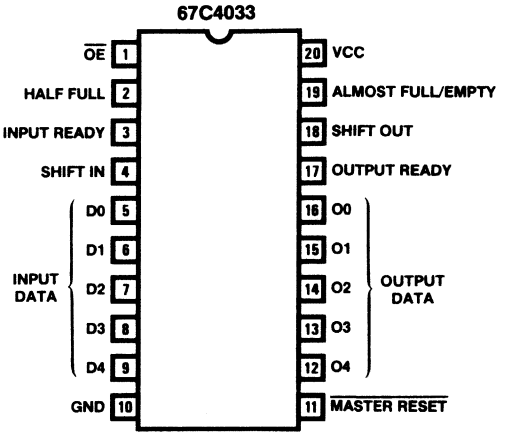
GENERAL DESCRIPTION

The 67C4033 device is a high-performance CMOS RAM-based First-In First-Out (FIFO) buffer product organized as 64 words by 5 bits wide. This device uses Monolithic Memories' latest CMOS process technology and meets the demands for high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, thus improving overall system performance. By using Read and Write pointers for addressing each memory location, the data can propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well for high-speed disk controllers, graphics, and communication network systems. The 550 μwatt standby power specification of this device makes it ideal for ultra-low-power and battery-powered systems.

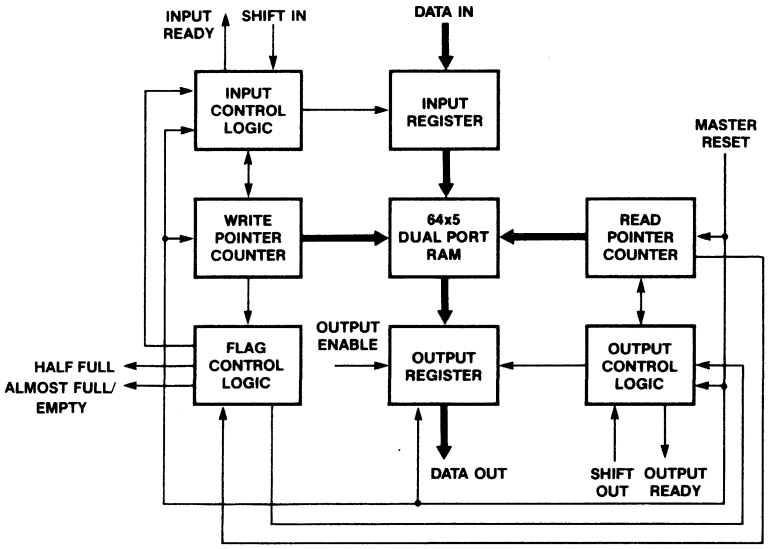
ORDERING INFORMATION

Part Number	Package	Temp	Description
67C4033-10	CD 020, PD 020, PL 020	Com	10 MHz in/out
67C4033-15	CD 020, PD 020, PL 020	Com	15 MHz in/out

CONNECTION DIAGRAMS



BLOCK DIAGRAM



Publication# 10684 Rev. A Amendment/0
Issue Date: January 1989

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to V_{CC} +0.5 V
Storage temperature ..... -65°C to +150°C
Power dissipation ..... 1.0 W
Latch-up trigger current, all outputs ..... 140 mA

OPERATING RANGES Over Temperature Range

SYMBOL	PARAMETER	FIGURE	67C4033-10 MIN	67C4033-10 MAX	67C4033-15 MIN	67C4033-15 MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
T_A	Operating free-air temperature		0	70	0	70	°C
f_{IN}	Shift In rate	1		10		15	MHz
t_{SIH}	Shift in HIGH time	1,B	14		14		ns
t_{SIL}	Shift in LOW time	1	25		25		ns
t_{IDS}	Input data setup to SI (Shift In)	1	0		0		ns
t_{IDH}	Input data hold time from SI (Shift In)	1	40		40		ns
t_{RIDS}	Input data setup to IR (Input Ready)	3	0		0		ns
t_{RIDH}	Input data hold time from IR (Input Ready)	3	30		30		ns
f_{OUT}	Shift Out rate	4		10		15	MHz
t_{SOH}	Shift Out HIGH time	4,B	24		21		ns
t_{SOL}	Shift Out LOW time	4	25		25		ns
t_{MRW}*	Master Reset pulse	8	35		35		ns
t_{MRS}	Master Reset to SI	8	65		65		ns

* See AC test and high-speed application note.

DC CHARACTERISTICS Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		67C4033-10 MIN	67C4033-10 MAX	67C4033-15 MIN	67C4033-15 MAX	UNIT
V_{IL}*	Low-level input voltage				0.8		0.8	V
V_{IH}*	High-level input voltage			2		2		V
I_{IN}	Input current	V_{CC} = MAX	GND<V_{IN}<V_{CC}	-1	1	-1	1	μA
I_{OZ}	Off-state output current	V_{CC} = MAX	GND<V_{OUT}<V_{CC}	-5	5	-5	5	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 20 μA		0.1		0.1	V
			I_{OL} = 8 mA		0.4		0.4	
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = -20 μA	V_{CC} -0.1		V_{CC} -0.1		V
			I_{OH} = -4 mA	2.4		2.4		
I_{OS}**	Output short-circuit current	V_{CC} = MAX	V_O = 0 V	-90	-20	-90	-20	mA
I_{CC}	Standby supply current	V_{CC} = MAX	V_{IH} = V_{CC} V_{IL} = GND		100		100	μA
	Operating supply current	I_{OUT} = 0	V_{IH} = MIN, V_{IL} = MAX f_{IN} = f_{OUT} = MAX		35		45	mA

* These are absolute voltages with respect to GND (Pin 10) and include all overshoots due to system and/or tester noise.

** Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

SWITCHING CHARACTERISTICS Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	67C4033-10 MIN	67C4033-10 MAX	67C4033-15 MIN	67C4033-15 MAX	UNIT
t_{IRL}*	Shift In ↑ to Input Ready LOW	1		60		55	ns
t_{IRH}*	Shift In ↓ to Input Ready HIGH			50		50	ns
t_{ORL}*	Shift Out ↑ to Output Ready LOW	4		55		45	ns
t_{ORH}*	Shift Out ↓ to Output Ready HIGH			50		41	ns
t_{ODH}	Output Data Hold (previous word)		5		5		ns
t_{ODS}	Output Data Shift (next word)			35		30	ns
t_{PT}	Data throughput	3,6		100		90	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8		100		100	ns
t_{MRIRH}	Master Reset ↓ to Input Ready HIGH			100		100	ns
t_{MRO}	Master Reset ↓ to Ouputs LOW			35		35	ns
t_{MRHFL}	Master Reset ↓ to Half-Full Flag LOW	9		100		100	ns
t_{MRAEH}	Master Reset ↓ to Almost Empty Flag HIGH			100		100	ns
t_{IPH}	Input ready pulse HIGH	3,B	19		16		ns
t_{OPH}	Output ready pulse HIGH	6,B	14		14		ns
t_{ORD}	Output ready ↑ to Data Valid	4		-3		-3	ns
t_{AEH}	Shift Out ↑ to AF/E HIGH	10		110		110	ns
t_{AEL}	Shift In ↑ to AF/E LOW			110		110	ns
t_{AFL}	Shift Out ↑ to AF/E LOW	11		110		110	ns
t_{AFH}	Shift In ↑ to AF/E HIGH			110		110	ns
t_{HFH}	Shift In ↑ to HF HIGH	12		110		110	ns
t_{HFL}	Shift Out ↑ to HF LOW			110		110	ns
t_{PHZ}	Output Disable Delay	A		25		25	ns
t_{PLZ}				25		25	
t_{PZL}	Output Enable Delay			30		30	ns
t_{PZH}				30		30	

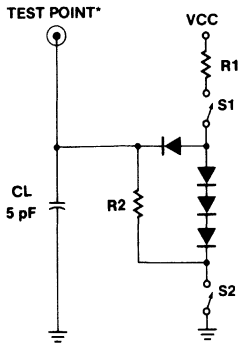
* See timing diagram for explanation of parameters.

CAPACITANCES*

SYMBOL	PARAMETER	TEST CONDITION	67C4033-XX MIN	67C4033-XX MAX	UNIT
C_{IN}	Input capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 4.5 V		10	pF
C_{OUT}	Output capacitance			7	pF

* Values not tested in production.

THREE-STATE TEST LOAD



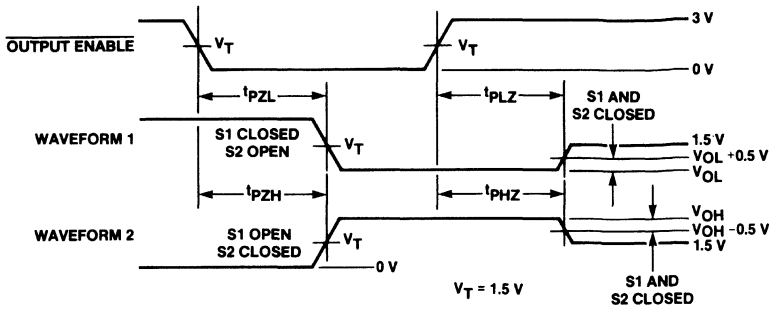
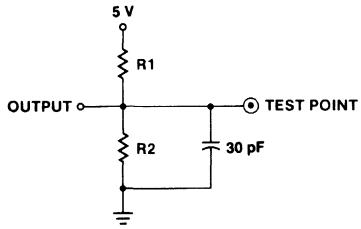


Figure A. Enable and Disable

Waveform 1 is for a data output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for a data output with internal conditions such that the output is high except when disabled by the output control.

STANDARD A.C. TEST LOAD



Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V
All Diodes are 1N916 or 1N3064

RESISTOR VALUES

I_{OL}	R1	R2
8 mA	600 Ω	1200 Ω

FUNCTIONAL DESCRIPTION

Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally resets both the read and write counters. When the Input Ready (IR) is HIGH, the FIFO is ready to accept DATA from the D_X inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then the IR will remain LOW.

Data Output

Data is read from the O_X outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e., data does not change if the FIFO is empty). A dual-port RAM inside the chip provides the capability of simultaneous and asynchronous writes (Shift-Ins) and reads (Shift-Outs).

AC TEST AND HIGH-SPEED APP. NOTES

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading; i.e., rising edge of the Shift-In pulse is not recognized until Input ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-In going HIGH. This same type of problem is also related to T_{IRH}, T_{ORL}, T_{ORH}, and the Status Flag timing as related to Shift-In and Shift-Out. For high-speed applications, proper grounding technique is essential.

HF AND AFE STATUS FLAGS

The Half-Full (HF) will be high only when the net balance of words shifted into the FIFO exceeds the number of words shifted out by thirty-two or more (i.e., when the FIFO contains thirty-two or more words). The Almost-Full/Empty (AFE) flag will be HIGH when the FIFO contains fifty-six or more words or when the FIFO contains eight or fewer words (see Figures 9, 10, and 11).

Care should be exercised in using the status flags because they are capable of producing arbitrarily short pulses. For example, if the FIFO contains thirty-one words, and SI and SO pulses are applied simultaneously, the HF flag may produce an arbitrarily short pulse, depending on the precise phase of SI and SO.

The flags will always settle to the correct state after the appropriate delay (e.g., T_{HFL}, T_{HFH} in this example). This property of the status flags will clearly be a function of the dynamic relation between SI and SO. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

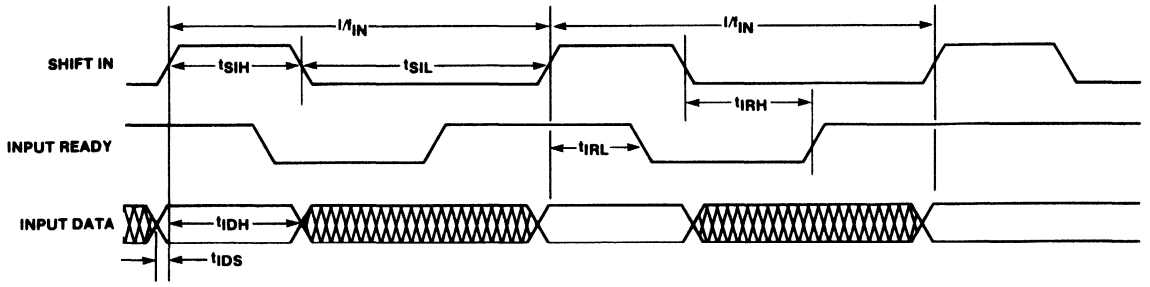


Figure 1. Input Timing

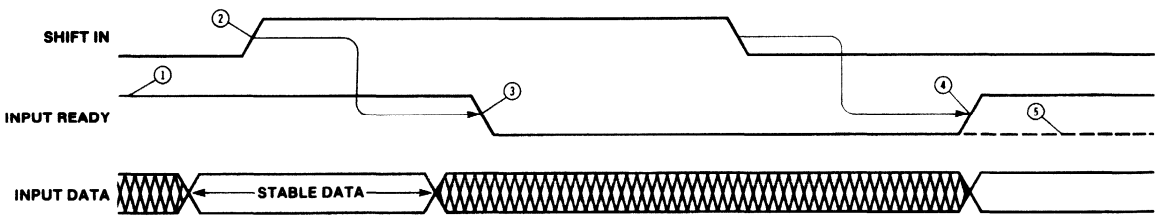


Figure 2. The Mechanism of Shifting Data into the FIFO

① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
② Input Data is loaded into the first available memory location.
③ Input Ready goes LOW indicating this memory location is full.
④ Shift-In going LOW allows Input Ready to sense the status of the next memory location. The next memory location is empty as indicated by Input Ready HIGH.
⑤ If the FIFO is already full then the Input Ready remains low.
Note: Shift-In pulses applied while Input Ready is LOW will be ignored.

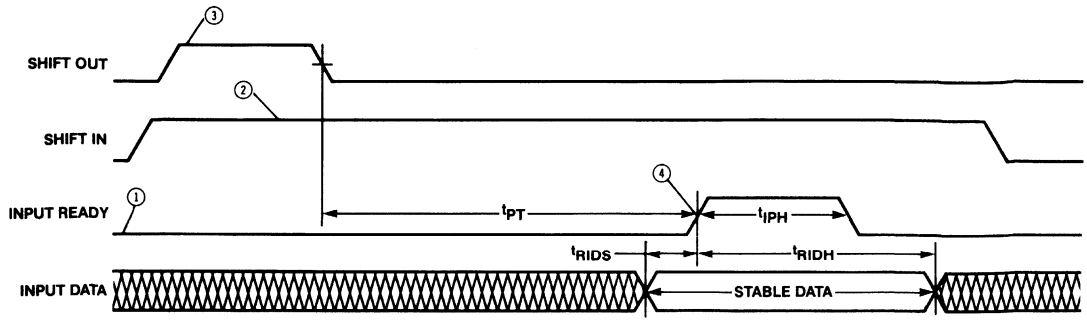


Figure 3. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.
② Shift In is held HIGH.
③ Shift Out pulse is applied. An empty location is detected by the internal pointers on the falling edge of SO.
④ As soon as Input Ready becomes HIGH the Input Data is loaded into this location.

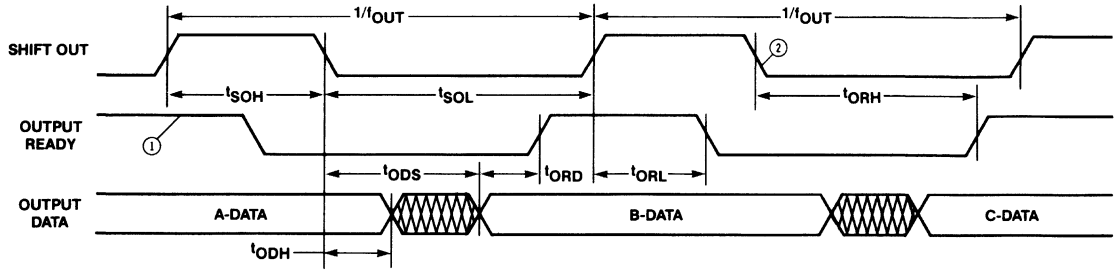


Figure 4. Output Timing

① The diagram assumes that the FIFO contains at least three words: A-Data (first input word), B-Data (second input word), and C-Data (third input word).
② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

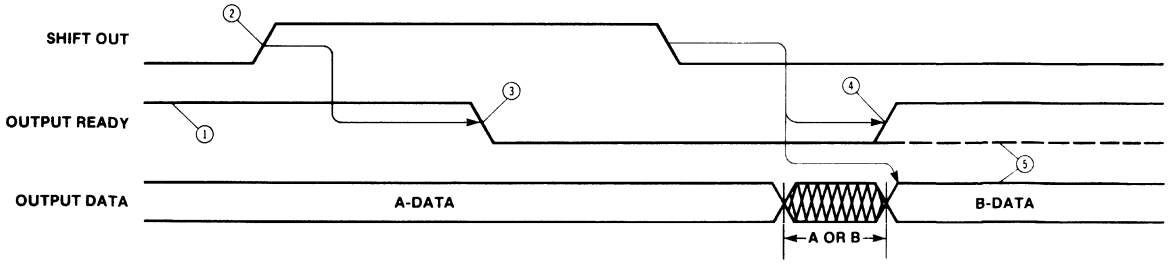


Figure 5. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
② Shift-Out goes HIGH causing B-Data (second input word) to advance to the output register. Output data remains as valid A-Data while Shift-Out is HIGH.
③ Output Ready goes LOW.
④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data remains the same (A-Data).

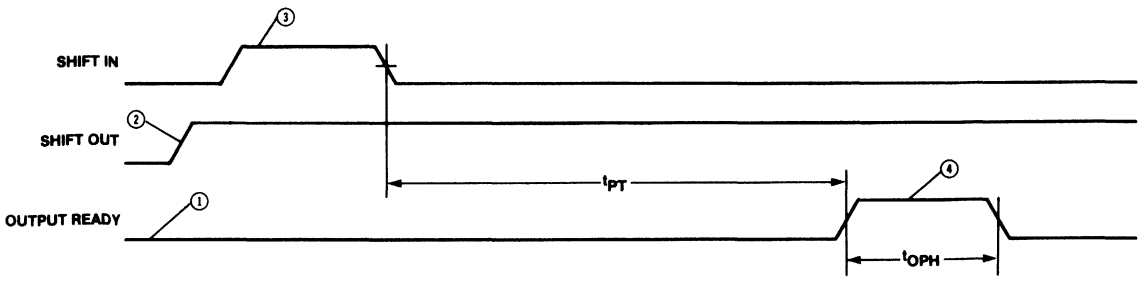


Figure 6. t_{PT} and t_{OPH} Specification

① FIFO is initially empty.
② Shift-Out is held HIGH.
③ Shift-In pulse applied. A full location is detected by the internal pointers on the falling edge of Shift-In
④ As soon as Output Ready becomes HIGH, the word is shifted out.

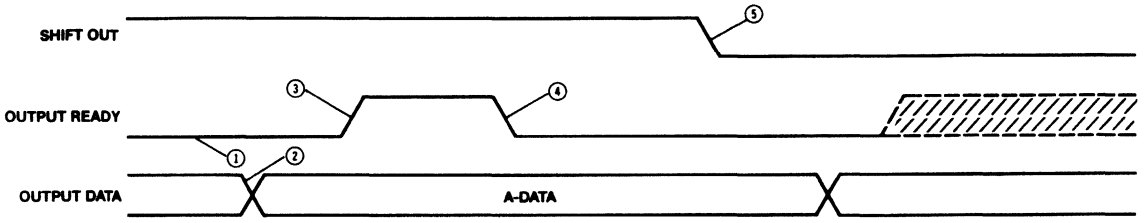


Figure 7. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

① The internal logic does not detect the presence of any data in the FIFO.
② New data (A) arrives at the outputs.
③ Output Ready goes HIGH indicating arrival of the new data.
④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
⑤ As soon as Shift Out goes LOW the Output Data is subject to change.
Output Ready will go HIGH or remain LOW depending on whether there are any additional upstream words in the FIFO.

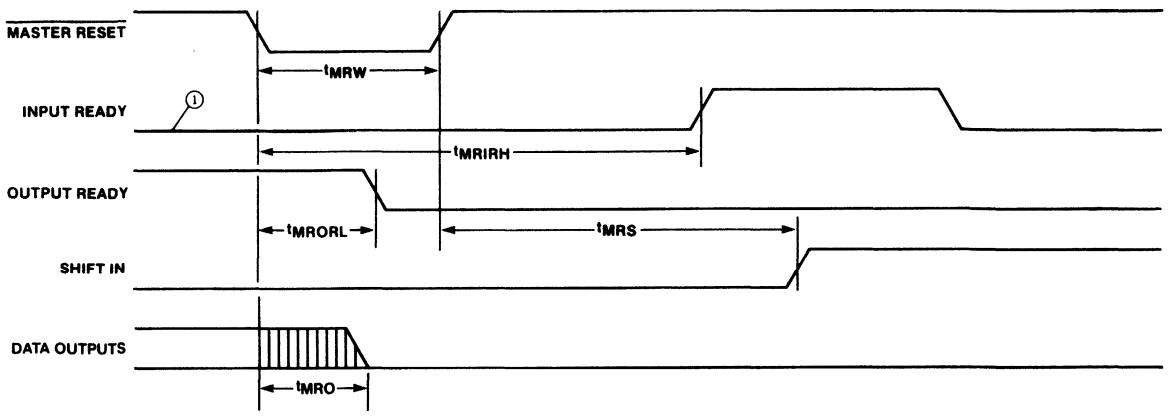


Figure 8. Master Reset Timing

① FIFO is initially full.

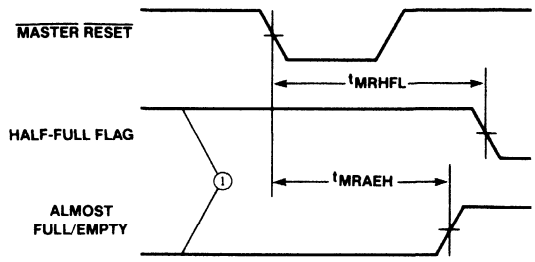


Figure 9. t_{MRHFL}, t_{MRAEH} Specifications

① FIFO intially has between 32 and 56 words.

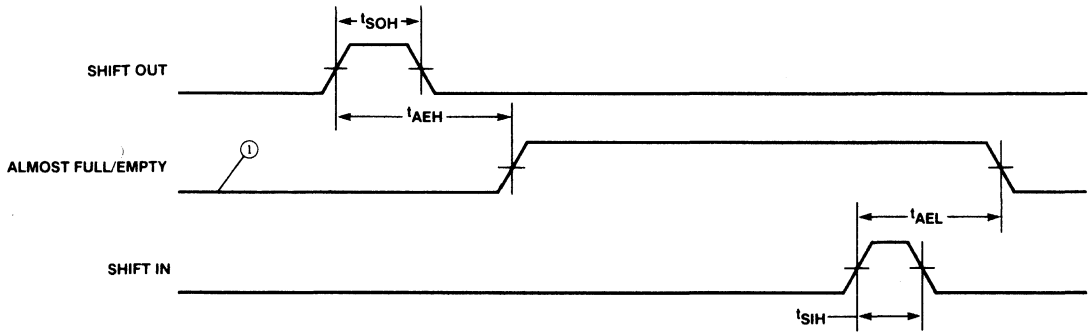


Figure 10. t_{AEH}, t_{AEL} Specifications

① FIFO contains 9 words (one more than almost empty).

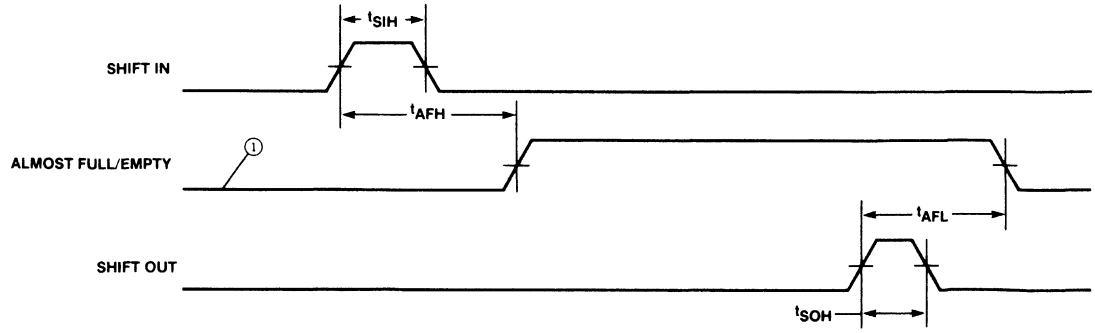


Figure 11. t_{AFH}, t_{AFL} Specifications

① FIFO contains 55 words (one short of almost full).

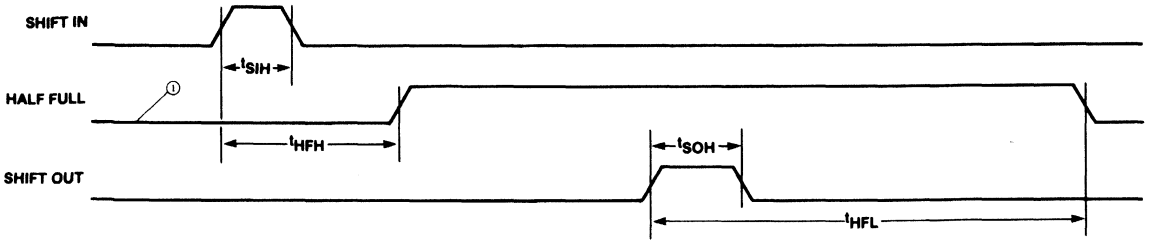
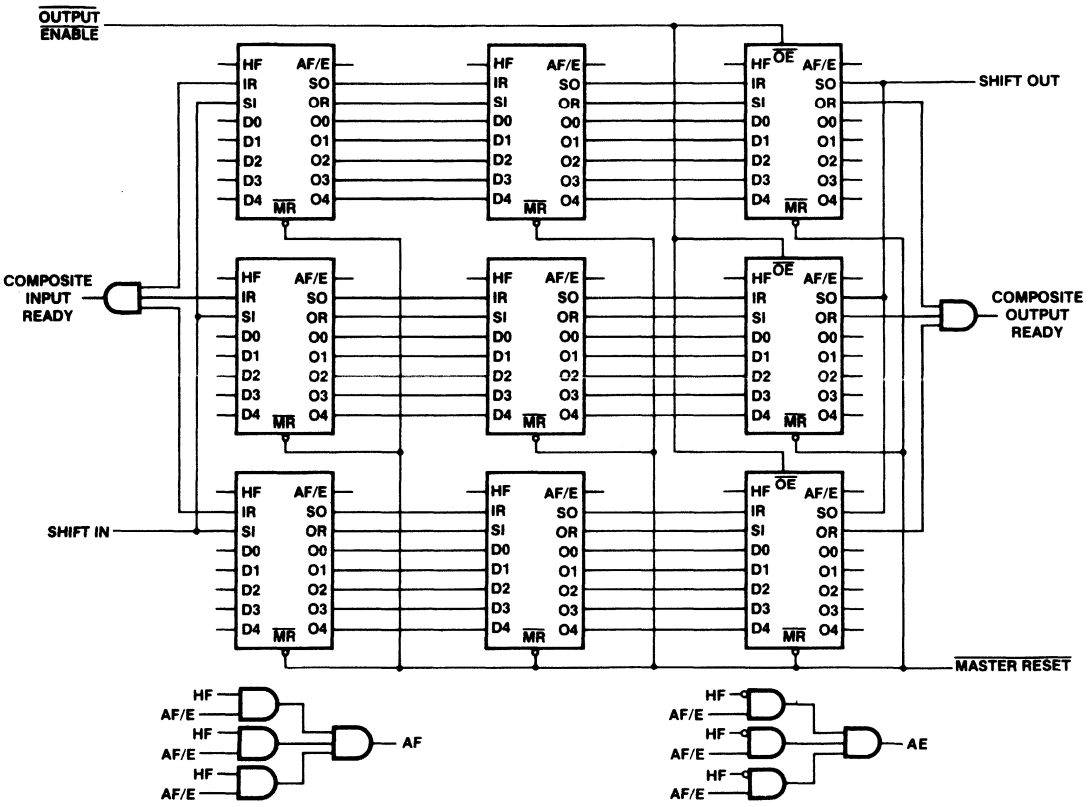


Figure 12. t_{HFL}, t_{HFH} Specifications

① FIFO contains 31 words (one short of half full).



Almost Full (AF) is eight words or less to FIFO full.
Almost Empty (AE) is eight words or less to FIFO empty

Figure 13. 192x15 FIFO

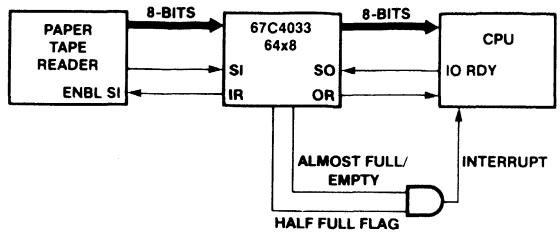
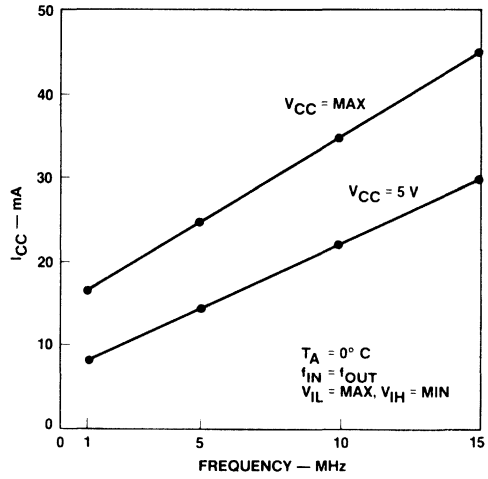


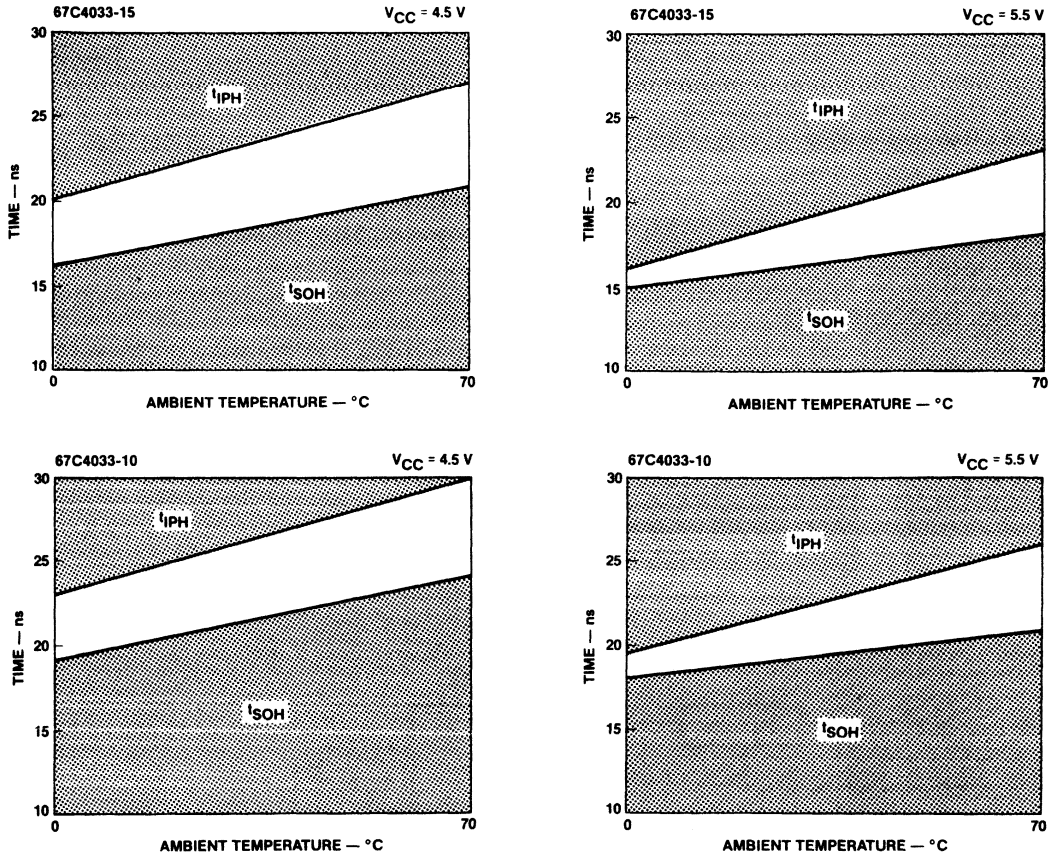
Figure 14. Application for 67C4033 "Slow and Steady Rate to Fast 'Blocked Rate' "

Note: Expanding the FIFOs in word width is done by ANDing the IR and OR as shown in Figure 13.

I_{CC} VS. FREQUENCY



Guaranteed Distribution of t_{IPH}, t_{SOH} vs. Temperature (For Cascadability Only)



Guaranteed Distribution of t_{OPH}, t_{SIH} vs. Temperature (For Cascadability Only)

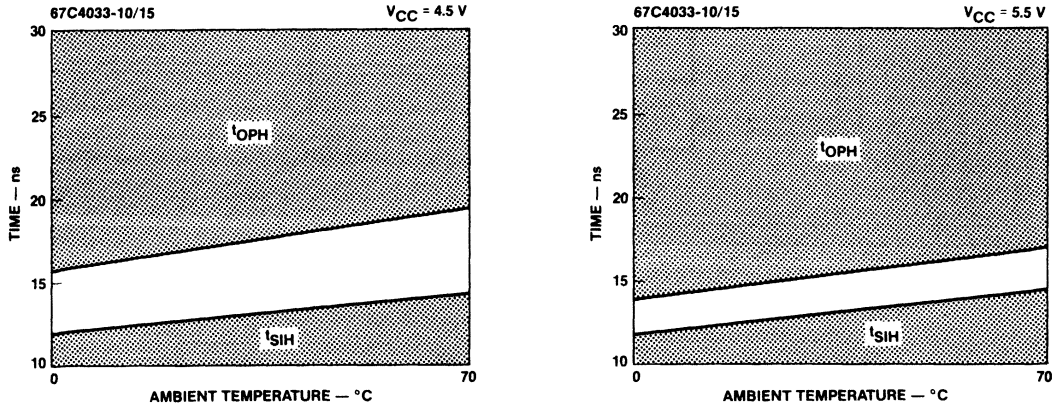


Figure B. Cascadability

Am4601

Programmable-Flags, 512 x 9 FIFO

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 512 x 9 RAM-based FIFO
- 25 and 35 ns access times
- Two fixed flags; full and empty
- Two programmable flags; programmable from 1 to 511
- Programmable polarity for all four flags
- Data, $\overline{R}$, and $\overline{W}$ pinout compatible with industry-standard (720X) FIFOs
- Programmable depth mode

GENERAL DESCRIPTION

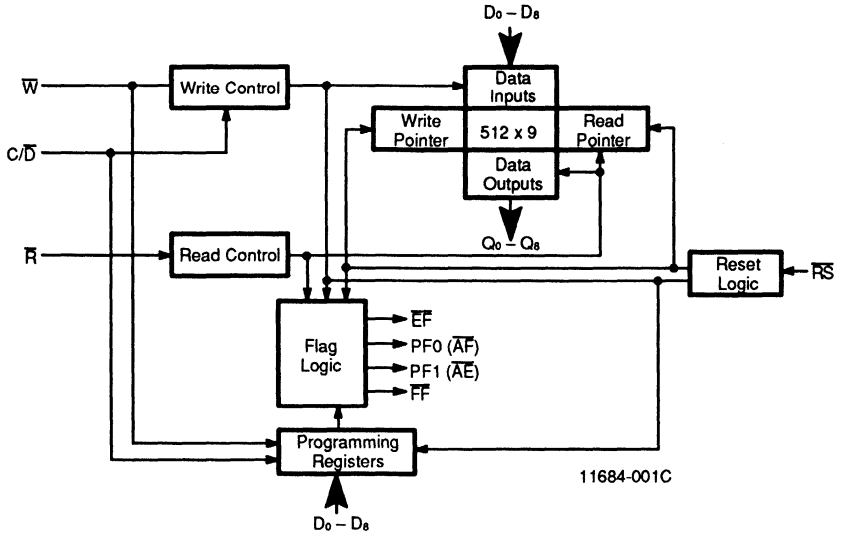
The Am4601 is a RAM-based CMOS FIFO that is 512 words deep with 9-bit wide words. It has two fixed flags, Full and Empty, and two programmable flags, programmable from 1 to 511 in increments of one.

The Am4601 can accept data and output data asynchronously and simultaneously at data rates from 0 to 28.5 MHz. The Am4601 has four programming registers which allow the user to program the two programmable flags, to program the polarity of each of the four flags, and to change the total usable depth of the FIFO.

The Am4601 data, $\overline{R}$ and $\overline{W}$ pinout is identical to industry standards 720X FIFOs.

The Am4601 is ideally suited for data buffering applications such as in communication, image processing, mass storage, DSP and printing systems. The programmable flags and the programmable depth mode of the Am4601 are especially useful for advance status signaling and message packing required for high performance systems.

BLOCK DIAGRAM



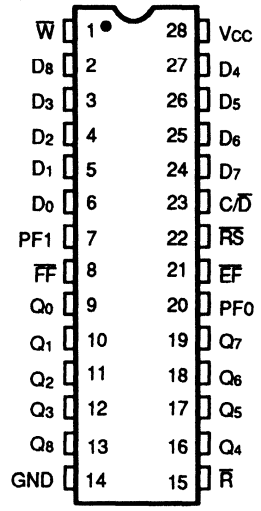
PRODUCT SELECTOR GUIDE

Part Number	Am4601-25	Am4601-35
Access Time	25 ns	35 ns
Maximum Power Supply Current	90 mA	80 mA
Operating Frequency	28.5 MHz	22.2 MHz
Operating Range	Com'l	Com'l

Publication# 11684 Rev. C Amendment/0
Issue Date: March 1991

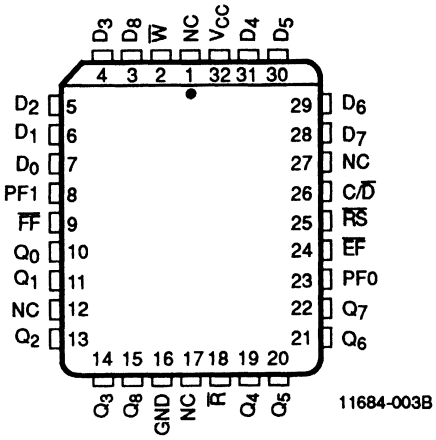
CONNECTION DIAGRAMS
Top View

DIP



11684-002B

PLCC

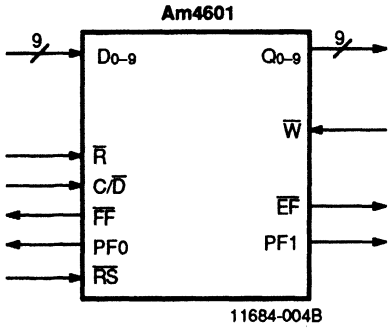


11684-003B

Notes:

Pin 1 is marked for orientation for plastic packages.
NC: No Connection.

LOGIC SYMBOL



11684-004B

PIN DESCRIPTION

D_8–D_0

9-Bit Input Data

Q_8–Q_0

9-Bit Output Data

$\overline{R}$

Active-Low Read Control

$\overline{W}$

Active-Low Write Control

C/$\overline{D}$

Command/Data Selection

C/$\overline{D}$ =1: Enables writing to the programming registers (FIFO is empty and PB = 0)

C/$\overline{D}$ = 0: Enables writing to the FIFO memory.

$\overline{RS}$

Master Reset

Resets, when low, the FIFO address pointers, and initializes the programming registers to their default values.

$\overline{EF}$

Empty Flag

Programmable polarity

$\overline{FF}$

Full Flag

Programmable polarity

PF0

Programmable Flag 0

Defaults to Almost Full ($\overline{AF}$) upon reset.

PF1

Programmable Flag 1

Defaults to Almost Empty ($\overline{AE}$) upon reset.

V_{CC}

Power Supply Pin

Input, +5 Volts

GND

Ground Supply Pin

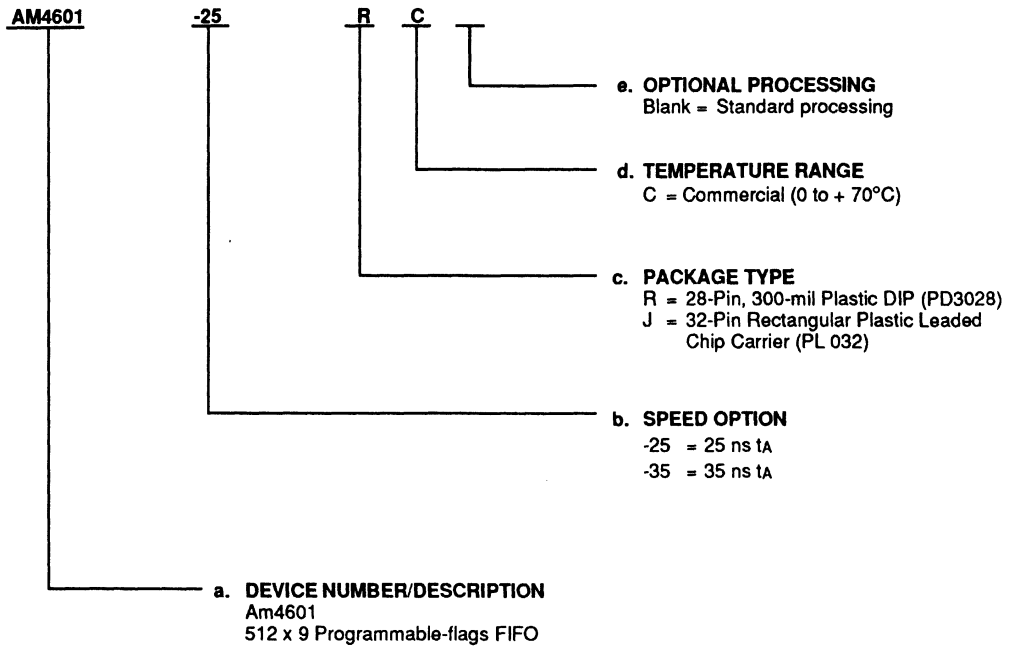
Input, 0 Volts

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM4601-25	RC, JC
AM4601-35	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released valid combinations.

FUNCTIONAL DESCRIPTION

The Am4601 Programmable-Flags CMOS FIFO is designed around a 512 x 9 dual-port static RAM array (see block diagram). Two dedicated address counters – read address pointer and write address pointer-facilitate the sequential FIFO operation. The address pointers roll over to address zero after reaching address 511.

Flag logic determines the difference between the Write and Read address pointers and generates the four status flags. The trip points of two programmable flags and the polarity of all four flags are programmed via the programming registers. The flag logic also prevents overwriting the FIFO when it is full and reading the FIFO when it is empty.

Resetting the FIFO is realized by pulsing the $\overline{RS}$ pin. Both address pointers are initialized to zero and the programming registers return to their default vales.

For applications that require a FIFO of a different depth than 512, the Am4601 can be programmed to block writing when the programmable flag PF0 is asserted. Thus the Am4601 functions as a programmable-depth FIFO.

Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle (See Figure 7). For a valid Reset cycle to occur, both the Read ($\overline{R}$) and Write ($\overline{W}$) must be HIGH through the low-to-high transition of the Reset ($\overline{RS}$) signal. The Reset cycle initializes the FIFO to an empty condition and the programming registers to a default state. Both address pointers are reset to zero, the programmable depth mode is disabled, and the Register Programming bit in register 3 (PB) is enabled to allow programming of the registers. The polarity of the Full flag, the Empty flag and programmable flag 0 is set to assertive-low, and the polarity of programmable flag 1 is set to assertive-high. PF0 is initialized to trigger at address 496 ($\overline{AF}$) and PF1 is set to trigger at 16 ($\overline{AE}$).

Read / Write Operations

Am4601 read and write operations are controlled by $\overline{R}$, $\overline{W}$, and C/$\overline{D}$ control lines. $\overline{R}$ controls the read operation, $\overline{W}$ controls the write operation, and C/$\overline{D}$ the data into the FIFO memory or into the programming registers.

The falling edge of $\overline{R}$ initiates the read cycle and valid data appears on the outputs (Q_0–Q_8) after the access time (t_A). Data remains valid until t_{dv} after the rising edge of $\overline{R}$ and then the outputs go to high-impedance state. Cycling the $\overline{R}$ also increments the Read address pointer. When the FIFO is empty, $\overline{R}$ is ignored.

Data may be written into the FIFO memory (C/$\overline{D}$ = 0)or into the programming registers (C/$\overline{D}$ = 1, the FIFO is empty, and PB = 0). $\overline{W}$ going low initiates the write cycle. Data on the input must be stable t_{DS} before and t_{DH} after the rising edge of $\overline{W}$.

When C/$\overline{D}$ = 1, PB = 0, and the FIFO is empty, the data will be written into the programming registers. Otherwise the data will be written into the FIFO memory, and the write address counter will be incremented. When the FIFO is full, or when the write blocking bit is set and the FIFO reaches the PF0 programmed limit, the $\overline{W}$ signal is ignored.

A special case of write occurs when a write operation is initiated while the part is full. The next read will cause $\overline{FF}$ to go inactive, and data can then be latched into the FIFO t_{WPF} after the rising edge of $\overline{FF}$ (see Figure 11).

A special case of read occurs when a read operation is initiated while the part is empty. The data latched in by the next write will be accessed t_A ns after the rising edge of $\overline{EF}$. Read is held active, and cannot be deasserted until t_{RPE} after the rising edge of $\overline{EF}$ (see Figure 10).

Flag Operation

After a Reset cycle the FIFO is empty and the flags reflect the FIFO's empty status and the flag defaults ($\overline{EF}$ = 0, $\overline{FF}$ = 1, PF0 = 1, PF1 = 0). After the first write operation, the Empty flag changes its state (to "not empty") following the rising edge of $\overline{W}$. PF0 and PF1 are asserted following the falling edge of the $\overline{W}$ during the cycle that makes the number of words in the FIFO equal to the flag's programmed values. The Full flag changes its state (from "not full" to "full") after the falling edge of $\overline{W}$ at the cycle that writes into the last location of the FIFO (see Figure 8).

When reading the first word out of a full FIFO, the Full flag changes its state (from "full" to "not full") after the rising edge of $\overline{R}$. PF0 and PF1 change their state following the rising edge of the $\overline{R}$ during the cycle that makes the FIFO hold fewer words than the programmed value. When reading the last word from the FIFO the Empty flag changes status from "not-empty" to "empty" following the falling edge of $\overline{R}$ (See Figure 9).

When asserted, the Full flag prevents any further write operations into the FIFO. Similarly, the Empty flag, when asserted, prevents any further read operations. When the FIFO is programmed as a programmable depth FIFO (Write Blocking Bit = 1), PF0, when asserted, prevents any further write operations into the FIFO. Thus, PF0 serves in this mode as a Full flag.

PF0 and PF1 assertion is similar to the Full Flag. They are asserted following the falling edge of the Write which takes the FIFO to the programmed depth. They are deasserted on the rising edge of the Read which empties the FIFO to the programmed depth. PF0 and PF1 can be programmed to any value from 1 to 511. The value 0 is illegal for either PF0 or PF1.

During programming, the flags may change their states. The flags must be ignored during the programming sequence.The flags settle to their proper states following the fourth register write at the end of the programming sequence.

Programming the Flags

The Am4601 has four, 8-bit wide, programming registers that allow the programming of:

- Programmable flag 0 (PF0) value
- Programmable flag 1 (PF1) value
- Write blocking bit (WB)
- Programming blocking bit (PB)

The four programming registers may be programmed after master reset or when the FIFO is empty and PB = 0. The registers are programmed by four sequential write operations with $C/\overline{D}$ = 1 (see Figures 5 & 6).

$C/\overline{D}$ = 1 routes the data from D_0– D_7 inputs into the programming registers and prevents the FIFO's write address pointer from incrementing. A special register pointer increments automatically after each programming write operation and points to the next register. Figure 1 shows the data format of the programming registers.

The four registers must be programmed in four sequential write operation. Stopping before the completion of four programming cycles will result in FIFO malfunction. The flags change their states during programming and must be ignored during these four cycles. The programming registers are write-only.

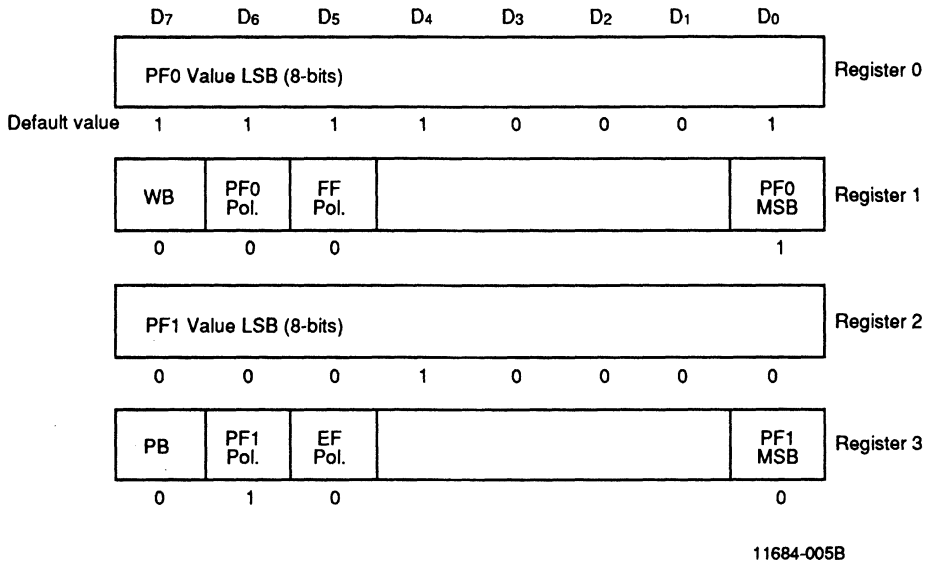


Figure 1. Programming Registers Format and Defaults

Register 0:

Stores the 8 LSB bits of Programmable flag 0 (PF0) location. A Reset cycle sets register 0 to the value 496 (16 words from full).

Register 1:

Stores the MSB location-bit of PF0 and the following control bits:

WB

Write Blocking control bit; enables write blocking with PF0.

WB = 1: Changes the PF0 flag to act as a FULL flag. The PF0 flag will block the write pulses to the FIFO after the flag is set. This feature can be used in applications where only a part of the 512 bytes is needed. In those applications the programmable FIFO is used as a programmable depth FIFO.

WB = 0: The PF0 flag has no control on the write pulses to the FIFO. The write pulses will be blocked only after the FULL flag is set.

After Reset, WB bit is 0.

PF0 Pol.

Selects the polarity of the PF0 programmable flag.

PF0 Pol = 0: The programmable flag will be asserted-low.

PF0 Pol = 1: The programmable flag will be asserted-high.

After Reset, PF0 Pol bit is 0.

FF Pol.

Selects the polarity of the FULL flag.

$\overline{FF}$ Pol. = 0: The FULL flag will be active-low.

$\overline{FF}$ Pol. = 1: The FULL flag will be active-high.

After Reset, $\overline{FF}$ Pol. bit is 0.

Register 2:

Stores the 8 LSB bits of Programmable flag 1 (PF1) location. After Reset PF1 is set to 16 (16 words from empty).

Register 3:

Stores the MSB bit of PF1 location and the following control bits:

PB

Programming Blocking Bit; enables blocking of programming.

PB = 0: The registers are programmed by writing to the FIFO while the C/$\overline{D}$ input is 1, while the FIFO is empty. With C/$\overline{D}$ = 1, writes to the registers while the FIFO is not empty will be addressed to the FIFO core array and not the registers. The registers can be accessed again after a master reset, or when the FIFO is empty. After a reset cycle the PB bit is 0.

PB = 1: PB = 1 disables any further writes to the registers. The programming registers cannot be written into until PB is reset to 0 by a Master reset. PB is set by writing into the register and is reset by a reset cycle.

PF1 Pol.

Selects the polarity of the PF1 programmable flag.

PF1 Pol. = 0: The programmable flag will be asserted-low.

PF1 Pol. = 1: The programmable flag will be asserted-high.

After Reset, PF1 Pol. bit is 1.

EF Pol.

Selects the polarity of the EMPTY flag.

EF Pol. = 0: The EMPTY flag will be active-low.
EF Pol. = 1: The EMPTY flag will be active-high.

After reset, the EF Pol. bit is 0.

AFTER MASTER RESET

After master-reset the programming registers go to the following default values:

Register 0	1 1 1 1	0 0 0 1
Register 1	0 0 0 X	X X X 1
Register 2	0 0 0 1	0 0 0 0
Register 3	0 1 0 X	X X X 0

PF0: Is set at 497, asserted-low to act as an Almost Full, active-low flag ($\overline{AF}$). When Low, PF0 will indicate that the FIFO has more than 496 words.

PF1: Is set at 16, asserted-high to act as an Almost Empty, active-low flag ($\overline{AE}$). When Low, PF1 will indicate that the FIFO has less than 16 words in it.

Empty flag Polarity: Active-low

Full flag Polarity: Active-low

WB: The write block is reset to 0; i.e. the FIFO will be in normal operation mode.

PB: The programming block is reset to 0 to allow programming of the registers.

APPLICATIONS

The Am4601 programmable FIFO provides high speed data buffering for digital systems. The FIFO's programmable flags allow the system designer to optimize data throughput and to achieve better system performance. The most common uses of the programmable flags are advance system signaling of boundary conditions, and message packing. The programmable depth mode is useful to buffer complete messages of different lengths.

Programmable Flags for Advance System Signaling

In many systems data is generated or received by a subsystem with slow response time (The system may generate or receive data at one rate, but requires substantially longer time to stop, or start the data stream). For such a system, time must be allowed so that the system can react to the full or empty flags and prevent data loss due to writing into a full FIFO (or reading out of an empty FIFO). In many cases, the user uses the half full flag (HF) of a standard FIFO as a system level signal to stop and start the data flow. While this solution works in many applications, it has some drawbacks. The FIFO cannot be filled more than half way, resulting in inefficient use of a deeper (and costlier) FIFO where a less expensive, half-depth FIFO could be used. In other cases, the system is slowed to accommodate the time it takes to react to the flags. There, the system and the FIFO are not used to their best performance.

The Am4601 programmable flags are specifically designed to answer this application. The user may program the two programmable flags to trip at any point. Thus, if the FIFO is getting near to full condition, a programmable flag can be set to trigger at a desired number of cycles before the FIFO fills up. Thus, the system gets an early warning with enough time to react to the boundary condition flags (full and empty). At the same time, the FIFO and the system may run at full speed allowed by the data stream.

Programmable Flags for Message Packing

In other systems, throughput and performance are achieved by sending complete messages through the system data channels. The reason is that a substantial overhead is associated with establishing a communication channel. Be it a simple parallel bus, or a sophisticated communication trunk, it takes a long time for the arbitration circuits to grant a subsystem access to the communication channel. Passing a short, or partial message through the channel awards a small benefit for the hefty expense of arbitrating for the channel. A much more efficient use of communications channels is to send complete messages of preferred sizes.

When a FIFO is used at either side of a communication channel, the system may benefit from writing into the FIFO a complete message, or reading a complete message from it. Since a standard FIFO provides only empty, full, and half-full status flags, the system designer is limited to using the FIFO for message lengths that fit into the FIFO status signals. Moreover, the FIFO can be used to contain one or two messages only.

Using the Am4601 programmable flags, the user can signal the system that space is provided to receive a message of a preferred length. Also, the flags may be used to tell the system on the either side that the FIFO contains at least one complete message for transmission. This way, the system throughput may be optimized using complete message transmission and reception.

Programmable Depth

Where a long string of data of a particular length needs to be received or transmitted, the Am4601 can have its depth altered. The Am4601 is then programmed to disallow further write operation once one of the programmable flags (PF0) is triggered. The FIFO depth can be therefore programmed to any length between 1 and 511. In this mode the full flag is replaced by the programmable flag.

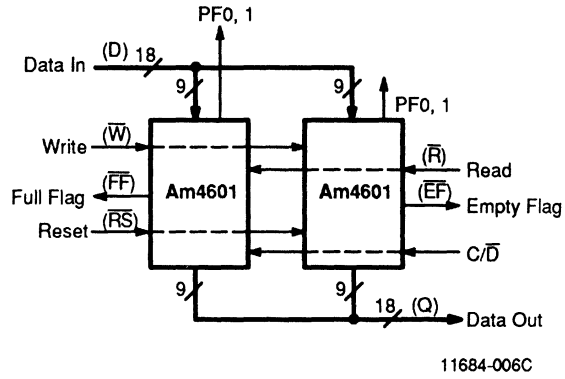


Figure 2. Width-Expansion to Form a 512 x 18 FIFO

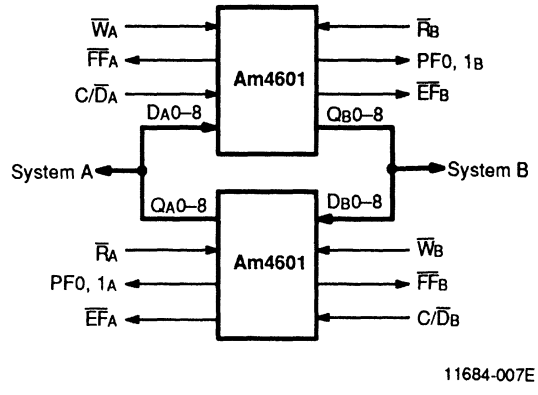


Figure 3. Bidirectional FIFO Mode

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0.5 to +7.0 V
All Signal Voltages	–0.5 to +7.0 V
DC Output Current	20 mA
Power Dissipation	1.0 W
Operating Temperature	–55 to +125°C
Storage Temperature	–65 to +155°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Supply Voltage	+4.5 to +5.5 V
Operating Temperature	0 to +70°C

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Commercial		Unit
			Min.	Max.	
I_{OH}	Output High Current	V_{OH} = 2.4 V, V_{CC} = 4.5 V	–2.0		mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V, V_{CC} = 4.5 V	+6		mA
V_{IH}	Input High Voltage	(Note 1)	2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	(Note 1)		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}, V_{CC} = 5.5 V	–10	10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5 V	–10	10	µA
I_{CC1}	Static Operating Supply Current	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5 V (Note 2)		15	mA
I_{CC2}	Dynamic Operating Current, (22.2 MHz Max.)	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5 V (Note 2)		80	mA
I_{CC3}	Dynamic Operating Current, (28.5 MHz Max.)	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5 V (Note 2)		90	mA

Notes:

1. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do no attempt to test these values without suitable equipment.
2. I_{CC} measurements are made with outputs open.

CAPACITANCE (Note 3) (V_{CC} = 5.0, T_A = 25°C, f = 1.0 MHz)

Parameter Symbol	Parameter Descriptions	Test Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	7	

Note:

3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

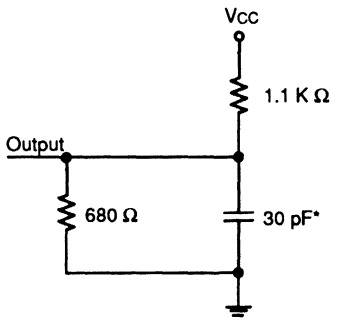
No.	Parameter Symbol	Parameter Description	Am4601-25		Am4601-35		Unit
			Min.	Max.	Min.	Max.	
Write Timing							
1	t_{WC}	Write Cycle Time	35		45		ns
2	t_{WPW}	Write Pulse Width	15		15		ns
3	t_{WR}	Write Recovery Time	8		10		ns
4	t_{DS}	Data Setup Time	15		15		ns
5	t_{DH}	Data Hold Time	2		2		ns
6	t_{AS}	C/$\overline{D}$ Setup Time	5		5		ns
7	t_{AH}	C/$\overline{D}$ Hold Time	0		0		ns
8	t_{WFF}	Write LOW to Full Flag LOW/HIGH		30		30	ns
9	t_{WPF}	Write LOW to PF0, 1 asserted		45		45	ns
10	t_{WEF}	Write HIGH to Empty Flag HIGH/LOW		30		30	ns
11	t_{WLZ}	Write HIGH to data bus at LOW-Z (Note 1)	10		10		ns
Read Timing							
12	t_{RC}	Read Cycle Time	35		45		ns
13	t_{A}	Access Time		25		35	ns
14	t_{RR}	Read Recovery Time	8		10		ns
15	t_{RPW}	Read Pulse Width	25		35		ns
16	t_{RLZ}	Read LOW to data bus at LOW-Z (Note 1)		5		5	ns
17	t_{DV}	Data Valid from Read HIGH	5		5		ns
18	t_{RHZ}	Read HIGH to data bus HIGH-Z (Note 1)		18		20	ns
19	t_{RFF}	Read HIGH to Full Flag HIGH/LOW		30		30	ns
20	t_{RPF}	Read HIGH to PF0, 1 asserted		45		45	ns
21	t_{REF}	Read LOW to Empty Flag LOW/HIGH		30		30	ns
Reset Timing							
22	t_{RSC}	Reset Cycle Time	35		45		ns
23	t_{RS}	Reset Pulse Width	25		25		ns
24	t_{RSS}	Reset Setup Time	25		35		ns
25	t_{RSR}	Reset Recovery Time	10		10		ns
26	t_{EFL}	Reset to Empty and PF1 Flags LOW	35			45	ns
27	t_{FFH}	Reset to Full and PF0 Flags HIGH	35			45	ns

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output loads	See Figure 4



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* Includes jig and scope capacitances

Figure 4. AC Test Load

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

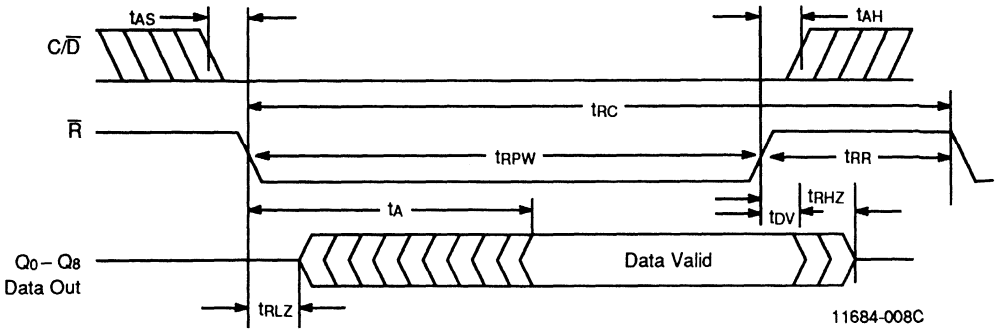


Figure 5. Read Timing Diagram

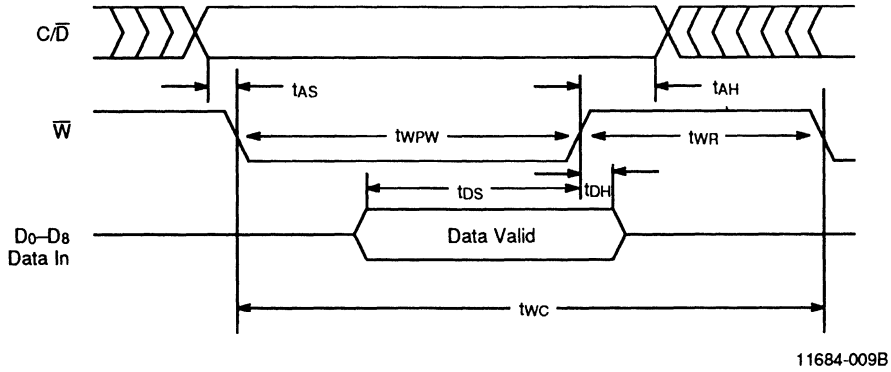


Figure 6. Write Timing Diagram

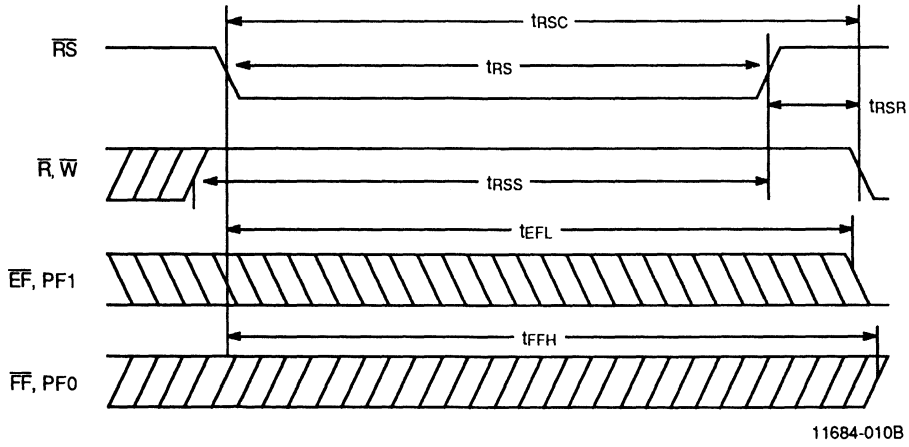


Figure 7. Reset Timing Diagram

SWITCHING WAVEFORMS

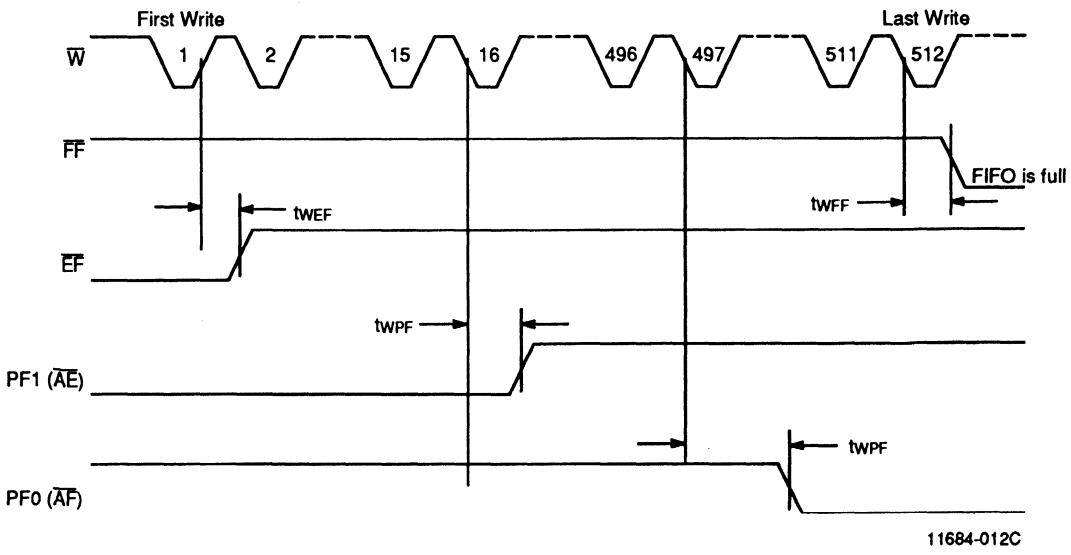


Figure 8. Flag Timing (Write Cycles) – Operated in Default Value

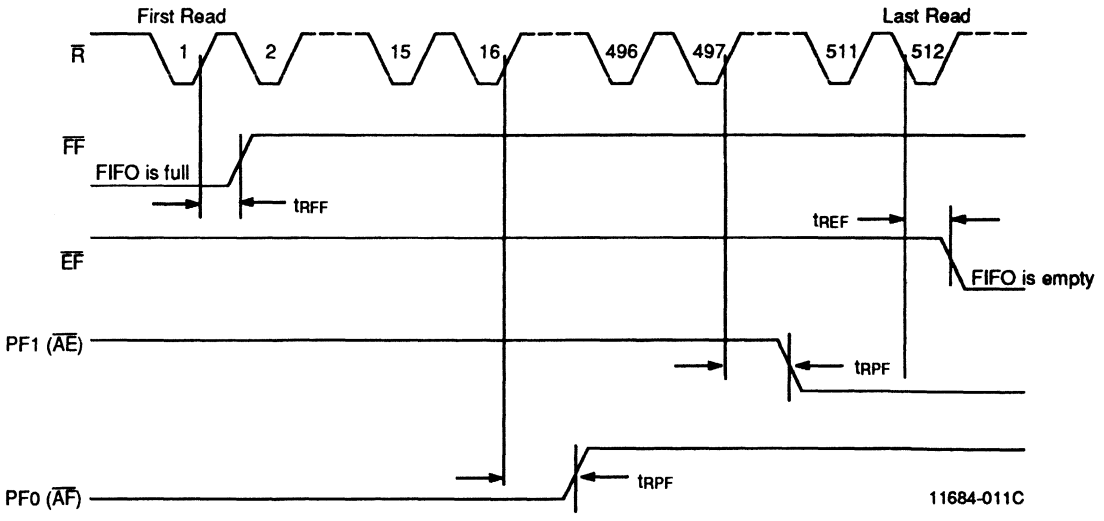
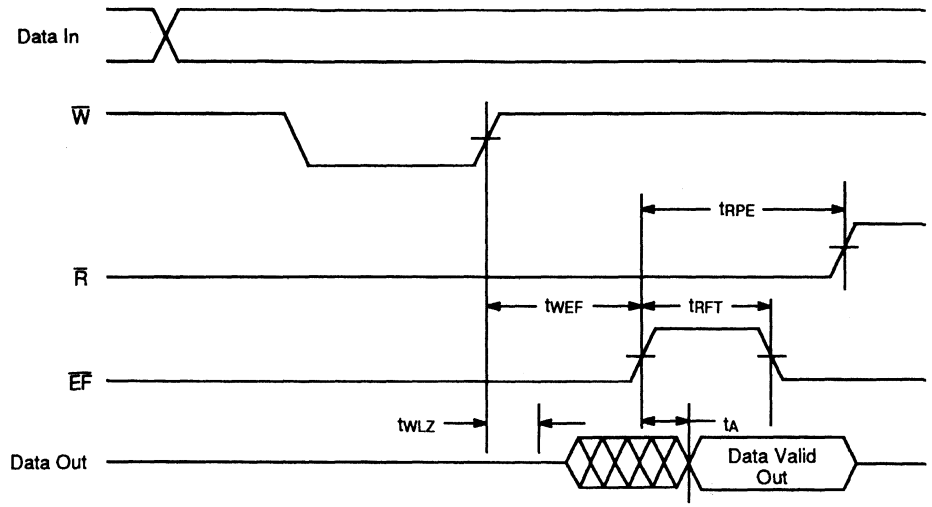


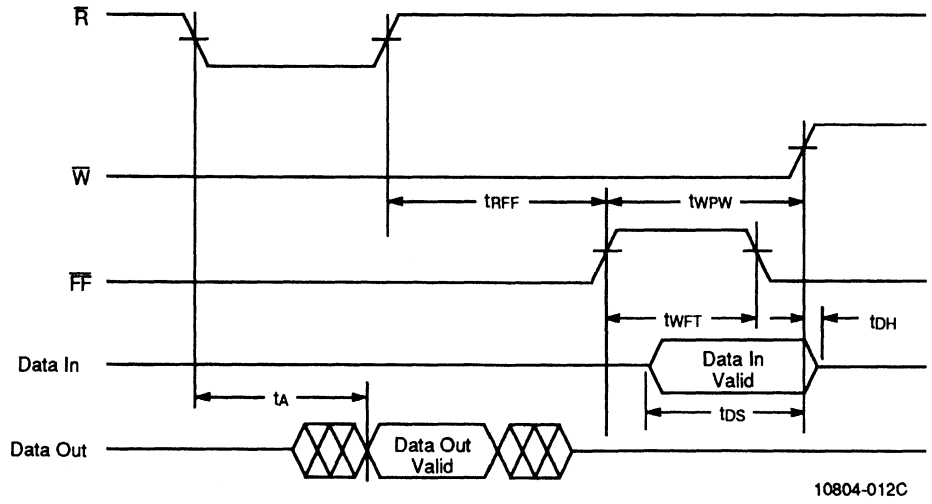
Figure 9. Flag Timing (Read Cycles) – Operated in Default Value



Note: ($t_{RPE} = t_{RPW}$, $t_{RFT} = t_{REF}$)

10804-011B

Figure 10. Read Data Flow-Through Mode



10804-012C

Note: ($t_{WFT} = t_{WFF}$)

Figure 11. Write Data Flow-Through Mode

Am4701 BiFIFO

Dual 512 x 8 Bidirectional Parity Generator/Checker, Bypass Mode, Programmable AE/AF Flags

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Two 512x8 FIFO buffers
- Full and Empty Flags
- Built in parity checker/generator
- Programmable interrupt request
- Generates and detects framing bit
- Low power consumption
- Bidirectional full duplex communication
- Programmable Almost-Full and Almost-Empty flags
- Bypass mode—Changes the Am4701 to a transceiver
- Bidirectional mailbox communication
- Byte detect on read

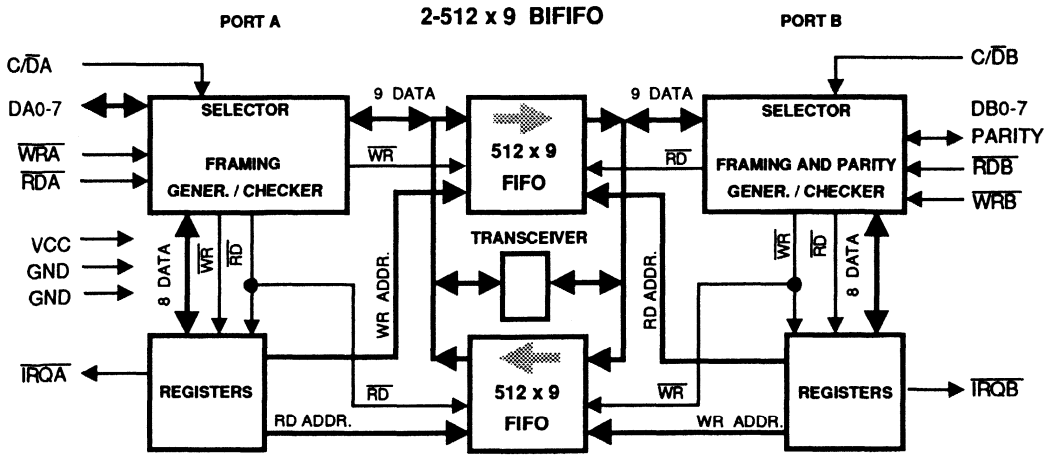
GENERAL DESCRIPTION

The Am4701 is a CMOS RAM-based, fully asynchronous, byte-wide bidirectional First In First Out (FIFO) device that is 512 words deep with 8-bit wide words in each direction. It contains two 512 x 9 FIFOs with the ninth bit in each array used for framing and parity functions.

The Am4701 can accept and output data asynchronously and simultaneously at data rates from 0 to 22.2 MHz for standard commercial temperature range products and 0 to 16.7 MHz for military temperature range APL products. Interrupt driven status flags are provided to signify Full, Empty and user programmable Almost Full and Almost Empty condition. Parity generation/checking, programmable interrupt requests, byte-detection, framing and port-to port communication through mail boxes are provided on chip. The Am4701 can also operate in Bypass Mode where it behaves like a transceiver.

The Am4701 is ideally suited for bidirectional interprocessor communication and data-buffering between a CPU and a peripheral device. The ability to buffer large transfers of data and its rate adaption capabilities make the Am4701 useful in communication, image processing, DSP and printing systems.

BLOCK DIAGRAM



11120-011A

PRODUCT SELECTOR GUIDE

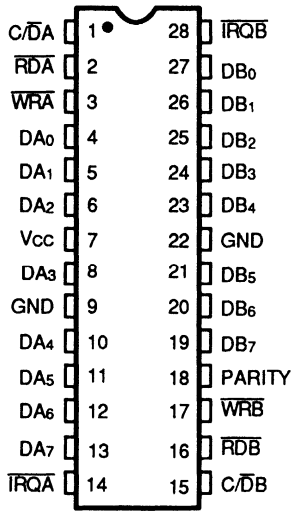
Part Number	Am4701-35	Am4701-45	
Access Time	35 ns	45 ns	
Maximum Power Supply	100 mA*	100 mA	120 mA
Operating Range	Com'l	Com'l	Mil

* At 16.7 MHz

CONNECTION DIAGRAMS

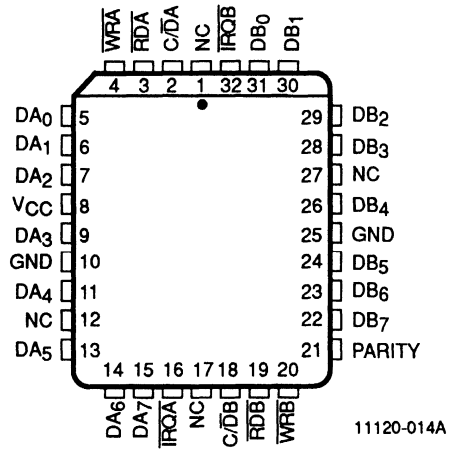
Top Views

DIPs*



11120-013A

PLCC



11120-014A

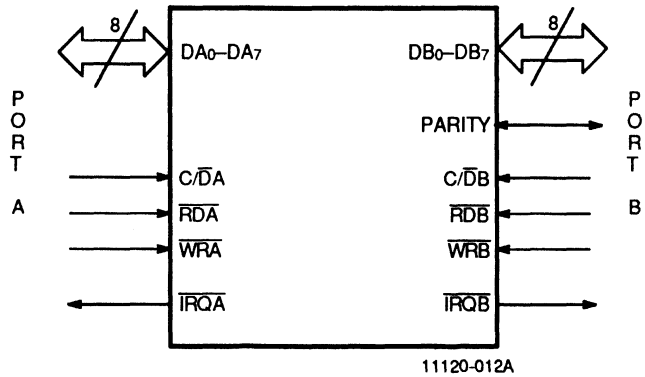
* Pinout identical for both plastic and ceramic DIPs.

Notes:

Pin 1 is marked for orientation for plastic packages.

NC: No Connection.

LOGIC SYMBOL

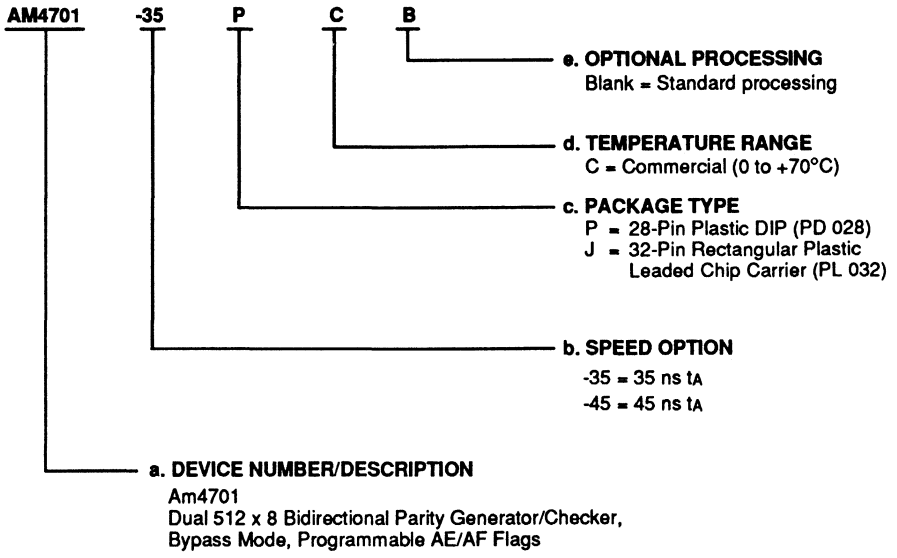


11120-012A

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM4701-35	PC, JC
AM4701-45	

Valid Combinations

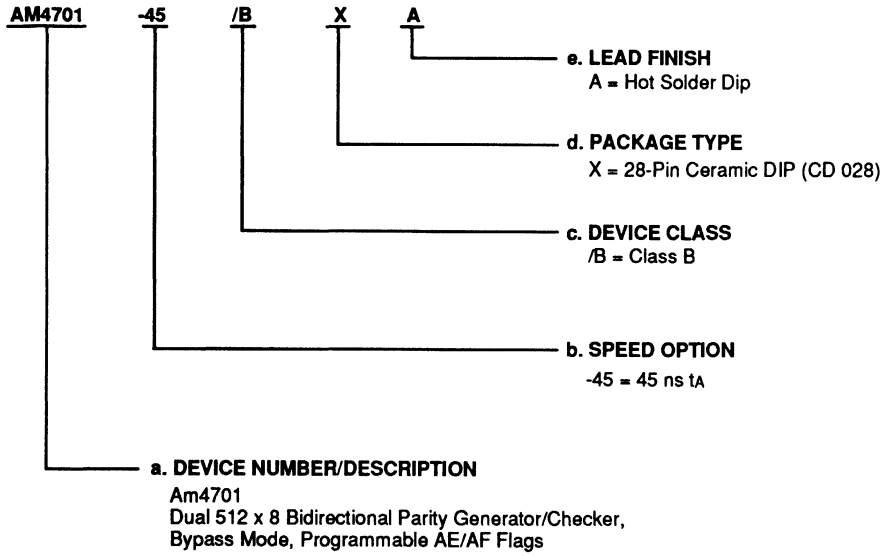
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM4701-45	/BXA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations.

Group A Tests

Group A Tests consist of subgroups 1, 2, 3, 7, 8, 9 10, 11.

Military Burn-in

Military burn-in is in accordance with the current revision of MIL-STD 883, Test Method 1015, conditions A through E. Test conditions are selected at AMD's option.

PIN DESCRIPTION

DA_7–DA_0, DB_7–DB_0

8-bit bidirectional data bus for port A,B.

PARITY

Bidirectional parity/framing bit (Port B only)

$\overline{RDA}$, $\overline{RDB}$

Read input for port A or B. The falling edge of Read initiates a read from the FIFO or the internal registers. Both ports can be read simultaneously by $\overline{RDA}$ and $\overline{RDB}$.

$\overline{WRA}$, $\overline{WRB}$

Write input to port A or B. The falling edge of Write initiates a write cycle. Both ports can write simultaneously by $\overline{WRA}$ and $\overline{WRB}$.

C/$\overline{D}$

Command/Data selection for port A or B. C/$\overline{D}$ = High: Read or Write to the internal registers. C/$\overline{D}$ = Low: Read or Write to the FIFO.

$\overline{IRQA}$, $\overline{IRQB}$

Interrupt request output of port A, B. The $\overline{IRQ}$ flag will be active low by any changes of status in the appropriate port and is reset by reading the status register of the same port. Each port's $\overline{IRQ}$ flag can be masked by its mask register.

Vcc

Power Supply Pin, Input, +5 Volts

GND

Ground Supply Pin, Input, 0 Volts

FUNCTIONAL DESCRIPTION

The Am4701 BiFIFO consists of two 512 x 8 FIFOs connected to provide bidirectional FIFO action between two data ports, A and B. One FIFO provides buffering in the direction from A to B; the other FIFO provides buffering from B to A. The Am4701 also provides a set of application specific support logic to support communication between microprocessors and peripheral devices. This logic includes the following functions:

- Optional FIFO bypass for direct data transfer
- 9th bit for framing bit generation and detect
- Optional parity generate and detect on Port B
- Optional parity error insertion as framing bit
- Byte detect
- Mailbox registers
- Programmable Almost Empty and Almost Full flags
- Read and write pointer reset
- Interrupt on flag assertion

Operation of the Am4701 BiFIFO is controlled by two sets of registers, one for each port. Command registers in each set determine the operating mode for each port, and Status registers in each set indicate the status of chip operations. The remaining registers in each set provide data to support status bit generation. Though the registers will be reset to the default state during power up, it is recommended to always use the master reset to ensure proper operation. An interrupt pin is provided for each port. This pin can be activated by bits in its associated Status register and allow external hardware detection of a change in the status of the BiFIFO.

There are a variety of applications of the Am4701 BiFIFO. The bidirectional FIFO buffering feature simplifies CPU to CPU communication. The parity logic on Port B allows convenient communication between a CPU and a bus which requires parity generation and detection. The direct connect transceiver function provides efficient communication of command and status data between a CPU and a peripheral chip such as a disk controller while the FIFO function provides efficient buffering of its high speed data.

Read/Write Operations

Am4701 read and write operations are controlled by $\overline{RD}$, $\overline{WR}$ and C/$\overline{D}$ control lines for each port. $\overline{RD}$ gates BiFIFO data to the bus, and the rising edge of the WR signal latches data from the bus into registers or a FIFO in the Am4701.

The C/$\overline{D}$ input selects the source or destination of the data. When C/$\overline{D}$ is low, data is written into or read from the appropriate FIFO for that port, with one exception: when Port A is in the Bypass mode, data will be transferred directly between Port A and Port B, bypassing the FIFOs. When C/$\overline{D}$ is high, data is written to or read from one of the registers in the port register set.

The register set for the Am4701 is shown in Table 1. All registers are read or written in a two cycle operation. The first cycle loads a Pointer register to select the register to be read, and the second cycle performs the read or write data transfer to the selected register. The Pointer register is cleared to zero by the data transfer cycle. Because the Pointer register is cleared to zero, the Status register may also be read directly in a single cycle. This is because the zero select code corresponds to the Status register. The Status register is therefore always selected and available to be read unless the Pointer register has been set to another value.

Table 1. Register Address Assignments

Reg Addrs	Write	Read
0	Pointer	Status
1	Command	Command
2	Mask	Mask
3	Byte Detect	Byte Detect
4	Outbound Mailbox	Outbound Mailbox
5	AE/AF	AE/AF
6	Reset Read Pointer	Inbound Mailbox
7	Reset Write Pointer	

Pointer Register

7	6	5	4	3	2	1	0
FB					A_2	A_1	A_0

11120-019A

The Pointer register contents select which register in the register set is to be read or written, as shown in Table 1. The Pointer register is a write-only register. All register accesses are performed in two consecutive cycles: register select cycle and register data transfer cycle. The Pointer register is set by the register select cycle, and it is reset to zero by the completion of the data transfer cycle. The format of the Pointer register is as follows.

Bit	Name	Function
FB	Framing Bit	Writes a framing bit into the FIFO. This bit is set by writing it twice to the Pointer register. An 80 (hex) code is written to select the Pointer register and an 80 code is written to the Pointer register during the transfer cycle.
A2–A0	Reg Select	Selects a register for read or write transfer per Table 1.

Command Register

7	6	5	4	3	2	1	0	
MR	SH	BP						Command, Port A
MR	SH		PE	PO/PE				Command, Port B

11120-020A

The Command register sets the operating mode for each port. The Command register format for Port A and Port B are different. Port A can be put into Bypass mode, and Port B can enable its parity generate/detect logic as well as determine its polarity. The format of the command registers is as follows.

Bit	Name	Function
MR	Master Reset	Software master reset. Resets both FIFOs and the register sets on both ports. Either port can set the master reset bit. The MR bit in the command register must be written twice consecu tively and the status register of the same port must be read to complete a master reset operation. This prevents accidental resets. Setting the MR in the command register sets the MR bit in both status registers.
SH	Shift	Selects the FULL, EMPTY, AE and AF flags from the other port for display in the Status register. This allows displaying current status of the other port.
BP	Bypass	Bypass mode select (Port A only). See Bypass mode section.
PEN	Parity Enable	Parity generate and check enable. (Port B only.) When this bit is set, the parity logic on Port B generates and checks bus parity at the Port B I/O inputs. See Parity Generate and Check section.
PO/PE	Odd/Even	Parity Odd or Even select. PO/PE = 1 for odd parity, PO/PE = 0 for even.

Status Register

7	6	5	4	3	2	1	0
MR	FULL	EMPT	AF	AE	MB	BDT	PE/FD

11120-021A

The Status register indicates the status of various conditions on its associated port. The bits in the status register will be set automatically when those conditions occur and will activate the $\overline{IRQ}$ pin for the appropriate port. Reading the Status register will clear the PE/FD, MR, and the BDT bits. The mailbox bit is cleared by reading the Inbound Mailbox register. FULL, EMPTY, AF, and AE are cleared by reading the status register provided the condition making the bit go true ceased to exist. If the condition causing the bit the be set is still prevalent, then reading the status counter makes these bit "dynamic" and reflect the real condition of the FIFO until the FIFO exits and re-enters that condition. Then, the $\overline{IRQ}$ signal and the appropriate bit will be asserted again. Note that when the Shift bit in the Command register is a one, the Status register will display the FULL, EMPTY, AF, end AE flags for the other port. The format of the Status register is as follows.

Bit	Name	Function
MR	Master Reset	Set when either port has issued a master reset. The MR bit will be cleared by reading the status register.
FULL	Full	Outbound FIFO is full. Write command will be ignored as long as the FIFO is full. The flag is cleared by reading the status register and reading the FIFO in either order (see explanation above). The flag is also cleared by MR.
EMPT	Empty	Inbound FIFO is empty. Read command will be ignored as long as the FIFO is empty. The flag is cleared by reading the status register and writing to the FIFO in either order (see explanation above). The flag is also cleared by MR.
AF	Almost Full	Outbound FIFO is almost full. Set when the FIFO reaches or exceeds the depth limit programmed into the AE/AF register. Cleared by reading the status register and making the FIFO go below the depth limit (see explanation above). The flag is also cleared by MR.
AE	Almost Empty	Inbound FIFO is almost empty. Set when the FIFO reaches or is under the depth limit programmed into the AE/AF register. Cleared by reading the status register and making the FIFO go above the depth limit (see explanation above). The flag is also cleared by MR.
MB	Mailbox	The Inboard Mailbox register has been written into by the other port. Cleared by reading the Inbound Mailbox register or by MR.
BDT	Byte Detect	Set when the data at the output of the inbound FIFO matches the data in the Byte Detect register. Cleared by reading Status reg or MR.
PE/FD	Parity Error/ Frame Detect	Set by the 9th bit of the inbound FIFO. Indicates a framing bit or Frame Detect parity error was inserted into the FIFO by the other port. Cleared by reading Status reg or MR.

Mask Register

7	6	5	4	3	2	1	0
	FULL	EMPT	AF	AE	MB	BDT	PE/FD

11120-022A

The Mask register masks the bits of the Status register which will generate the interrupt request, $\overline{IRQ}$. The bits are set by the appropriate conditions but do not trigger the $\overline{IRQ}$ signal if masked out. A one in the Mask register enables interrupt by the corresponding bit in the Status register; a zero in the Mask register disables it. The MR bit of the Status register is unmaskable and will always cause an interrupt when set. The bit definitions for the Mask register are the same as for the Status register.

Byte Detect Register

7	6	5	4	3	2	1	0
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

11120-023A

The Byte Detect register contains a programmable byte to be detected while reading the FIFO. When the data being read from the FIFO matches the contents of the Byte Detect register, the BDT flag in the Status register is set.

AE/AF Register

7	6	5	4	3	2	1	0
AF_3	AF_2	AF_1	AF_0	AE_3	AE_2	AE_1	AE_0

11120-024A

The contents of the AE/AF register defines the limits for the Almost Empty and Almost Full flags. Limit programming is done in increments of 16. A code of 0 (hex) for either limit corresponds to 16 for the Almost Empty flag and (512–16) for the Almost full flag. A code of F for either limit corresponds to 256 for the Almost empty flag and (512–256) for the Almost Full flag. Master reset will set this register corresponding to a limit of 16 for both AE and AF. In this case, AF will set at 16 writes before full, and AE will set at 16 reads before empty.

Bit	Name	Function
AF_{3-0}	Almost Full	Almost Full limit code: 0000 = 16, 0001 = 32, etc. 1111 = 256.
AE_{3-0}	Almost Empty	Almost Empty limit code: 0000 = (512–16), 0001 = (512–32), etc.

Outbound Mailbox Register

7	6	5	4	3	2	1	0
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

11120-023A

Each port has an 8-bit mailbox where it can receive messages from the other port. The mailbox for a given port is called the Inbound Mailbox. The mailbox for the other port is called the outbound Mailbox. The Outbound Mailbox register is the mailbox register for the other port. This register is written into when a message is to be sent to the other port. Writing to this register will cause the MB bit to be set in the Status register of the other port and will cause a mailbox interrupt on that port if enabled by its Mask register.

The Outbound Mailbox register can be read as well as written. The contents of the Outbound Mailbox register will be cleared to zero and zeros will be read back when the other port reads its Inbound Mailbox register. This can be used to determine whether the other port has received the message.

Inbound Mailbox Register

7	6	5	4	3	2	1	0
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

11120-023A

The Inbound Mailbox register receives 8-bit messages from the other port. The other port sends a message by writing into its Outbound Mailbox register. The message thus written appears in the Inbound Mailbox for this port. When the mailbox register has been written into, the MB bit is set in the Status register. The MB bit is reset and the mailbox register is cleared to zeros when the Inbound Mailbox register is read.

FIFO Read and Write Pointer Reset

The read pointer for the inbound FIFO and the write pointer for the outbound FIFO can be reset by writing with the appropriate register select code. The operation requires two cycle as for any other register write operation: address latching and a (dummy) write. No data is actually transferred, but the appropriate pointer is reset. Resetting the write pointer allows overwriting a block that may have contained bad data. Resetting the read pointer allows rereading a block.

Resetting the read or write pointers may cause erroneous AF and AE flags. Only a master reset will cause correct AF and AE flags. It is recommended that the AF and AE flags be masked by the Mask register when using these pointer reset commands.

Master Reset

The master reset operation resets both FIFOs and the register sets on both ports. Either port can initiate a master reset operation. The MR bit in the command register must be written twice consecutively and the status register of the same port must be read to complete a master reset operation. This prevents accidental resets. Setting the MR in the command register sets the MR bit in both status registers. A master reset sequence is outlined below:

Port 1	Port 2
Port 1 writes a 1 into the MR bit of the command register (a 2-cycle register operation).	
Port 1 writes a 1 into the MR bit of the command register (a 2-cycle register operation) again.	
	Both $\overline{IRQ}$ signals are asserted The MR bits in both status registers are set
	If port 2 reads its status register, its $\overline{IRQ}$ signal will be deasserted. The MR bit in the status register will not be cleared.
Port 1 reads its status register	
	The master reset operation is complete
Port 1 $\overline{IRQ}$ signal is deasserted The MR bit of port 1's status register is cleared.	
	If port 2 has already read its status register, the MR bit will now be cleared.
	If port 2 has not read its status register yet, both $\overline{IRQ}$ and the MR bit will be cleared once port 2 reads it.

After a master reset, the Am4701 will come up in the default state described below.

- Both FIFOs cleared to empty
- Command registers cleared
  - Port A Bypass mode disabled
  - Port B Parity generate and detect disabled
- AE/AF register cleared to zero: i.e., AF and AE flags set to 16
- Mask registers set to Full and Empty flags only enabled
- $\overline{IRQ}$ is reset on both ports due to Master Reset (despite Empty condition on both ports)

The registers will typically be reset to the default state by power up; however, this power up reset cannot be guaranteed. Therefore, a Master Reset should always be performed after power up to insure proper operation.

Status Interrupts

If a condition for an interrupt occurs, the corresponding bit in the status register will be automatically set. If that bit is enabled by its corresponding bit in the Mask register, the $\overline{IRQ}$ signal for that port will be asserted. Reading the status register clears the $\overline{IRQ}$ signal and may clear the bit in the Status register as well. One exception is the MB, Mailbox bit which can only be cleared by reading the Inbound Mailbox register.

Status register interrupts are used to signal the CPU on a port that something interesting has happened rather than having to continually poll for activity.

Framing Bit

The FIFOs in the Am4701 are 512 x 9 in organization. Eight data bits communicate with the external port data buses; the ninth bit is used as a framing bit to identify natural divisions in the data. The Framing bit can be set by writing to the Pointer register with the FB bit set to one.Two write operations are required, one to set the address and one to set the framing bit (like any other register access). Both operations are performed with 1 in the FB location and address 0. This will cause a one to be written to the ninth FIFO bit when the other eight

FIFO data bits are written. The Framing bit is reset to zero when the word is written into the FIFO.

When the eight bits of data are read from the FIFO, the Framing bit is written into the FB bit of the Status register. If the Framing bit is a one and the corresponding Mask register bit is set, an interrupt will be generated. The Framing bit can thus be used to signal the receiving port that a block of data has been received, for example.

Port B has additional capability for setting the Framing bit. If Port B parity generation and detect is not enabled and if the Parity input pin is high during a Port B FIFO write, the Framing bit will be set. This allows hardware generation of the Framing bit.

Parity

The Am4701 has built-in parity generate and parity check logic for port B. The parity generate and check logic simplifies interfacing the Am4701 to a bus with byte parity. Parity generation for data being read from the FIFO and written to the bus provides the required bus parity bit along with the eight bits of bus data. Parity check logic for data being read from the bus and written into the FIFO provides the required parity checking on the data received from the bus.

Parity Generate

Port B parity generate and check logic is enabled by a bit in the Port B Command register. A corresponding bit in the Command register defines the parity sense: odd or even. When this logic is enabled, parity is generated for data being read from the FIFO on port B.

Parity check

When Port B's parity generate and check bit in the command register is set, data coming into the FIFO on port B will be checked for parity. If parity error is detected port B's $\overline{IRQ}$ and parity error bit will be set. The FIFO will automatically attach an error bit to the word in error and when this word comes out of port A, port A's $\overline{IRQ}$ and parity error bit will be set. This will allow the recipient of the data to recognize the word in error and to act accordingly.

Port A Bypass Mode Data Transfer

The Bypass mode allows Port A to bypass the FIFOs and directly control the Port B data bus. In this mode, the Am4701 functions as a transceiver-similar to a 74LS245. In this mode, data written to Port A will be gated directly onto the Port B data bus. Reading Port A data will read the state of the Port B data bus lines. The truth table for this operation is shown in Table 2.

Bypass mode allows a CPU on Port A to control a peripheral chip such as a disk controller on Port B. The CPU typically requires direct access to the command and status registers of the disk controller chip to set up a disk I/O operation. Once the operation is begun, the FIFOs are used to buffer the high speed disk data. By providing the Bypass mode, the Am4701 allows this communication without requiring external logic.

Also, the Bypass mode allows port A to read from and write into port B's register set. This feature is useful in applications where one port has "intelligent" control and the other port is a "slave" only.

The Bypass mode supports the following operations (see table):

Data transfer from port B to port A (Port A read)

Data transfer from port A to port B (port A write)

Port A access of port A registers

Port A access of port B's registers

Port A access of port B's registers is performed in two cycles just like an ordinary register access with the exception that port A's C/$\overline{D}$ signal is held Low and port B's C/$\overline{D}$ is held High during both register address latching and register data transfer.

Table 2. Bypass Mode Truth Table

Function	$\overline{RDA}$	$\overline{WRA}$	C/$\overline{D}$A	$\overline{RDB}$	$\overline{WRB}$	C/$\overline{D}$B
Writing data from Port A to Port B Bus.	H	L	L	X	X	L
Reading data from Port B to Port A Bus.	L	H	L	X	X	L
Writing data to Port A registers.	H	L	H	X	X	X
Reading data from Port A's reg'rs to Port A.	L	H	H	X	X	X
Writing data from Port A to B registers.	H	L	L	H	L	H
Reading data from B registers to Port A.	L	H	L	L	H	H

Mailbox Operations

Each port has an 8-bit mailbox where it can receive messages from the other port. The mailbox for a given port is called the Inbound Mailbox. The mailbox for the other port is called the outbound Mailbox. The Outbound Mailbox register is the mailbox register for the other port. This register is written into when a message is to be sent to the other port. Writing to this register will cause the MB bit to be set in the Status register of the other port and will cause a mailbox interrupt on that port if enabled by its Mask register.

The Outbound Mailbox register can be read as well as written. The contents of the Outbound Mailbox register will be cleared to zero and zeros will be read back when the other port reads its Inbound Mailbox register. This can be used to determine whether the other port has received the message.

An example of the mailbox passing protocol is given below.

Port 1	Port 2
Port 1 writes a message byte to Port 2 by writing to its Outbound Mailbox register	
	Port 2 $\overline{IRQ}$ signal is asserted and MB bit set
	Port 2 reads its Status register and recognizes the MB bit. The IRQ signal is reset.
	Port 2 reads its Incoming Mailbox. The mailbox register, and the MB bit are reset.
Port 1 reads the message it wrote in its Outbound Mailbox register. If all bits are zero, Port 2 must have read its mail.	
.... Ready for next message	

APPLICATIONS

The Am4701 provides bidirectional buffering of high speed digital data. Its application support logic makes it well suited to providing communication between two CPUs, between a CPU and a bus and between a CPU and a peripheral device.

An example of a simple 8-bit CPU-to-CPU connection is shown in Figure 1. In this case, parity is not used, and a simple, high speed communication path is set up using a single chip.

Figure 2 shows an example of the Am4701 used to provide communication between a CPU and a bus with byte parity. In this case, the parity generation and check logic available on Port B is used to provide the parity generation and checking required by the bus. The Am4701 provides this function without requiring any external logic, representing a savings in chip count, board space and complexity.

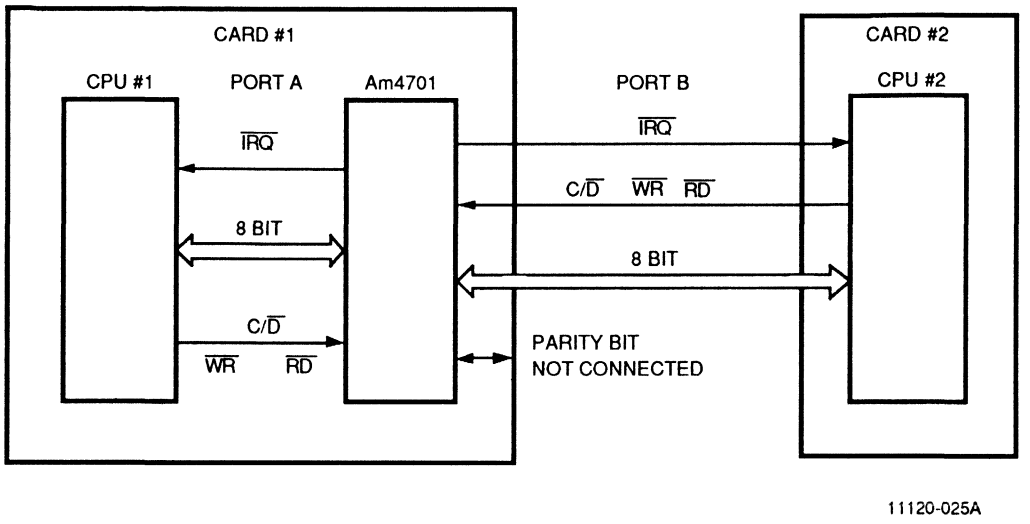


Figure 1. CPU-CPU Communication

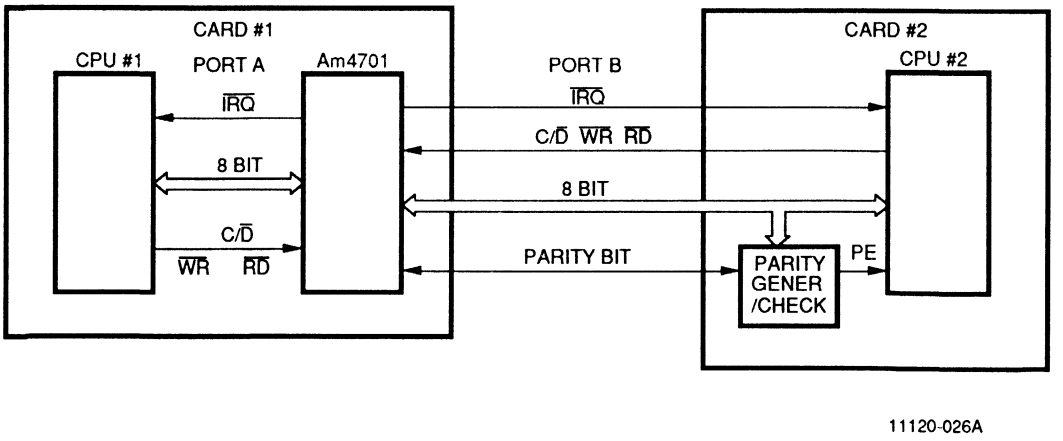


Figure 2. CPU-CPU Communication With Parity

In Figure 3, the Am4701 is used as a single chip interface between a CPU and a peripheral device such as a disk controller chip. The Am4701 provides a number of benefits in this single chip communication design. The Bypass mode allows the CPU to set up both the registers in the peripheral device as well as the Port B register set of the Am4701. The bidirectional FIFO function provides buffering of data at rates up to 16 megabytes/second. Finally, the interrupt function provides direct indication to the CPU of data transfer status of the peripheral device, allows the CPU to set up the most efficient mode of processing by exception, and provides control information to the peripheral interface logic (the PAL) to allow it to sequence the peripheral device in a direct manner.

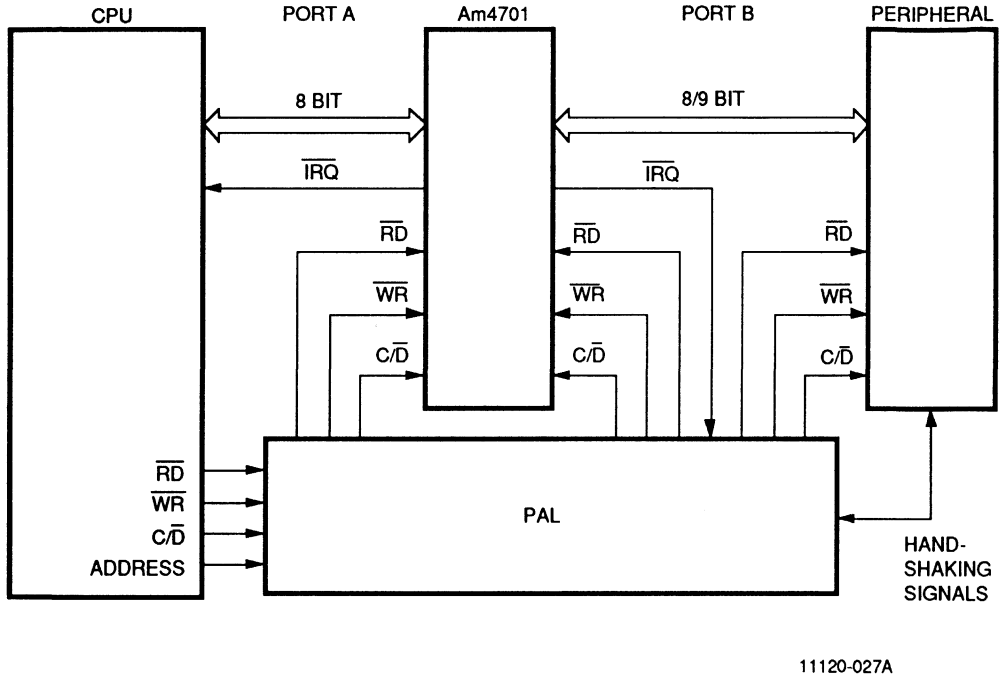


Figure 3. CPU-Peripheral Communication with Bypass

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to +7.0 V
All Signal Voltages	-0.5 to +7.0 V
DC Output Current	20 mA
Power Dissipation	1.0 W
Operating Temperature	-55 to +125°C
Storage Temperature	-65 to +155°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Commercial (C) Devices

Supply Voltage	+4.5 to +5.5 V
Operating Temperature	0 to +70°C

Military (M) Devices*

Supply Voltage	+4.5 to +5.5 V
Case Operating Temperature	-55 to +125°C

Operating ranges define those limits between which the functionality of the device is guaranteed.

** Military product 100% tested at T_C = +25°C, +125°C, and −55°C.*

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1,2, 3 are tested unless otherwise noted).

Parameter Symbol	Parameter Description	Test Conditions	COM'L		MIL		Unit
			Min.	Max.	Min.	Max.	
I_{OH}	Output High Current	V_{OH} = 2.4 V, V_{CC} = 4.5 V	−2.0		−2.0		mA
I_{OL}	Output Low Current	V_{OL} = 0.4 V, V_{CC} = 4.5 V	+6.0				mA
V_{IH}	Input High Voltage	(Note 1)	2.0	V_{CC} + 0.5		V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage	(Note 1)		0.8		0.8	V
I_{IX}	Input Leakage Current	GND≤V_{IN} ≤ V_{CC} V_{CC} = 5.5 V	−10	10	−10	10	µA
I_{OZ}	Output Leakage Current	GND≤V_{OUT} ≤ V_{CC} V_{CC} = 5.5 V	−10	10	−10	10	µA
I_{CC1}	Static Operating Supply Current	GND≤V_{OUT} ≤ V_{CC} V_{CC} = 5.5 V (Note 2)		15		20	mA
I_{CC2}	Dynamic Operating Current, (16.7 MHz Max.)	GND≤V_{OUT} ≤ V_{CC} V_{CC} = 5.5 V (Note 2)		100		120	mA
I_{CC3}	Dynamic Operating Current, (22.5 MHz Max.)	GND≤V_{OUT} ≤ V_{CC} V_{CC} = 5.5 V (Note 2)		120		N/A	mA

Notes:

1. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. I_{CC} measurements are made with outputs open.

CAPACITANCE (Note 3) (V_{CC} = 5.0 V, T_A = 25°C, f = 1.0 MHz)

Parameter Symbol	Parameter Descriptions	Test Conditions	Typ.	Unit
C_I	Input Capacitance	V_{IN} =0 V	5	pF
C_{VO}	Input/Output Capacitance	V_{VO} = 0 V	7	

Note:

3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

AC SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherise noted*)

No. (Note 5)	Symbol	Description	COM'L 35 ns		COM'L/MIL 45 ns		Unit
			Min.	Max.	Min.	Max.	
Read Cycle Parameters							
1	t_{RC}	Read cycle time	45		60		ns
2	t_{RA}	Read Access time		35		45	ns
3	t_{RAP}	Read Access time with Parity		45		55	ns
4	t_{RPW}	Read Pulse width	35		45		ns
5	t_{RR}	Read Recovery time	10		15		ns
6	t_{OH}	Output Hold after RD	5		5		ns
7	t_{LZ}	RD Low to Output Active	5		5		ns
8	t_{HZ}	RD High to Output Disable		25		30	ns
9	t_{AH}	C/D Hold time after RD or WR	5		5		ns
10	t_{AS}	C/D Setup Time to RD or WR	5		5		ns
11	t_{RCS}	Write End to Begin Read (Note 4)	20		30		ns
Write Cycle Parameters							
12	t_{RCH}	Read End to Begin Write (Note 4)	20		30		ns
13	t_{WC}	Write Cycle Time	45		60		ns
14	t_{WP}	Write Pulse Width	20		45		ns
15	t_{DW}	Data Setup time to WR	20		30		ns
16	t_{DH}	Data Hold Time after WR	0		5		ns
17	t_{WR}	Write Recovery Time	10		15		ns
18	t_{FL}	Fall Through Time	45		60		ns
IRQ and Flag Timing							
21	t_{WLIL1}	Write low to IRQ low (FULL flag)		45		55	ns
21	t_{WLIL2}	Write low to IRQ low (AF flag)		55		75	ns
22	t_{WHIL1}	Write high to IRQ low		35		45	ns
23	t_{RHIH}	Read status high to IRQ high		35		45	ns
24	t_{RLIL1}	Read low to IRQ low (EMPTY flag)		45		55	ns
24	t_{RLIL2}	Read low to IRQ low (AE flag)		55		75	ns
25	t_{RHIL}	Read high to IRQ low		35		45	ns
26	t_{RLIH}	Read low to MB flag reset		35		45	ns
Bypass Timing							
27	t_{FLB}	Flow Through Delay (Bypass)	45		60		ns

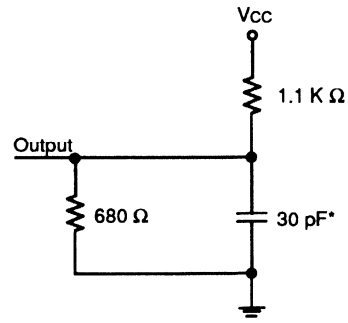
Notes:

4. This parameter refers to read/write on the same port.
5. Switching Waveforms Reference numbers.

* Subgroups 7 and 8 apply to functional tests.

AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output loads	See AC Test Load



11120-015A

* Includes jig and scope capacitances

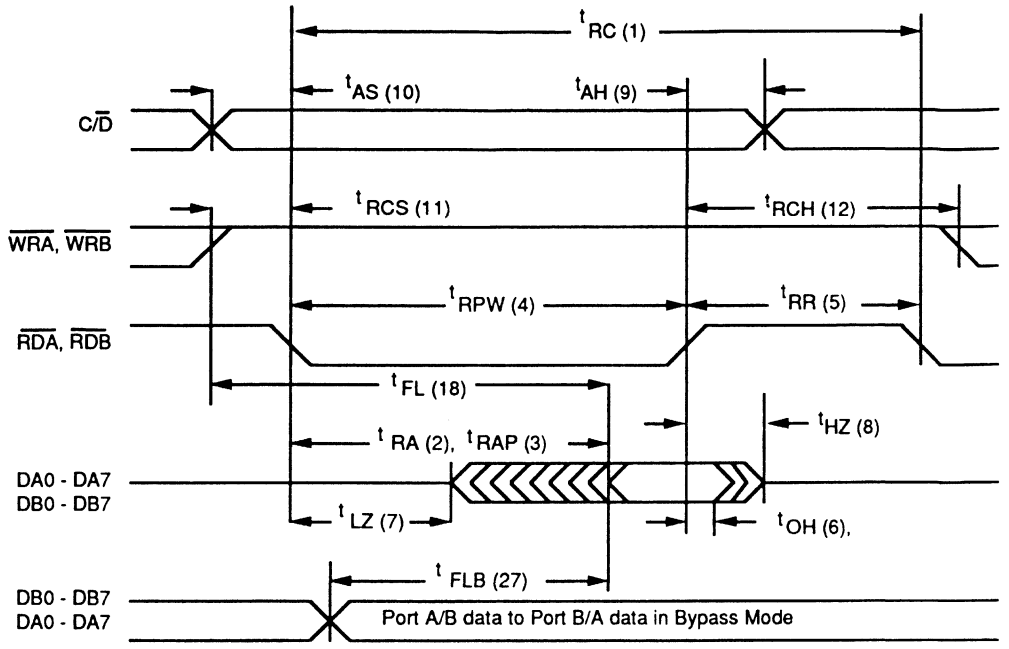
AC Test Load

KEY TO SWITCHING WAVEFORMS

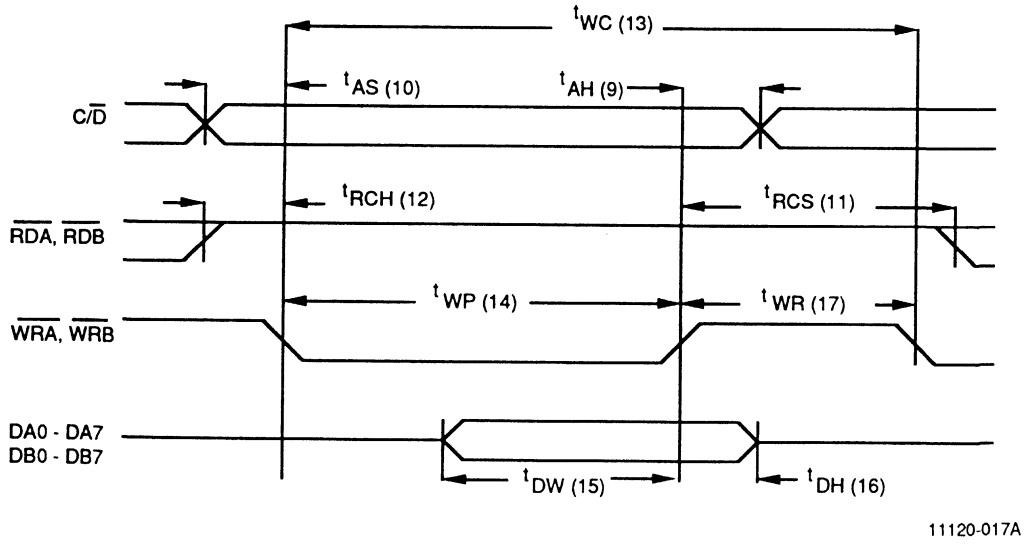
WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

KS000010

SWITCHING WAVEFORMS

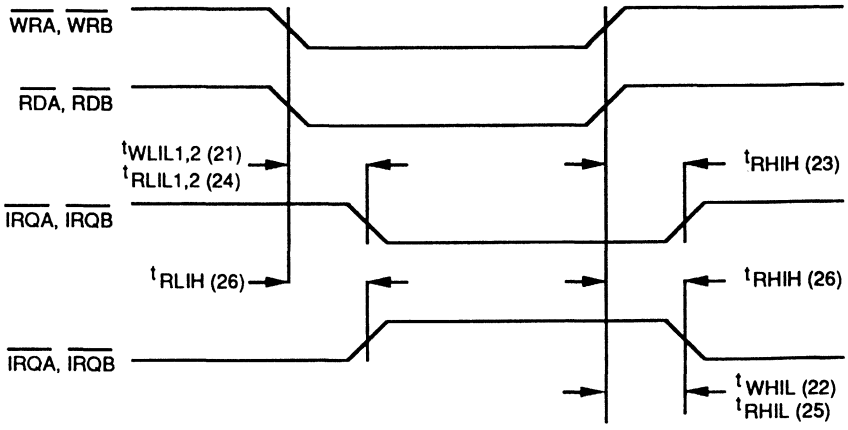


Read Timing



Write Timing

SWITCHING WAVEFORMS



11120-018A

IRQ Timing

674219

FIFO RAM Controller

Advanced Micro Devices

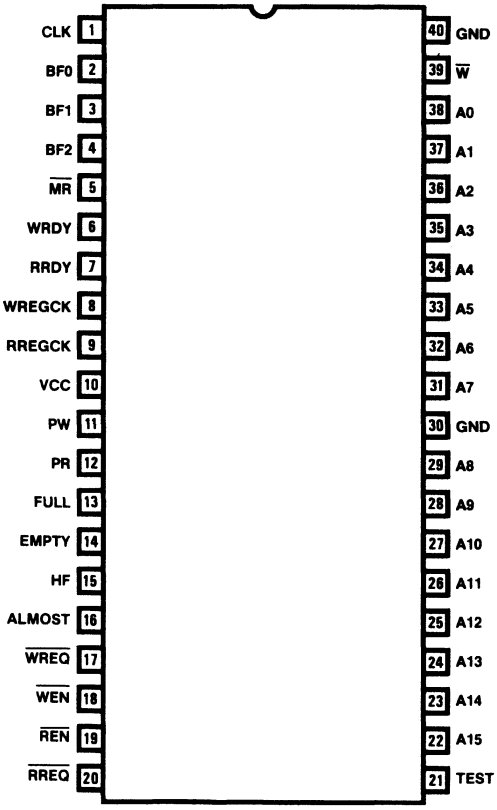
Features/Benefits

- High-speed, no fall-through time
- Deep FIFOs—16-bit SRAM address
- Arbitration read/write
- Control signals for data latching
- Full, Half-Full, Empty, Almost flags for buffer sizes from 512 to 64 K
- Three-state outputs

Applications

- LAN equipment
- Data communication
- Disk/tape controllers
- Host-to-dedicated-processor interface

Pin Configuration



Ordering Information

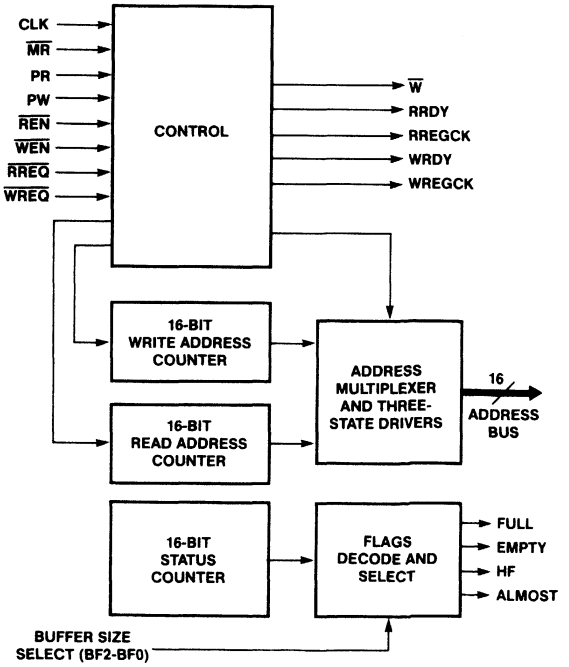
Part Number	Package		Temperature
	Pins	Type	
674219	40	CD 040	Com

Description

The 674219 FIFO RAM Controller provides addressing control, status, and arbitration for a static RAM array used as a First-In-First-Out (FIFO) buffer. The sixteen address lines can address a FIFO buffer area ranging from 512 to 65,536 static RAM words. Control signals including W (the write enable signal for the static RAMs), handshaking signals for the read and write ports, and strobes for external data latching.

The 674219 allows single-port static RAMs to resolve read and write request conflicts according to priority rules selected via the Priority-on-Read (PR) and Priority-on-Write (PW) inputs. If priority is given to either port, or if only one port is used, the maximum data rate through that port is 10 MHz.

Block Diagram



Publication# 10685 Rev. A Amendment/0
Issue Date: May 1988

Definition of Terms

LATCHED A request has been received by the 674219 on one of its ports. The request has been internally latched, but not sampled.

SAMPLED The state of a latched request when it has been internally synchronized.

PROCESSED A decision to perform a sampled request.

PERFORMED When the processed request is executed as a memory cycle.

PENDING REQUEST A sampled request that has been held until the FIFO completes its current operation(s).

WRITE DATA PORT The register(s) where the system places the data that is to be written into the FIFO.

READ DATA PORT The register(s) where the system reads the FIFO data.

WRITE DATA REGISTER The register(s) which serves as the data input to the FIFO.

READ DATA REGISTER The register(s) where the FIFO leaves the read data for the system to take.

Architecture

The 674219 FIFO RAM Controller, together with an array of static RAMs and two registers, comprises a First-In-First-Out (FIFO) memory. (See Figure 1.)

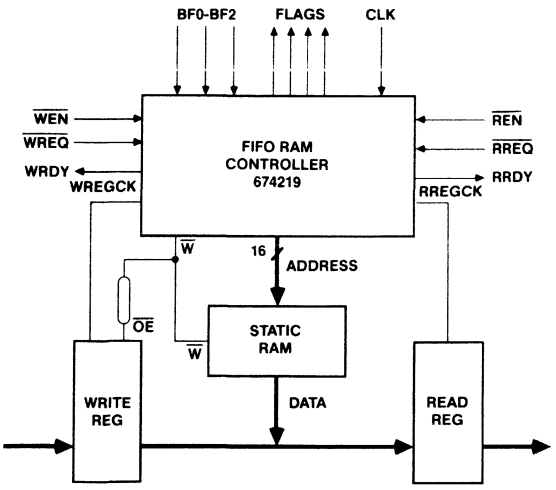


Figure 1. 57/674219 In and Implementation of a FIFO Buffer

The 674219 provides addresses and control signals to the static RAMs, and interfaces with the system via a write port, a read port, and status flags. The 674219 includes three 16-bit counters: a write-address counter, a read-address counter, and a status counter. The status flags are generated as a function of the state of the status counter and the buffer length selected. The write port has a Write REQuest ($\overline{WREQ}$) input, a Write ENable ($\overline{WEN}$) input, and a Write ReaDY (WRDY) output. The read port has a Read REQuest ($\overline{RREQ}$) input, a Read ENable ($\overline{REN}$) input, and a Read ReaDY (RRDY) output. Two priority-control inputs, Priority-on-Write (PW) and Priority-on-Read (PR), determine the priority rules by which the 674219 arbitrates between simultaneous read and write requests. The 674219 provides two clock signals (RREGCK, WREGCK) to the Read Data Register and the Write Data Register, as well as a Write signal ($\overline{W}$) to be connected to the Write Enable ($\overline{WE}$) inputs of the static RAMs. Sixteen address outputs provide the read and write addresses to the static RAMs. When both $\overline{REN}$ and $\overline{WEN}$ are HIGH, the address outputs go into high-impedance (Hi-Z) state, so that the static RAMs can be accessed externally.

A Master Reset ($\overline{MR}$) input allows initializing the part by clearing the three counters and presetting the flags. (See Table 1.)

FLAG	CONDITION
Empty	High
Full	Low
Almost	High
Half	Low

Table 1. Condition of Flags After Master Reset

Pin Definitions

V_{CC} 5.0 V ± 10%

GND Ground

CLK CLOCK—Controls synchronous operation of the device. All requests are sampled internally on every other LOW-to-HIGH transition of the clock. These transitions are called sampling clock edges. The first sampling clock edge is the first LOW-to-HIGH transition of the clock after master reset.

BF2-BF0 BUFFER SIZE CONTROLS—Determine the desired buffer size. (See Table 3.) Setting the buffer size is essential for correct operation of the status flags.

$\overline{MR}$ MASTER RESET—Clears all counters when LOW. The first LOW-to-HIGH transition of the clock, following a LOW-going Master Reset pulse, is the first sampling clock edge; the first request to be serviced is a write request. (See Figure 7.)

A15-A0 ADDRESS OUTPUTS—Three-state outputs which provide a read address when $\overline{W}$ is HIGH, or a write address when $\overline{W}$ is LOW. A15-A0 are in the Hi-Z state only when both $\overline{REN}$ and $\overline{WEN}$ are HIGH.

TEST An input used during manufacturing final test. For normal operation, TEST should be tied to GND.

$\overline{W}$ WRITE CONTROL—Used to control the SRAM arrays Write Enable pin and to output enable the write data register.

$\overline{WREQ}$ WRITE REQUEST—A LOW-going pulse on this pin requests a write to the FIFO. A write request can only be latched if the write port is enabled ($\overline{WEN}$ is LOW), and the previous write request has been processed (WRDY is HIGH).

$\overline{RREQ}$ READ REQUEST—A LOW-going pulse on this pin requests a read from the FIFO. A read request can only be latched if the read port is enabled ($\overline{REN}$ is LOW), and the previous read request has been processed (RRDY is HIGH).

$\overline{WEN}$ WRITE ENABLE—When this input is HIGH, all write requests are ignored. When $\overline{WEN}$ is LOW and WRDY is HIGH, a write request ($\overline{WREQ}$ = LOW-going pulse) will be latched by the 674219. If both $\overline{WEN}$ and $\overline{REN}$ are HIGH, the address outputs A15-A0 go into the Hi-Z state, permitting external access to the SRAM array.

$\overline{REN}$ READ ENABLE—When this input is HIGH, all read requests are ignored. When $\overline{REN}$ is LOW and RRDY is HIGH, a read request ($\overline{RREQ}$ = LOW-going pulse) will be latched by the 674219. If both $\overline{WEN}$ and $\overline{REN}$ are HIGH, the address outputs A15-A0 go into the Hi-Z state, permitting external access to the SRAM array.

PW, PR WRITE PRIORITY and READ PRIORITY—These two inputs determine the rules governing the arbitration between write and read requests. (See Table 2.) *These inputs must not both be HIGH simultaneously.*

WRDY WRITE READY—When this output is HIGH, and $\overline{WEN}$ is LOW, a write request may be sent to the $\overline{WREQ}$ pin.

WRDY goes LOW on the sampling clock edge which samples the write request. WRDY will go HIGH on the non-sampling clock edge which starts the write cycle. WRDY will stay LOW if the FIFO is full.

Write requests should be made only when WRDY is HIGH.

RRDY READ READY—When this output is HIGH, and $\overline{REN}$ is LOW, a read request may be sent to the $\overline{RREQ}$ pin.

RRDY goes LOW on the sampling clock edge which samples the read request. RRDY will go HIGH on the non-sampling clock edge which starts the read cycle. RRDY will stay LOW if the FIFO is empty.

Read requests should be made only when RRDY is HIGH.

WREGCK WRITE REGISTER CLOCK—This output is used to clock the write data register.

RREGCK READ REGISTER CLOCK—This output is used to clock the read data register.

EMPTY EMPTY FLAG—When HIGH, indicates that the FIFO is empty. Read requests are not permitted when the FIFO is EMPTY.

FULL FULL FLAG—When HIGH, indicates that the FIFO is full. Write requests are not permitted when the FIFO is FULL.

HF HALF-FULL FLAG—When HIGH, indicates that the FIFO has half, or more, of its locations occupied.

ALMOST ALMOST FLAG—When HIGH, indicates that one of the following conditions exists:

1. The FIFO is almost empty (less than sixteen words in the FIFO), if ALMOST is HIGH and HF is LOW.
2. The FIFO is almost full (sixteen or less locations are available) if ALMOST is HIGH and HF is HIGH.

Requests, Arbitration and Data Capture

A clock, supplied via the CLK input of the 57/674219, generates the internal sequence of events which constitutes a single FIFO operation. The read and write ports recognize and latch read and write requests asynchronously, provided that the respective enable ($\overline{REN}$ or $\overline{WEN}$) is LOW, and the request window setup time is observed.

The FIFO *write* operation is as follows (see Figure 2):

Stage 1 A write request is sent to the 674219 by a LOW-going pulse on the $\overline{WREQ}$ pin.

Stage 2 The write request is latched internally, asynchronous to the clock.

Stage 3 WRDY goes LOW on the sampling clock edge that latched the request to indicate to the system that the request has been latched and synchronized internally. WRDY also indicates to the system that the write port is no longer accepting write requests. In order to guarantee that a request is properly synchronized, the request must not occur during the window stated by the tWRQC specifications.

Stage 4a Regardless of whether the write cycle is started or not, WREGCK will go HIGH for one clock cycle on the non-sampling clock edge that follows WRDY going LOW. The transition from LOW-to-HIGH on the WREGCK pin clocks data into the write data port, reading the data for writing to the SRAM.

Stage 4b A decision to wait, or to perform the write cycle is made based on the following:

Case 1 If read priority is set, the 674219 will process all pending read requests first. The write cycle will be delayed until all of the read cycles have been performed. Then, and only then, will the pending write cycle be performed.

Case 2 If write priority is set, regardless if there is a pending read request or not, the write cycle will start on the next non-sampling clock edge that follows WRDY going LOW. If there was a pending read request, the read cycle will not be started until the write cycle has been completed.

Case 3 If no priority is set, and there is no pending read request, the FRC will start the write cycle on the next non-sampling clock edge that follows WRDY going LOW.

Case 4 If no priority is set, and there are simultaneous requests (i.e., a read request and a write request have both been latched before the same sampling clock edge), the FIFO will decide which is to be processed first according to the following:

If the last case of simultaneous requests (with no priority) performed a read cycle first, the write request will be processed first, followed by the read request.

If the last case of simultaneous requests (with no priority) performed a write cycle first, the read request will be processed first, followed by the write request.

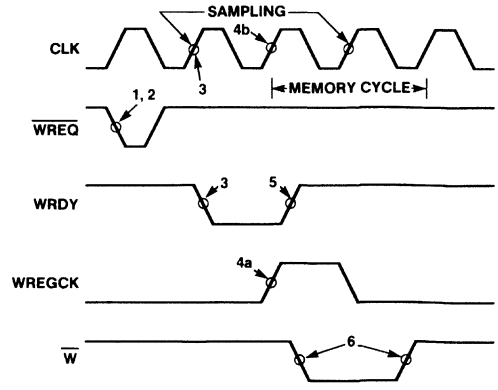


Figure 2. The Stages of a FIFO Write Operation

Stage 5 WRDY will go HIGH on the non-sampling edge that starts the write cycle.

Stage 6 Once a request has been granted, the memory cycle takes place over two clock cycles, starting with the non-sampling clock edge on which the request is granted (WRDY going from LOW-to-HIGH). The Write line ($\overline{W}$) goes LOW at tCWL after the clock edge starting the memory cycle and stays low until tCWH after the clock edge terminating the memory cycle.

The FIFO *read* operation is as follows (see Figure 3):

Stage 1 A read request is sent to the 674219 by a LOW-going pulse on the $\overline{RREQ}$ pin.

Stage 2 The read request is latched internally, asynchronous to the clock.

Stage 3 RRDY goes LOW on the sampling clock edge that latched the request to indicate to the system that the request has been latched and synchronized internally. RRDY also indicates to the system that the read port is no longer accepting read requests. In order to guarantee that a request is properly synchronized, the request must not occur during the window stated by the tRRQC specifications.

Stage 4 A decision to wait, or to perform the read cycle is made based on the following:

Case 1 If write priority is set, the 674219 will process all pending write requests first. The read cycle will be delayed until all of the write cycles have been performed. Then, and only then, will the pending read cycle be performed.

Case 2 If read priority is set, regardless if there is a pending write request or not, the read cycle will start on the next non-sampling clock edge that follows RRDY going LOW. If there was a pending write request, the write cycle will not be started until the read cycle has been completed.

Case 3 If no priority is set, and there is no pending write request, the FRC will start the read cycle on the next non-sampling clock edge that follows RRDY going LOW.

Case 4 If no priority is set, and there are simultaneous requests (i.e., a read request and a write request have both been latched before the same sampling clock edge), the FIFO will decide which is to be processed first according to the following:

1. If the last case of simultaneous requests (with no priority) performed a read cycle first, the write request will be processed first, followed by the read request.
2. If the last case of simultaneous requests (with no priority) performed a write cycle first, the read request will be processed first, followed by the write request.

Stage 5 RRDY will go HIGH on the non-sampling edge that starts the write cycle.

Stage 6 Once a request has been granted, the memory cycle takes place over two clock cycles, starting with the non-sampling clock edge on which the request is granted (RRDY going from LOW-to-HIGH). Read REGister Clock (RREGCK) goes LOW for one clock cycle, starting with the sampling edge that occurred within the read memory cycle. RREGCK clocks data from the SRAM array to the read data port on the LOW-to-HIGH transition, which terminates the read cycle.

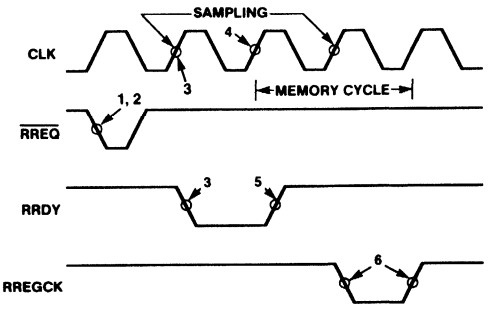


Figure 3. The Stages of a FIFO Read Operation

Priority

Two input signals, Priority-on Read (PR) and Priority -on-Write (PW), determine the arbitration rule which sequences the read and write cycles, for various cases as follows: (see Table 2):

PW	PR	PRIORITY
0	0	No priority
0	1	Priority on READ
1	0	Priority on WRITE
1	1	(Not allowed)

Table 2. Priority Encoding

No-Priority Case

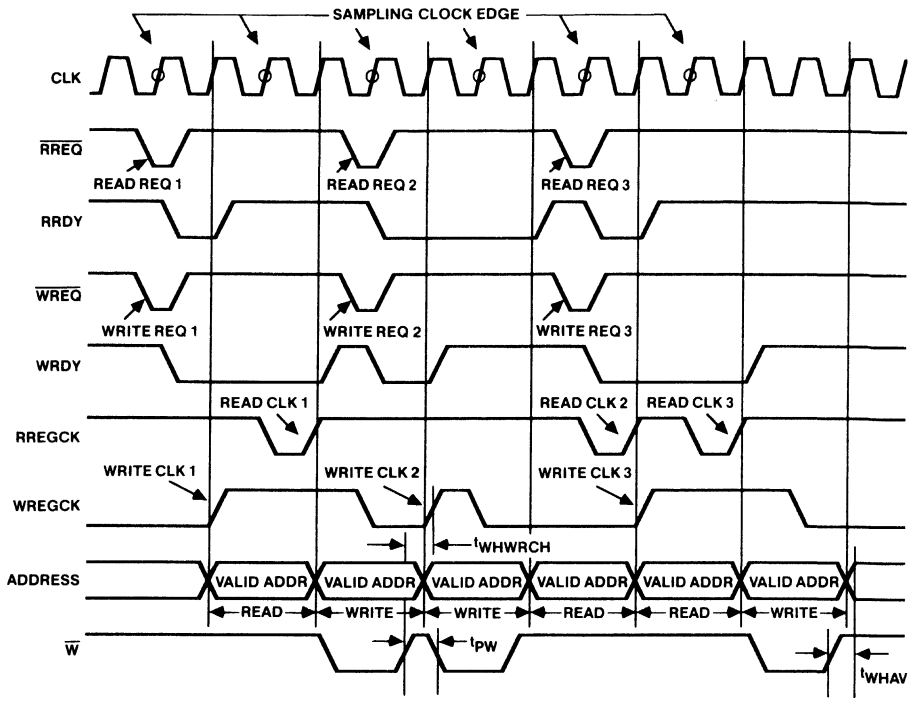
If no priority is selected (PR = PW = LOW), each request is processed in the order it came into the FRC.

If no priority is set and both a read and write request are latched before the same sampling clock edge, the 674219 will perform read and write cycles alternately. (See Figure 4.)

Write Priority Case

If write priority is selected (PR = LOW, PW = HIGH) write requests are always processed before read requests (assuming that the requests meet the setup time).

If write priority is set and both a read and write request are latched before the same sampling clock edge, (i.e., a simultaneous request), the write cycle will take place first. If, before the next sampling clock edge, another write request is latched, another write cycle will take place, and the pending read request will not be processed. Only when the sampling clock edge encounters no further write requests will the pending read request be processed. At this time the read cycle will start and the RRDY output will go HIGH. (See Figure 5.)



Notes: 1. Assumes not at FULL and not at EMPTY.
2. Assumes last case of simultaneous requests processed a write first.

Figure 4. Operation With No Priority

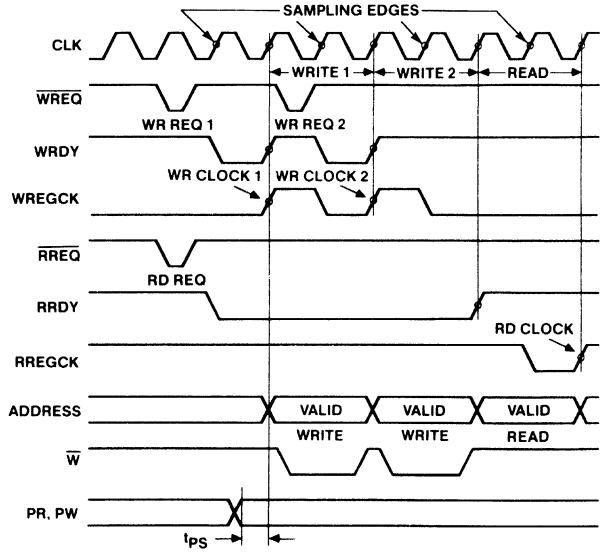


Figure 5. Operation With Write Priority

Read Priority Case

If read priority is selected (PR = HIGH, PW = LOW) read requests are always processed before write requests assuming that the requests meet the setup time).

If read priority is set and both a read and write request are latched before the same sampling clock edge, (i.e., a simultaneous request), the read cycle will take place first. If, before the next sampling clock edge, another read request is latched, another read cycle will take place and the pending write request will not be processed. Only when the sampling clock edge encounters no further read requests will the pending write requests be processed. At this time, the write cycle will start and the WRDY output will go HIGH. (See Figure 6.)

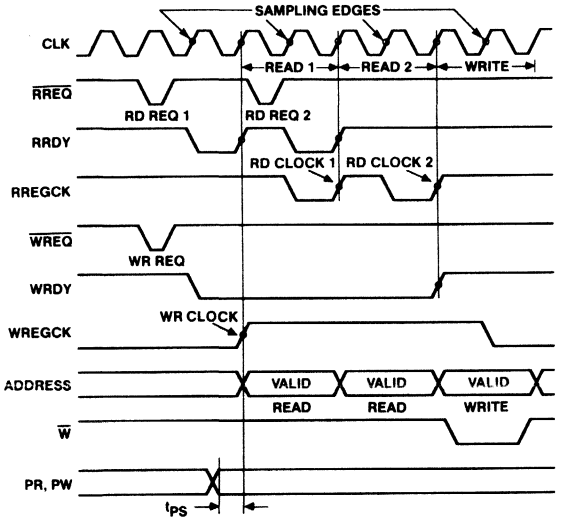


Figure 6. Operation With Read Priority

Buffer Length

A three-bit input control field, BF2-0, selects the buffer length ("depth") of the FIFO. Any power of 2 from 512 to 65,536 may be chosen as the buffer length. (See Table 3.)

BF2	BF1	BF2	BUFFER SIZE
0	0	0	512
0	0	1	1024
0	1	0	2048
0	1	1	4096
1	0	0	8192
1	0	1	16384
1	1	0	32768
1	1	1	65536

Table 3. Buffer Length

Status Flags

The flags are generated as a function of the buffer length, selected via inputs BF2-BF0, and the state of the status counter. The status flags are:

EMPTY When HIGH, the EMPTY flag indicates that the FIFO is empty. The EMPTY flag goes HIGH on the first sampling clock edge during the memory cycle which empties out the FIFO.

FULL When HIGH, the FULL flag indicates that the FIFO is full, and no more data can be written into it until a read cycle takes place. The FULL flag goes HIGH on the first sampling clock edge during the memory write cycle which fills up the FIFO.

HF When HIGH, the Half-Full flag indicates that the FIFO is filled to half its depth, or more.

ALMOST When HIGH, the ALMOST flag indicates that one of the following conditions exists:

1. The FIFO is almost empty (less than sixteen words in the FIFO), if ALMOST is HIGH and HF is LOW.
2. The FIFO is almost full (sixteen or less locations are available) if ALMOST is HIGH and HF is HIGH.

The flags Master Reset to the states shown in Table 1.

First Write Cycle (After a Master Reset or When FIFO is Empty)

The first LOW-to-HIGH clock edge, following Master Reset ($\overline{MR}$) going LOW-to-HIGH, is the first sampling clock edge. The sampling clock edge occurs every other positive-going transition of the clock. The LOW pulse on $\overline{MR}$ clears the three internal 16-bit counters (status, read and write). The FIFO is set to the EMPTY state, and no read requests are allowed (RRDY = LOW).

After an interval of at least tMRS after $\overline{MR}$ goes HIGH, a LOW-going pulse on the $\overline{WREQ}$ pin tells the 674219 that a write to the FIFO is requested. The write request is latched by the write port, provided that $\overline{WEN}$ is LOW. (See Figure 7.) The following sampling clock edge samples the request, and causes WRDY to go LOW. WRDY goes HIGH again on the next (non-sampling) positive clock edge, regardless of priority. The write cycle takes place over two clock periods, starting on the positive non-sampling clock edge following the sampling clock edge which brought WRDY HIGH. The data is clocked into the external Write Data Register on the same non-sampling clock edge, and into the external Read Data Register on the second sampling clock edge, to allow minimal fall-through time. (See again Figure 7.) EMPTY will go LOW to indicate that there is valid data in the FIFO. RRDY goes HIGH indicating that there is data to be read from the FIFO. The same sequence of events occurs for the first write request that is initiated when the FIFO is empty.

Methodology for Reading

In order to maintain a consistent system level architecture, the 674219 has been constructed such that the system should read the data port *before* a read request is sent. (See Figure 8.)

This ability allows the FIFO a zero fall-through time on all cycles. The system is able to get the data from the FIFO right away, without having to wait for the FRC to perform a read cycle of the SRAMs.

On the read port, a positive-going edge of RREGCK signals to the system that the read data register is being updated. The system should read the data first and then send a request to obtain the next word from memory to the read data register.

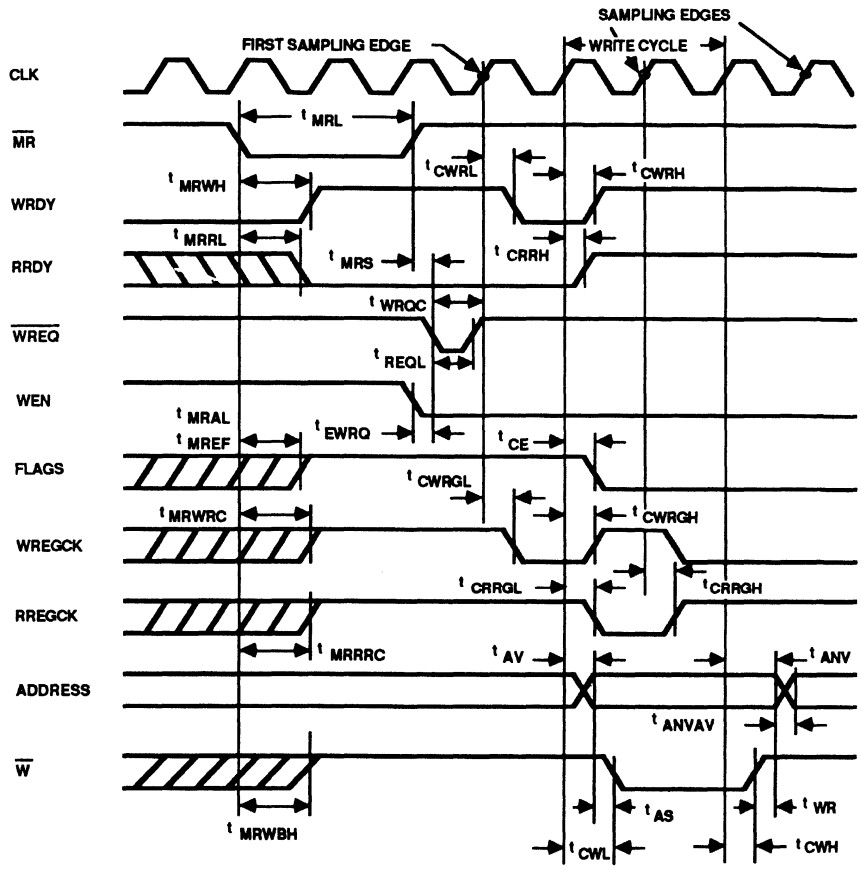


Figure 7. First Write After Master Reset or When FIFO Is Empty

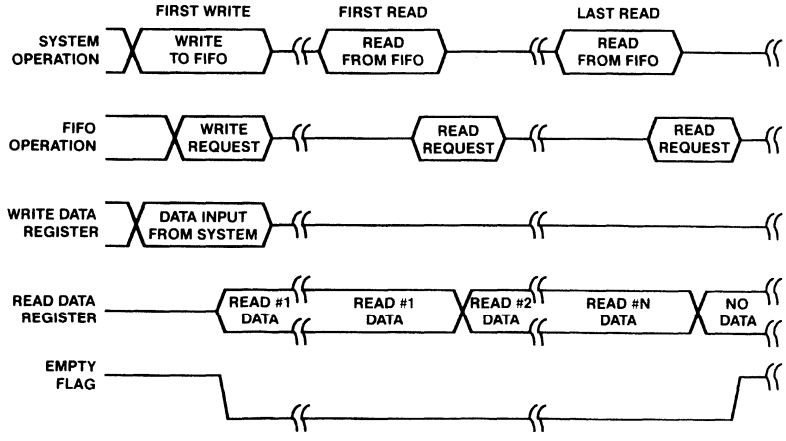


Figure 8. Methodology for Reading From the FIFO

Write Cycle (Figure 9)

A write request, indicated by a LOW-going pulse on the $\overline{WREQ}$ pin, is latched by the 674219, provided that $\overline{WEN}$ is LOW and WRDY is HIGH. The request is sampled internally on the sampling clock edge. WRDY goes LOW on the same sampling clock edge, to indicate to the system that a write request has been latched and synchronized internally. In addition, WREGCK will go HIGH for one clock cycle on the non-sampling clock edge that follows WRDY going LOW, regardless of whether the write request is processed. The write request will be processed only if one of the following sets of conditions is true:

1. Write Priority has been selected.

   If write priority has been selected, the FRC will process all write requests before any pending read requests.

2. No read request has been latched.

   If no read request has been latched, regardless of priority, the FRC will process the write request immediately and will start the write memory cycle on the non-sampling clock edge that follows WRDY going LOW.

3. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the read request first.

   In this case, the 674219 will process the write request first, and then process the read request.

4. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the write request first.

   In this case the 674219 will process the read request first, and then process the write request.

Once the write request has been processed, a write cycle takes place over two clock cycles starting with the non-sampling clock edge on which WRDY goes HIGH. $\overline{W}$ will go LOW, tCWL after the start of the write cycle. $\overline{W}$ is used to Write Enable the SRAM array and to Output Enable the write data register. Two clocks later (tCWH) $\overline{W}$ will go HIGH again, terminating the write cycle.

In order to avoid the bus contention inherent in shared-I/O memory systems, a delay line and an OR gate may be required (see Memory Interface Design Guidelines).

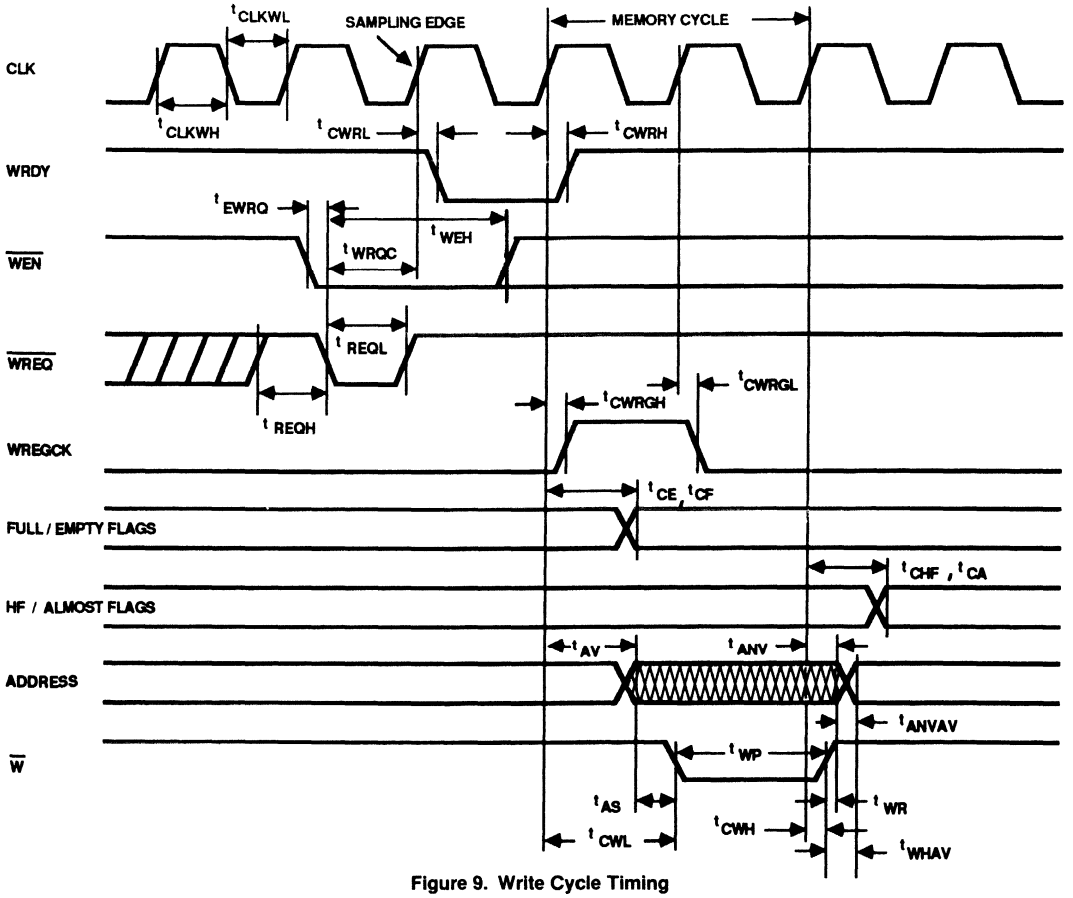


Figure 9. Write Cycle Timing

Read Cycle (Figure 10)

A read request, indicated by a LOW-going pulse on the $\overline{\text{RREQ}}$ pin, is latched by the 674219, provided that $\overline{\text{REN}}$ is LOW and RRDY is HIGH. The request is sampled internally on the sampling clock edge. RRDY goes LOW on the same sampling clock edge to indicate to the system that a read request has been latched and synchronized internally. The read request is processed only if one of the following sets of conditions is true:

1. Read Priority has been selected.

   If read priority has been selected, the FRC will process all read requests before any pending write request.

2. No write request has been latched.

   If no write request has been latched, regardless of priority, the FRC will process the read request immediately and will start the read memory cycle on the non-sampling clock edge that follows RRDY going LOW.

3. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the write request first.

   In this case, the 674219 will process the read request first.

4. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the read request first.

   In this case, the 674219 will process the write request first, and then process the read request.

Once the read request has been processed, a read cycle takes place over two clock cycles starting with the non-sampling clock edge on which the RRDY goes HIGH. RREGCK goes LOW on the next sampling clock edge, stays LOW for one clock cycle, and goes HIGH on the following non-sampling clock edge, thus clocking the data which appears at the SRAM array's data outputs into the Read Data Register. RREGCK going HIGH terminates the read cycle.

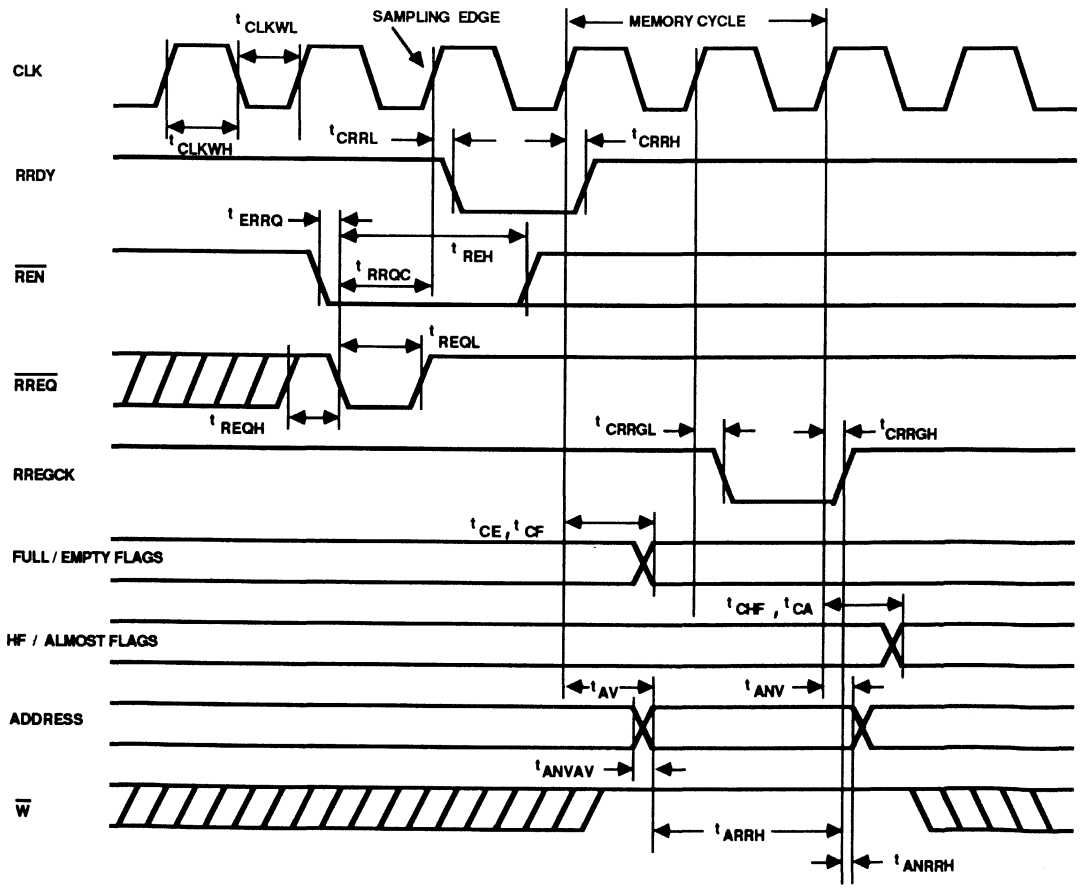


Figure 10. Read Cycle Timing

Memory Interface Design Guidelines

Introduction

The purpose of the memory interface design guideline is to aid the engineer in interfacing the 674219 FIFO RAM Controller (FRC) to an array of static RAMs. This guideline will be broken down into three separate sections. The first section is a timing analysis of the read cycle. The second section is a timing analysis of the write cycle. The final section will guide the designer through a real design.

Figure 11 shows a typical SRAM interface schematic.

Section One: Read Cycle Timing Analysis

Figure 12 shows the basic timings which are critical to the read cycle. Some of these parameters apply to the FRC, some to the SRAM array, and others to external logic. For convenience, these parameters are broken up below:

FRC Parameters:

t_{AV}	Clock to Address Valid Time
t_{ANV}	Clock to Address Not Valid Time

SRAM Parameters

t_{RC}	Read Cycle Time
t_{ACS}	Chip Select Access Time
t_{AA}	Address Access Time
t_{OH}	Output Data Hold Time from Address Change
t_{HZ}	Chip Deselect to Output in High-Z

External Logic:

Chip Select Decoder Parameters:

t_{DECODE}	t_{PD} through Decoder

Read Data Register Parameters:

t_S	Data Setup Time
t_H	Data Hold Time

Other Parameters (See Text):

t_{RDREGH}	Clock to RDCLK High [RDCLK is the clock input of the Read Data Register]

(This parameter is normally t_{CRRGH} of the FRC)

There are six separate equations which must each be met in order to determine what speed of SRAM the designer will need. It is assumed that the user has already specified a speed of operation and the external components needed. The equations listed can be used at any frequency, up to a maximum of a 20-MHz clock rate.

Since every read cycle consists of two physical clock cycles, all equations are with respect to 2T (2 x Cycle Time).

The first equation which should be satisfied is the read cycle time (tRC). This identifies what speed SRAM is required. The equation is based on the total time that the address is valid minus the decoder time. Since the decoder has some minimum skew on the negating edge, this time is ADDED to the equation. The equation thus becomes:

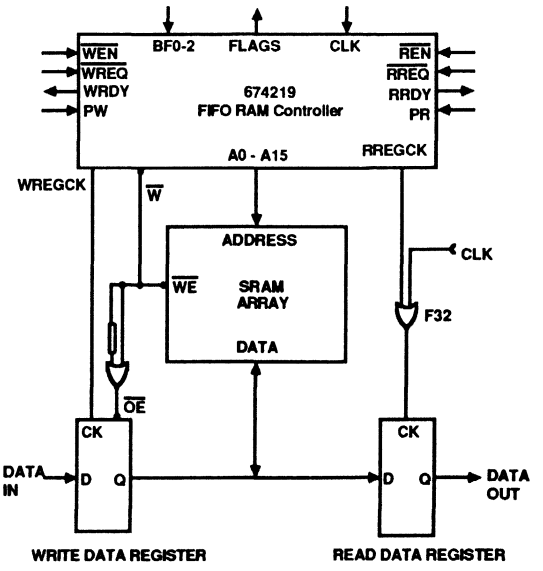


Figure 11. A Typical SRAM Interface

Equation 1-1

$$t_{RC} \leq 2T - t_{DECODE(max)} + t_{DECODE(min)} - t_{ANVAV(max)}$$

The access time must be looked at next. There are actually two separate equations that help determine the access time.

Equation 1-2 determines the address access time (tAA). tAA is based on the time that the address is valid before the read register gets clocked. The equation takes into account the setup time of the read data register (tS) as well. The equation is:

Equation 1-2

$$t_{AA} \leq 2T - MAX(t_{AV} - t_{RDREGH}) - t_{S(min)}$$

Where $MAX(t_{AV} - t_{RDREGH})$ is the maximum difference between t_{AV} and t_{RDREGH}

Equation 1-3 determines the chip select access time (tACS). This time is based on the time the address is valid before the read register gets clocked MINUS the maximum skew through the chip select decoder. This is done to ensure that the decoder delay is taken into consideration. Again, the read register setup time is considered. The modified equation thus becomes:

Equation 1-3

$$t_{ACS} \leq 2T - t_{DECODE(max)} - MAX(t_{AV} - t_{RDREGH}) - t_{S(min)}$$

Where $MAX(t_{AV} - t_{RDREGH})$ is the maximum difference between t_{AV} and t_{RDREGH}

The next two equations take into consideration the read data hold time with respect to the address (tOH), and the chip deselect to data outputs in High-Z time (tHZ). We will consider the more critical tOH. tOH can easily be determined by comparing the data hold time PLUS the clock to address not valid (tANV) time with the sum of the clock to RDCLK HIGH time (tRDREGH) and the data register hold time (tH). The equation for this becomes:

Equation 1-4

$t_{OH(min)} + t_{ANV(min)} \geq t_{RDREGH(max)} + t_{H(min)}$

If the SRAM has an extraordinarily long read data hold time (tOH), the above equation must be modified to include the now more critical chip deselect to data outputs in High-Z time (tHZ). This is done by simply substituting tHZ for tOH. The modified equation is:

Equation 1-5

$t_{HZ(min)} + t_{ANV(min)} \geq t_{RDREGH(max)} + t_{H(min)}$

In addition to the above equations, one more is necessary in certain cases. In Figure 12, the read cycle is shown. At the very end of a read cycle, the read data register is clocked. The normal clocking signal for the FRC is RREGCK. Since the read data register's clock is normally connected to RREGCK, if RREGCK goes HIGH after the data from the SRAMs goes away, the data will be lost. This is only true if the SRAMs have a low tOH(min). Normally, in all of the above equations, the clock to RREGCK HIGH (tCRRGH) is substituted in place of tRDREGH. In the cases where a low tOH does not guarantee the data will be properly clocked, the user has another alternative.

By adding an external OR gate between the clock and RREGCK, the user can effectively shorten tCRRGH(max). The gate "ANDs" the active LOW RREGCK with the clock when it is LOW. This produces an active LOW output signal called RDCLK (see Figure 12). This will bring the edge of read register clock into specification for any tOH, even one of zero. Figure 11 shows a typical example of a SRAM interface, including this gate, should it be necessary.

Because the OR gate inherently has some delay, an equation is necessary to calculate the new tCRRGH. (This "new" parameter is called tRDREGH). It should be noted that if the designer finds it necessary to implement this logic, due to a low tOH, he/she must replace the tRDREGH in Equation 1-1 through 1-5 with the result from the following equation, rather than the normal tCRRGH. The equation for the gate is:

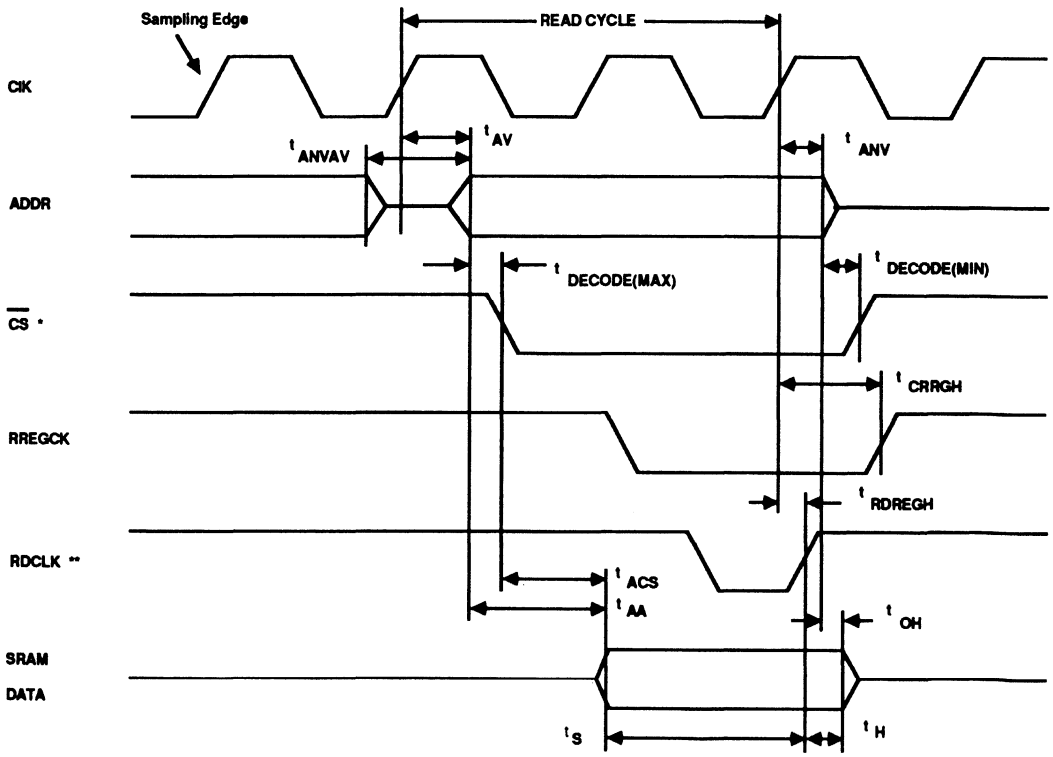
Equation 1-6

$t_{RDREGH\ (max)} = t_{PDOR\ (max)}$

Where $t_{PDOR(max)}$ is the maximum t_{PD} through the OR gate.

Since the clock will bring RDCLK low some tPDOR(max) later, the setup time of the read data register is automatically achieved.

The above equations complete the timing analysis for a read cycle. Once the user has gone through both the read and write cycle timings, an appropriate Static RAM may be chosen.



* CS to the Static RAM bank
** Actual clock input to the Read Data Register. This may be the same as RREGCK or may be the output of the OR-gate shown in Figure 1

Figure 12. Read Cycle Timing

Section Two: Write Cycle Timing Analysis

Figure 13 shows the basic timings which are critical to the write cycle. Some of these parameters apply to the FRC, some to the Static RAM array, and others to external logic. The parameters that are unique to the write cycle will be summarized below:

FRC Parameters:

t_{PW}	Write Pulse Width HIGH
t_{WHAV}	$\overline{W}$ HIGH to Address Valid
t_{ANVAV}	Address Not Valid to Address Valid
t_{WHWRCH}	$\overline{W}$ HIGH to WREGCK HIGH

SRAM Parameters

t_{WC}	Write Cycle Time
t_{AW}	Address Valid to End of Write
t_{CW}	$\overline{CS}$ to End of Write
t_{WP}	$\overline{WE}$ Pulse Width LOW
t_{DW}	Data Valid to End of Write
t_{WZ}	$\overline{WE}$ LOW to Outputs in High-Z

External Logic:

Write Data Register Parameters:

t_{PZ}	$\overline{OE}$ to Outputs in Low-Z
t_{CP}	Clock to Outputs Valid

Other Parameters (See Text):

t_{WOE} $t_{DLY(max)} + t_{ORSKEW(max)}$

There are six equations which must determine the write cycle specifications for the Static RAM. It is assumed that the user has already selected the frequency of operation and the external components needed for his/her system.

Since every write cycle consists of two physical clock cycles, all equations are with respect to 2T (2 x Cycle Time).

The first equation which should be looked at is the write cycle time (tWC). This equation will determine what speed of SRAM is required for proper operation. This parameter is the same as the total time that the address is valid. This is calculated with the following equation:

Equation 2-1

$t_{WC} \leq 2T - t_{ANVAV(max)}$

There are three basic areas to be looked at once the write cycle time has been determined. The first is the access time of the SRAM. There are two separate equations in this area.

The first parameter to be analyzed is the time from address valid to the end of write (tAW). This parameter can be calculated by taking the total write cycle time (2T) and subtracting from it, the time from $\overline{W}$ going HIGH to the next address becoming valid. The equation is:

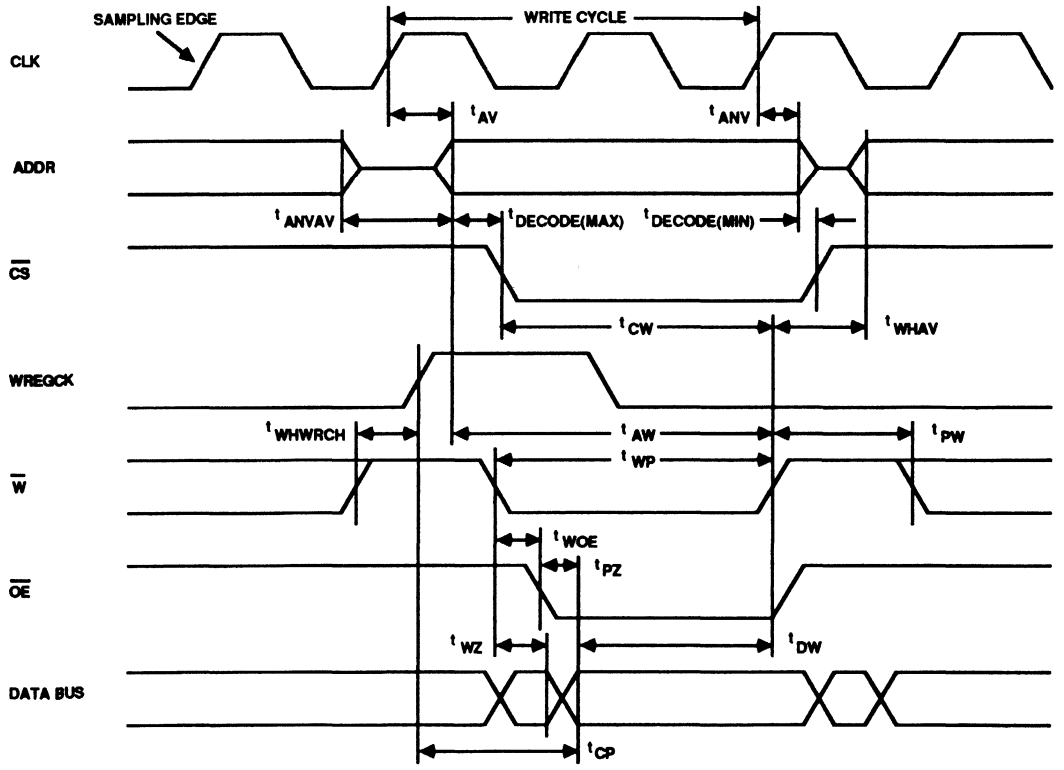


Figure 13. Write Cycle Timing

Equation 2-2

$t_{AW} \leq 2T - t_{WHAV(max)}$

The designer must also check the chip select to end of write time (tCW). This is often more critical than tAW in determining which SRAM to use in the system. The tCW parameter can be obtained in the same way as tAW except that the decode time is also included in the equation. The modified equation is:

Equation 2-3

$t_{CW} \leq 2T - t_{WHAV(max)} - t_{DECODE(max)}$

In addition to the various access times of the write cycle, the user must next look at the pulse width of the write signal (tWP). This is basically the difference between 2T and the FRC's write time HIGH (tPW). The equation is:

Equation 2-4

$t_{WP} \leq 2T - t_{PW(max)}$

The last area that needs to be analyzed is the data setup time of the SRAM. The data setup time is specified as the time data is valid before write goes HIGH (tDW).

There are three separate equations which determine the required tDW of the SRAM.

The write register has a certain propagation delay from its clock input pulse before the data becomes valid. Data must be valid at least tDW before $\overline{WE}$ goes HIGH or it will be lost. The equation takes into account the clock to output time (tCP) of the write register. The equation is:

Equation 2-5

$t_{DW} \leq 2T - t_{CP(max)} - t_{WHWRCH(max)}$

The write data register is enabled by the $\overline{W}$ signal of the FRC. The register takes some minimum time before it enables its outputs from the High-Z state (tPZ).

The SRAMs have some maximum time in which they disable their outputs when the $\overline{WE}$ signal goes LOW. This parameter is the time from $\overline{WE}$ LOW to the data outputs in High-Z (tWZ).

If tWZ(max) is greater than tPZ(min), bus contention will result. To counter this problem a delay must be introduced between the W signal of the FRC and the $\overline{OE}$ input of the write data register. In addition, an OR gate is used to bring $\overline{OE}$ HIGH shortly after $\overline{W}$ goes HIGH. This is illustrated in Figure 11. tWOE(max) is the total delay between $\overline{W}$ going LOW and $\overline{OE}$ going LOW. It is calculated by the following equation:

Equation 2-6

$t_{WOE(max)} = t_{DLY(max)} + t_{PDOR(max)}$

Where $t_{DLY(max)}$ is the maximum delay through the delay line.

$t_{PDOR(max)}$ is the maximum propagation delay through the OR gate.

Equation 2-5 dictated the tDW based on the clock to output time of the register. In most cases though, this time is automatically guaranteed. Since the data will not be valid (Low-Z) until some tPZ after $\overline{OE}$ goes LOW, even though it has been clocked properly, a new equation is necessary to determine the tDW of the SRAM. This equation must take into account the delay that was added in to prevent bus contention. It must also take into account the tPZ time of the register. The equation is very similar to Equation 2-5 with those exceptions. The equation thus becomes:

Equation 2-7

$t_{DW} \leq 2T - t_{PW(max)} - t_{PZ(max)} - t_{WOE(max)}$

One additional equation is required to determine the delay line required to prevent bus contention. The equation for the delay line takes into account the maximum tPD through the OR gate. The equation is based on the tWZ of the SRAM and the tPZ of the write data register. The equation is:

Equation 2-8

$t_{DLY(min)} = t_{WZ(max)} - t_{PZ(min)} - t_{OR(min)}$

The above equations complete the timing analysis of the write cycle. Once the user has gone through both the read and write cycle timings, an appropriate Static RAM may be chosen.

An Example Interface

In order to determine any Static RAM parameters, the user must know several things. He/she must identify the frequency of operation, the read and write data registers, the chip select decoder, and any other logic which may be necessary.

As an example, assume that a 5-MHz data throughput is desired. This will allow a 10-MHz all read or all write data rate. This data rate dictates a 20-MHz clock speed for the FRC.

For worst case design, assume that the selected SRAM has a tOH of zero. Since tOH = 0 ns, there must be an external OR-gate to clock the read register. In addition, assume that the selected SRAM has a $t_{WZ(max)} \leq 20$ ns.

In order to resolve any bus contention a delay line and another OR gate will be added.

74F series parts are used to keep the design clean. It should be noted that the user can use any kind of logic. Because of the particular worst case SRAM parameters that were chosen, this design contains the maximum number of parts that are required for any design.

Given the above considerations, this 20-MHz design requires the following parts:

Parts List:

QTY	PART	DESCRIPTION
1	674219	FIFO RAM Controller
1	74F138	Address Decoder
2	74F374	8-bit Register
1	74F32	OR-Gate
1	20 ns ±10%	Delay Line

The following is a step-by-step analysis of the read and write equations to determine the required SRAM parameters. The equations will also show the delay line needed to avoid bus contention.

Read Equations:

Equation 1-1

$t_{RC} \leq 2T - t_{DECODE(max)} + t_{DECODE(min)} - t_{ANVAV(max)}$

100 - 9.0 + 3.0 - 12
[FRC] [F138] [F138] [FRC]

$t_{RC} \leq 82.0$ ns

Equation 1-6

$t_{RDREGH(max)} = t_{ANV\ (min)} - t_{ORSKEW\ (max)}$

15 - 6.6
[FRC] [F32]

$t_{RDREGH(max)} = 6.6$ ns

Equation 1-2

$t_{AA} \leq 2T - MAX(t_{AV} - t_{RDREGH}) - t_{S(min)}$

100 - (40 - 8.4) - 2.0
[FRC] [FRC] [F32] [F374]

$t_{AA} \leq 66.4$ ns

Equation 1-3

$t_{ACS} \leq 2T - t_{DECODE(max)} - MAX(t_{AV} - t_{RDREGH}) - t_{S(min)}$

100 - 9.0 - (40 - 8.4) - 2.0
[FRC] [F138] [FRC] [F32] [F374]

$t_{ACS} \leq 57.4$ ns

Equation 1-4

$t_{OH(min)} + t_{ANV(min)} \geq t_{RDREGH(max)} + t_{H(min)}$

0 + 15 ≥ 8.4 + 2.0
[SRAM] [FRC] [F32] [F374]

15 ns ≥ 10.4 ns

Equation 1-5

$t_{HZ(min)} + t_{ANV(min)} \geq t_{RDREGH(max)} + t_{H(min)}$

0 + 15 ≥ 8.4 + 2.0
[SRAM] [FRC] [F32] [F374]

15 ns ≥ 10.4 ns

Write Equations:

Equation 2-1

$t_{WC} \leq 2T - t_{ANVAV(max)}$

100 - 12
[FRC] [FRC]

$t_{WC} \leq 88.0$ ns

Equation 2-2

$t_{AW} \leq 2T - t_{WHAV(max)}$

100 - 25
[FRC] [FRC]

$t_{AW} \leq 75.0$ ns

Equation 2-3

$t_{CW} \leq 2T - t_{WHAV(max)} - t_{DECODE(max)}$

100 - 25 - 9.0
[FRC] [FRC] [F138]

$t_{CW} \leq 66.0$ ns

Equation 2-4

$t_{WP} \leq 2T - t_{PW(max)}$

100 - 25
[FRC] [FRC]

$t_{WP} \leq 75.0$ ns

Equation 2-5

$t_{DW} \leq 2T - t_{CP(max)} - t_{WHWRCH(max)}$

100 - 12.5 - 18
[FRC] [F374] [FRC]

$t_{DW} \leq 69.5$ ns

Equation 2-8

$t_{DLY(min)} = t_{WZ(max)} - t_{PZ(min)} - t_{OR(min)}$

20 - 2.0 - 3.0
[SRAM] [F374] [F32]

$t_{DLY(min)} = 15$ ns (USE 20 ns ' 10%

Equation 2-6

$t_{WOE(max)} = t_{DLY(max)} + t_{OR(max)}$

22 + 6.6
[DELAY] [F32]

$t_{WOE(max)} = 28.6$ ns

Equation 2-7

$t_{DW} \leq 2T - t_{PW(max)} - t_{PZ(max)} - t_{WOE(max)}$

100 - 25 - 12.5 - 28.6
[FRC] [FRC] [F374] [delay]

$t_{DW} \leq 33.9$ ns

RESULTS

READ PARAMETERS:

Minimum t_{RC} = 82.0 ns
Minimum t_{AA} = 66.4 ns
Minimum t_{ACS} = 57.4 ns
Minimum t_{OH} = 0 ns (Assumed)
Minimum t_{HZ} = 0 ns (Assumed)

WRITE PARAMETERS:

Minimum t_{WC} = 88.0 ns
Minimum t_{AW} = 75.0 ns
Minimum t_{CW} = 66.0 ns
Minimum t_{WP} = 75.0 ns
Minimum t_{DW} = 33.9 ns (Equation 2-7 used for $t_{DW(min)}$)
Minimum t_{WR} = 0 ns (Because FRC's t_{WR} = 0 ns)

DELAY LINE:

20 ns Delay Line ('10%)

Based on those results, the Hitachi HM6168H-45 was selected. This is a 4096 x 4-bit Static RAM with a 45-ns access time. Its specifications are:

READ PARAMETERS:

Minimum t_{RC} = 45.0 ns
Minimum t_{AA} = 45.0 ns
Minimum t_{ACS} = 45.0 ns
Minimum t_{OH} = 5.0 ns
Minimum t_{HZ} = 0 ns

WRITE PARAMETERS:

Minimum t_{WC} = 45.0 ns
Minimum t_{AW} = 40.0 ns
Minimum t_{CW} = 40.0 ns
Minimum t_{WP} = 35.0 ns
Minimum t_{DW} = 20.0 ns
Minimum t_{WR} = 0 ns

Sixteen 4K x 4-bit SRAMs are required to complete a 32K x 8-bit FIFO buffer. The complete design is shown in Figure 14. This illustrates the two OR-gates, the delay line, the decoder, the two registers, the Static RAM array and the 674219 FIFO RAM Controller in a 20-MHz design.

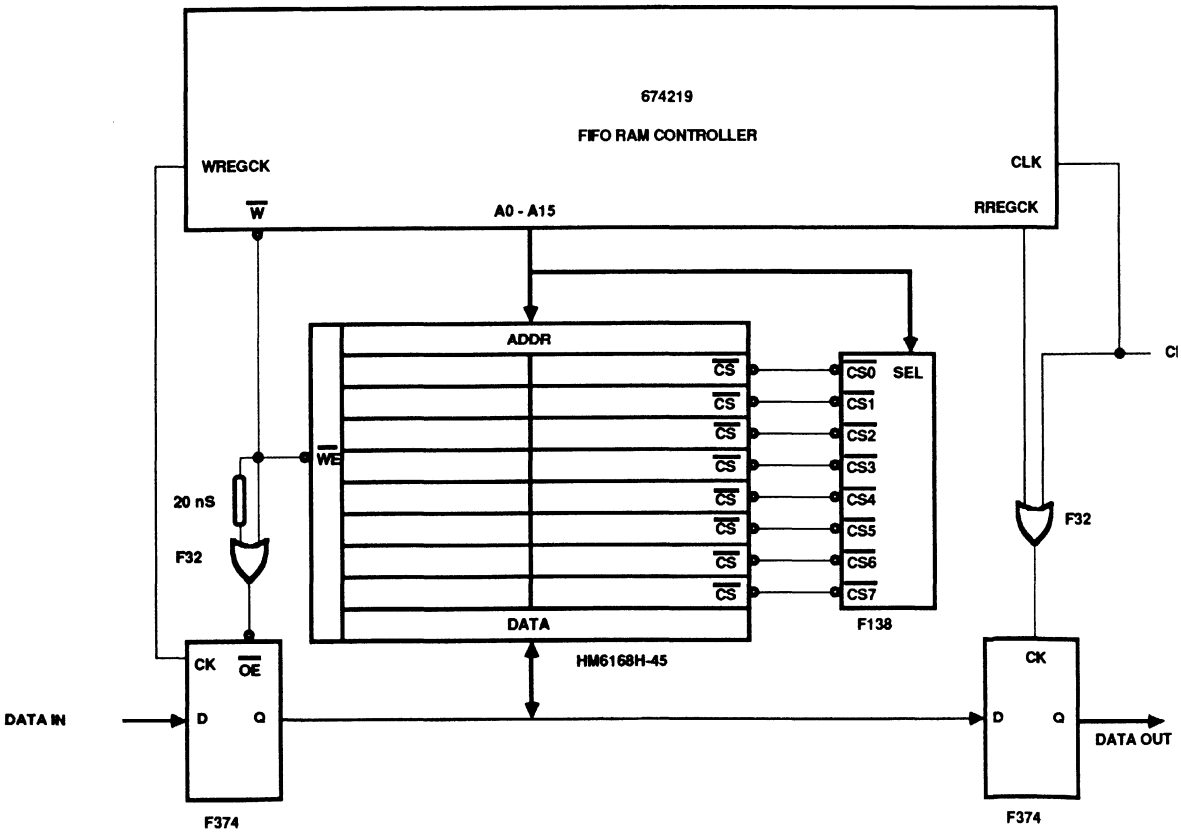


Figure 14. Worst Case Design for 20 MHz

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7.0 V
DC input voltage V_I ..... -0.5 V to 5.5 V
DC output voltage, V_O ..... -0.5 V to 5.5 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage termperature ..... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIG.	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	N/A	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	N/A	-55		125	0		75	°C
t_{CLKWH}	Clock width HIGH	9,10	45			31			ns
t_{CLKWL}	Clock width LOW	9,10	34			18			ns
f_{CLK}	Clock frequency	N/A			12.5			20	MHz
t_{REQL}	Request LOW time	7,9,10	12			12			ns
t_{REQH}	Request HIGH time	9,10	25			25			ns
t_{MRL}	Master Reset width LOW	7	60			50			ns
t_{MRS}	Master Reset HIGH to WREQ LOW	7	25			25			ns
t_{PS}	Priority to non-sampling clock setup time	5,6	30			25			ns
t_{EWRQ}	WEN to WREQ setup time	7,9	0			0			ns
t_{ERRQ}	REN to RREQ setup time	10	0			0			ns
t_{WEH}	WREQ to WEN hold time	9	15			15			ns
t_{REH}	RREQ to REN hold time	10	15			15			ns
t_{WRQC}	WREQ LOW to sampling clock setup time	7,9	5*		30*	10*		25*	ns
t_{RRQC}	RREQ low to sampling clock setup time	10	5*		30*	10*		25*	ns

* The request window must be observed to guarantee proper operation, between min and max values are not allowed.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-Level input voltage					0.8	V
V_A	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.5	V
I_{IL}*	Low-level input current	V_{CC} = MIN	V_I = 0.45 V			-250	μA
I_{IH}*	High-level input current	V_{CC} = MIN	V_I = 2.4 V			50	μA
I_I	Maximum input current	V_{CC} = MIN	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{CC} = MIN V_{CC} = MIN	I_{OL} (Address) = 16 mA I_{OL} (Control) = 8 mA I_{OL} (Flag) = 8 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{CC} = MIN V_{CC} = MIN	I_{OH} (Address) = -3 mA I_{OH} (Control) = -3 mA I_{OH} (Flag) = -3 mA	2.4			V
I_{OS}**	Output short-circuit current	V_{CC} = MAX	V_{OH} = 0 V	-20		-90	mA
I_{OZH} I_{OZL}	Off-state output currents	V_{CC} = MAX V_{CC} = MAX	V_O = 2.4 V V_O = 0.4 V			+40 -350†	μA
I_{CC}	Supply current	V_{CC} = MAX				350	mA

*Except TEST pin, which should always be grounded.

**No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

†I_{OZL} is Output leakage current plus I_{IL}.

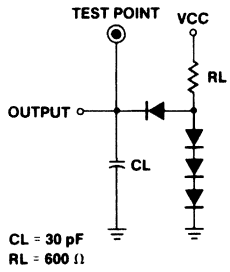
Switching Characteristics

SYMBOL	PARAMETER	FIG.	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{MRWH}	Master Reset LOW to WRDY HIGH	7			50			50	ns
t_{MRRL}	Master Reset LOW to RRDY LOW	7			50			50	ns
t_{MREF}	Master Reset LOW to EMPTY flag HIGH	7			50			50	ns
t_{MRAL}	Master Reset LOW to Almost HIGH	7			60			55	ns
t_{MRWRC}	Master Reset LOW to WREGCK HIGH	7			40			35	ns
t_{MRRRC}	Master Reset LOW to RREGCK HIGH	7			40			35	ns
t_{MRWBH}	Master Reset LOW to W HIGH	7			50			50	ns
t_{AV}	Clock to address valid	7,9,10,12,13			50			40	ns
t_{ANV}	Clock to address not valid	7,9,10,12,13	15			15			ns
t_{ANVAV}	Address not valid to address valid	7,9,10,12,13			20			12	ns
t_{CWRL}	Clock to WRDY LOW	7,9			35			35	ns
t_{CWRH}	Clock to WRDY HIGH	7,9			40			35	ns
t_{CWRGL}	Clock to WREGCK LOW	7,9			35			30	ns
t_{CWRGH}	Clock to WREGCK HIGH	7,9			35			30	ns
t_{CWL}	Clock to W LOW	7,9			50			45	ns
t_{CWH}	Clock to W HIGH	7,9			25			25	ns
t_{AS}	Address valid to W LOW	7,9	0		12	0		12	ns
t_{WR}	Address not valid to W HIGH	7,9			0			0	ns
t_{WP}	W pulse width LOW at f_{CLK}(max)	9,13	100*			50**			ns
t_{PW}	W pulse width HIGH	4,13	12		30	12		25	ns
t_{WHAV}	W HIGH to address valid	4,9,13			35			25	ns
t_{WHWRCH}	W HIGH to WREGCK HIGH	4,13			25			18	ns
t_{CRRL}	Clock to RRDY LOW	10			35			30	ns
t_{CRRH}	Clock to RRDY HIGH	7,10			40			35	ns
t_{CRRGL}	Clock to RREGCK LOW	7,10			35			30	ns
t_{CRRGH}	Clock to RREGCK HIGH	7,10,12			35			30	ns
t_{ARRH}	Address valid to RREGCK HIGH at f_{CLK}(max)	10	110*			60**			ns
t_{ANRRH}	Address not valid to RREGCK HIGH	10			10			8	ns
t_{CE}	Clock to EMPTY flag	7,9,10			40			35	ns
t_{CF}	Clock to FULL flag	9,10			40			35	ns
t_{CHF}	Clock to Half-Full flag	9,10			50			45	ns
t_{CA}	Clock to Almost flag	9,10			60			55	ns
t_{LZ}	Address bit LOW to Hi-Z	15			30			30	ns
t_{HZ}	Address bit HIGH to Hi-Z	15			30			30	ns
t_{ZL}	Address bit Hi-Z to LOW	15			30			30	ns
t_{ZH}	Address bit Hi-Z to HIGH	15			30			30	ns

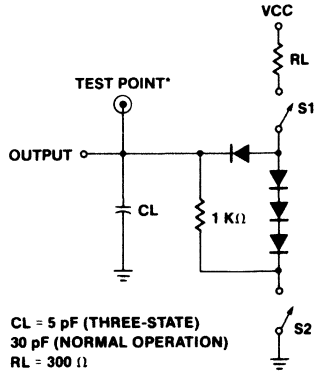
* f_{CLK}(max) = 12.5 MHz (Military).

** f_{CLK}(max) = 20 MHz (Commercial).

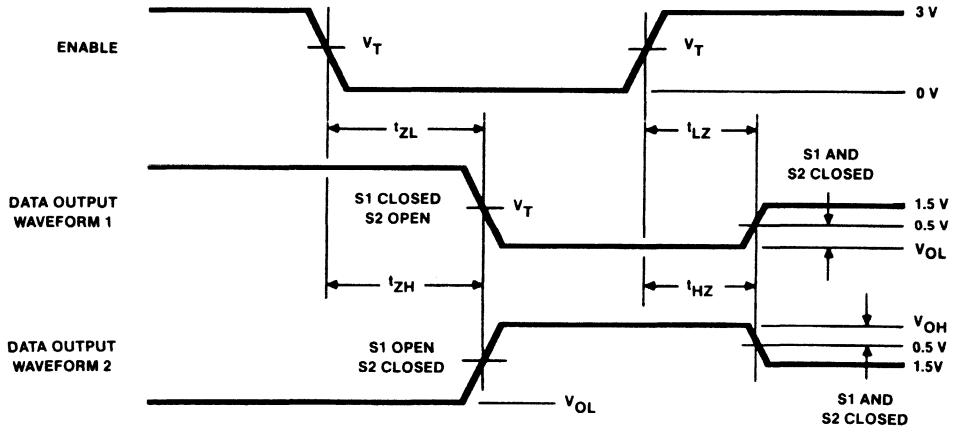
Standard Test Load



Load Circuit for Bi-State Outputs (Control and Flag Outputs)



Load Ciruit for Three-State Outputs (Address Outputs)



Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled.
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled.

Figure 15. Enable and Disable Timing

Notes: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N306A.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{out} = 50 Ω and $t_R \leq 2.5$ ns $t_F \leq 2.5$ ns.
F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

Basic FIFO Design Considerations

Designing with today's high speed RAM-based FIFOs offers a neat, low overhead solution to asynchronous buffering. Traditionally, FIFOs have been designed with a register-based architecture which tends to be shallow in depth (typical 64 words) and has performance problems such as long data fall-through times.

RAM-based FIFOs such as AMD's Am7202A/3A/4A/5A are architectured in such a manner to overcome the performance inadequacies of register-based FIFOs. These new, enhanced FIFOs incorporate a dual-port RAM as their core, and read/write address counters to generate status flags (See Figure 1).

Proper operation of the FIFO is initiated by a master reset cycle. The master reset is required to initialize the internal pointers and to determine the FIFO mode of operation. During this period, the FIFO is preconditioned to accept data. Both the read and write pointers are reset to their zero location and the flag logic is set to reflect the condition of the FIFO (Empty flag will be active). The FIFO is now ready to accept data. A write cycle begins with the falling edge of the $\overline{W}$ input and data is written into the first nine bit location of the RAM core. The write counter is then incremented. The read operation works in the same fashion, but is controlled by the $\overline{R}$ input signal. Reading data out is a function of how fast the device can access the RAM; therefore, the limiting parameter is t_A.

The Am720XA is an extremely fast device, accessing data in 15 ns. At these speeds the internal device logic is very sensitive to ringing inputs and noisy control lines.

Simple precautions can be taken to limit the possibility of incorrect operation due to false triggering. It is recommended that the user take time to insure proper design layout of the PC board. It is recommended that a ground plain board approach be used and that a decoupling capacitor be used for each FIFO (Figure 2).

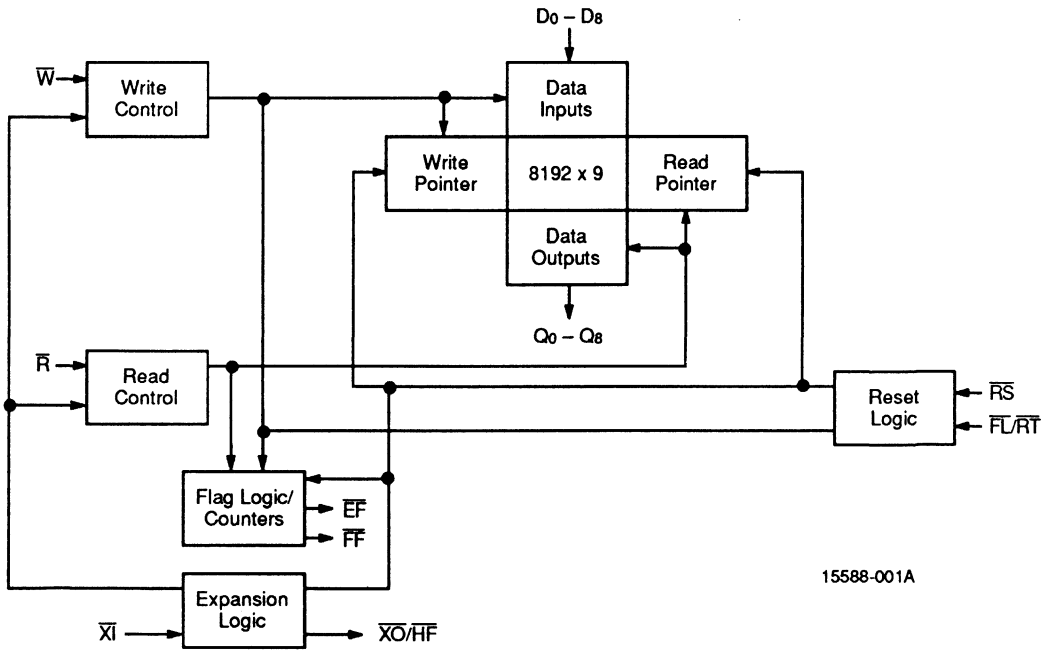


Figure 1. Block Diagram of Am7205A

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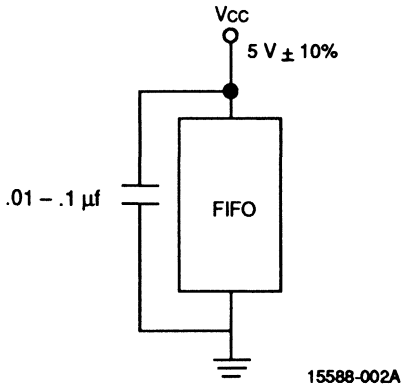


Figure 2. Power Supply Decoupling

Capacitor values should range from .01µf to .1µf. Larger values have little effect in filtering short duration noise on the Vcc line. A regulated power supply should be used in order to ensure that the device operates within the Vcc specification (Vcc = 4.5 V to 5.5 V).

Another source of noise to consider is crosstalk due to a very tight layout on the PC board. Trace to trace capacitance can cross-couple noise with signals on an adjacent trace. High speed clock signals should be routed clear of control and data lines of the FIFO.

Although an excessive inductive load normally doesn't cause a problem, there is a potential of output signal degradation due to this phenomenon. If a significant amount of capacitance and inductance is present, a transmission line reflection could occur. This will also reduce the noise margin of the signal and may cause illegal triggering of the next stage. This can be remedied by incorporating a line buffer at the output of the FIFO or terminating the receiver end of the signal.

When the output buffers switch, the FIFO must supply additional current through the buffer (Figure 3). This current is required to charge or discharge the output capacitance. Device packaging has a small inductance created by the package leadframe. This series package inductance along with the PC board inductance will reduce the noise margin of the buffer. The rapid change in current demand in the buffer creates a transient ground bounce. This ground bounce is a result of $V = L\ (di/dt)$, where V = Voltage, L = ground circuit inductance, di/dt = rate of change of the charge currents.

Special attention should be given to the $\overline{R}$ and $\overline{W}$ input clock lines. It is imperative that these signals be free of glitches and have clean edges. Under normal operation, rise and fall times should not be extremely long in duration so false triggering of the on-chip pointers does not occur as the signal slews through threshold. These lines directly control the location of the read and write counters. A very narrow glitch into the counter can misclock the counter, scramble data or corrupt flag locations. Master reset would then be required to continue proper operation.

System timing schemes usually use a 50% duty cycle clock. Typically the read and or write signals are generated in the same manner. A narrow transition during the $\overline{R}$ or $\overline{W}$ active low time may cause false clocking. It is advisable to limit the read and write pulse widths. By reducing the low time to a reasonable minimum (t_{RPW}, t_{WPW}), the time a glitch can cause false counter triggering is minimized (Figure 4).

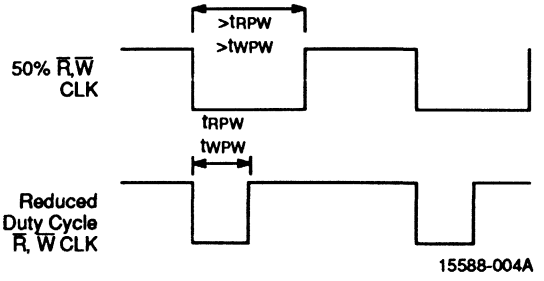


Figure 4. Timing Example

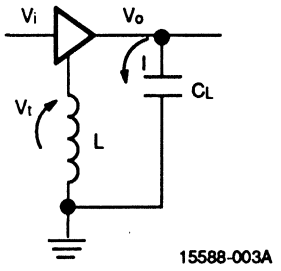


Figure 3. Buffer Configuration

Cascading FIFOs can be achieved by simply tying the $\overline{XO}$ output to the $\overline{XI}$ input of the next FIFO (see Fig. 5). One can create the depth of a storage buffer in multiples of the individual FIFO density being used. For more details on cascading FIFOs, refer to accompanying Application Note in this section.

The Am720XA series incorporates a CMOS threshold for it's $\overline{XI}$ input to increase the noise immunity to that input. Excessive noise from other board signals could inadvertantly cause a false carry signal when the FIFOs are cascaded. The increased $\overline{XI}$ input HIGH threshold of 3.5 V results in extra margin over a standard TTL logic interface. It should be remembered that the $\overline{XO}/\overline{XI}$ interface is a dedicated FIFO signal and does not imply an incompatability.

In short, the Am720XA series FIFOs are very easy to use. Simple considerations to board layout and timing makes designing with RAM-based FIFOs a clean solution for asynchronous buffer applications.

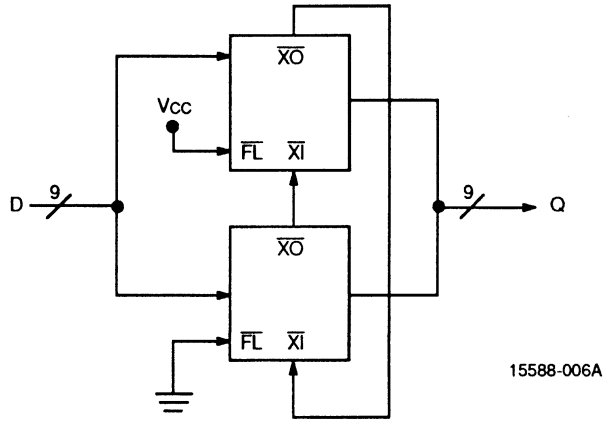


Figure 5. Two-cascaded FIFOs.

Operating FIFOs On Flag Boundary Conditions

by Patrick Wang

The Am7200, Am7201, Am7202A, Am7203A, Am7204A and Am7205A (256 x 9, 512 x 9, 1K x 9, 2K x 9, 4K x 9 and 8K x 9) FIFOs have three flags, Full ($\overline{FF}$), Empty ($\overline{EF}$), and Half-Full ($\overline{HF}$). These flags provide the user with the status of the FIFO and prevent overwriting while full and reading past empty. Because these FIFOs can perform asynchronous and simultaneous read and write operations, care must be taken when reading, writing and evaluating the flags near their boundary conditions.

When the FIFO only has one word in it, the falling edge of the Read signal ($\overline{R}$) will cause the Empty Flag ($\overline{EF}$) to be asserted. All subsequent read pulses will become blocked and thus will be ignored while $\overline{EF}$ remains LOW. Note that the internal logic of this part will block reads only after $\overline{R}$ goes HIGH, thus there is no shortening of any internal read signals caused by the assertion of the $\overline{EF}$. $\overline{EF}$ will go HIGH on the rising edge of $\overline{W}$ in the write cycle which eliminates the empty condition (Figure 1).

Operation of the Full Flag ($\overline{FF}$) is analogous to $\overline{EF}$. When the FIFO is one word from being full, the falling edge of $\overline{W}$ will cause $\overline{FF}$ to be asserted. All subsequent write pulses will become blocked and thus will be ignored while $\overline{FF}$ remains LOW. Note that the internal logic of this part will block writes only after $\overline{W}$ goes HIGH, thus there is no shortening of any internal write signals caused by the assertion of the $\overline{EF}$. $\overline{FF}$ will go HIGH on the rising edge of $\overline{R}$ in the read cycle which eliminates the full condition (Figure 2).

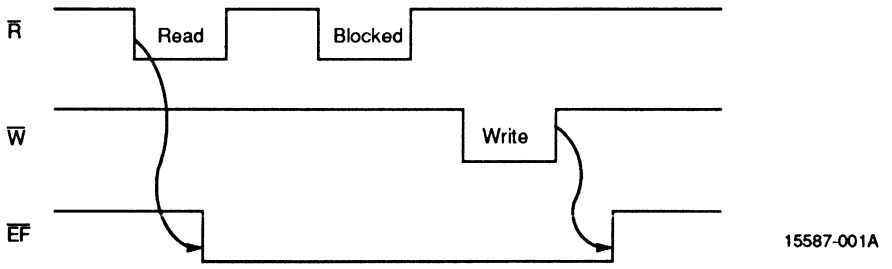


Figure 1. Normal Read Timing

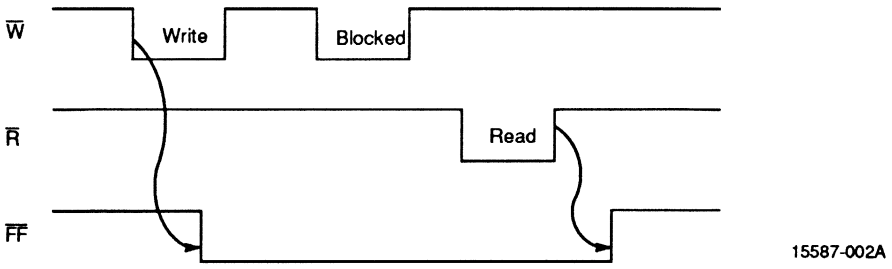


Figure 2. Normal Write Timing

Operating FIFO's on Flag Boundary Conditions

Read data flow-through occurs when the FIFO is empty and $\overline{R}$ is held LOW prior to a low going write pulse. The rising edge of $\overline{W}$ will deassert the $\overline{EF}$, but because $\overline{R}$ is held LOW, a read cycle is initiated when $\overline{EF}$ goes HIGH. This read then causes the $\overline{EF}$ to return LOW. $\overline{EF}$ will pulse HIGH with a width of not less than t_{RFT} (Figure 3). To maintain a minimum pulse width on $\overline{R}$, begin reads only after $\overline{EF}$ is HIGH, or hold $\overline{R}$ LOW for t_{RPE} after the rising edge of $\overline{EF}$.

Write data flow-through occurs when the FIFO is full and $\overline{W}$ is held LOW prior to a low going read pulse. The rising edge of $\overline{R}$ will deassert $\overline{FF}$, but because $\overline{W}$ is held LOW, a write cycle is initiated when $\overline{EF}$ goes HIGH. This write then causes $\overline{FF}$ to return LOW. $\overline{FF}$ will pulse HIGH with a width of not less than t_{WFT} (Figure 4). To maintain a minimum pulse width on $\overline{W}$, begin writes only after $\overline{FF}$ is HIGH, or hold $\overline{W}$ LOW for t_{WPF} after the rising edge of $\overline{FF}$.

t_{WPF} is a minimum pulse width defined by the deassertion of $\overline{FF}$ to the rising edge of $\overline{W}$ in a "write data flow-through" mode near full. t_{RPE} is a minimum pulse width defined by the deassertion of the $\overline{EF}$ to the rising edge of $\overline{R}$ in a "read data flow-thru" mode near empty. Both t_{RPE} and t_{WPF} are specified equal to minimum read (t_{RPW}) and write (t_{WPW}) pulse widths. Violation of these parameters may create a shortened internal command pulse which may cause improper flag assertion and missing or scrambled data.

In the data flow-through modes, holding $\overline{R}$ LOW while writing when empty, and holding $\overline{W}$ LOW while reading when full, will initiate a read and write cycle respectively. In order to block a read when empty, the deassertion of read must preceed $\overline{W}$ going HIGH in the write cycle which brings the part from empty to not-empty (Figure 5). Likewise, to block a write when full, the deassertion of $\overline{W}$ must preceed $\overline{R}$ going HIGH in the read cycle which brings the part from full to not-full (Figure 6). If the user is not aware of this, he may inadvertantly enter a data flow-through condition where he must abide by t_{RPW} and t_{WPW} pulse widths.

The Half-Full ($\overline{HF}$) flag is asserted by the falling edge of $\overline{W}$ and deasserted on the rising edge of $\overline{R}$. Because these FIFOs allow asynchronous assertion of the read and write clock lines, $\overline{HF}$ may pulse with arbitrarily short duration when the FIFO is operated at the half-full boundary condition. The FIFO is moving dynamically through half-full and the pulse width will be dependent on the precise phase of the read and write clocks. It is recommended that level-sensitive, rather than edge-sensitive, detection circuits should be used for monitoring the status of $\overline{HF}$.

The Am720X series FIFOs have Full, Empty and Half-Full flags to provide the user with the status of the FIFO and to prevent overwriting when full and reading when empty. Care must be taken in the asynchronous operation of this part near the boundary conditions of these flags. Read and write clock low times should be minimized for increased noise immunity. The status flags should be monitored and used to control the write and read clocks. The user must be aware of the boundaries and operation of the read and write data flow-through modes.

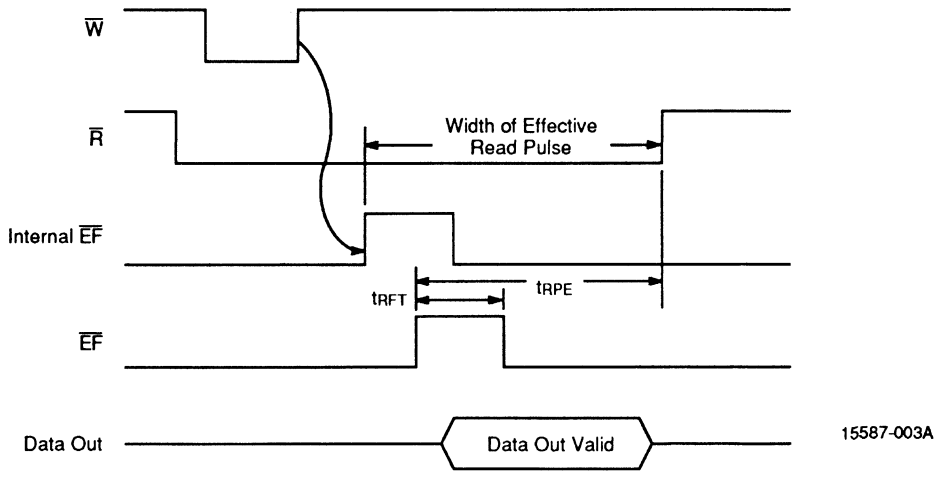


Figure 3. Read Flow-Through Mode

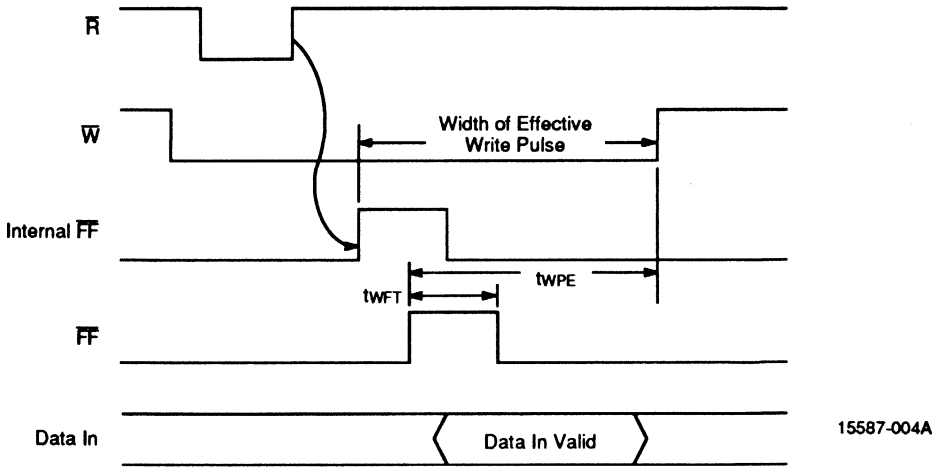
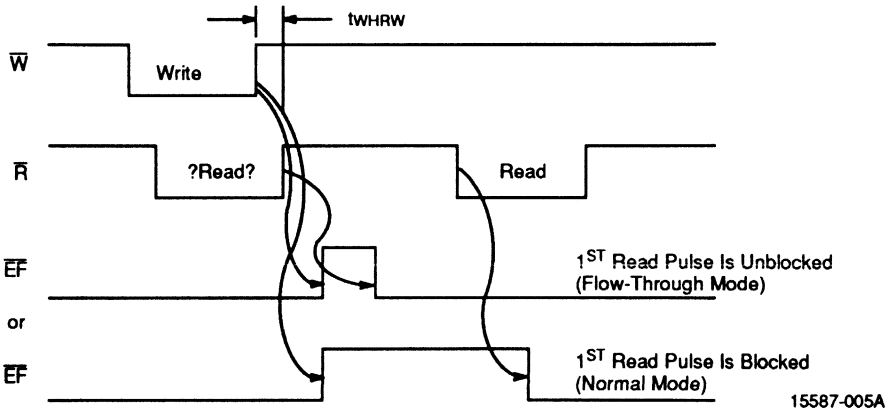
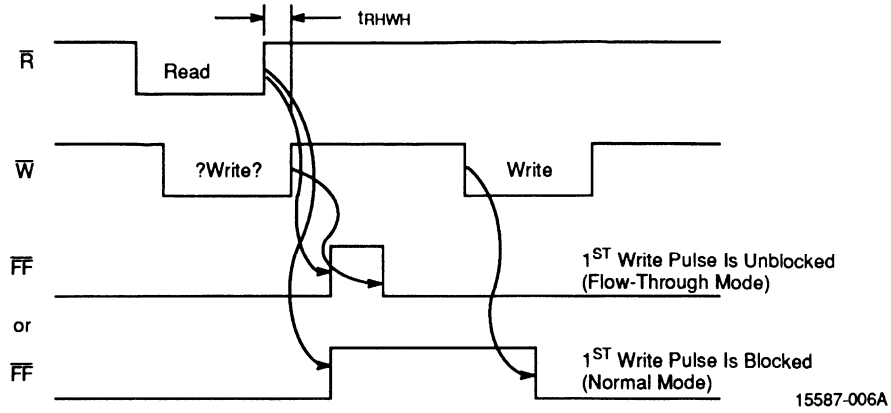


Figure 4. Write Flow-Through Mode



$\overline{EF}$ will switch depending on the time between $\overline{W}$ HIGH to $\overline{R}$ HIGH (t_{WHRH}).
t_{WHRH} < 0: Blocked
t_{WHRH} > 0: Flow-through may occur, t_{WPE} must be observed.

Figure 5. Read Flow-Through Boundary



FF will switch depending on the time between R HIGH to W HIGH (t_{RHWH}).
t_{RHWH} < 0: Blocked
t_{RHWH} > 0: Flow-through may occur, t_{RPE} must be observed.

Figure 6. Write Flow-Through Boundary

Cascading AMD High Density CMOS FIFOs

The Am7202A, Am7203A, Am7204A and Am7205A are high-speed 1K x 9, 2K x 9, 4K x 9 and 8K x 9 CMOS FIFOs, respectively, that can be cascaded to form even deeper FIFOs. This application note explains how these AMD FIFOs can be cascaded together, and includes details not covered in the datasheet. The AC behavior of parts in cascade mode is discussed, and seven new AC parameters are introduced along with 'typical' times. Descriptions of composite flags and cascade pulse timing during special Read conditions are also presented.

In Depth Expansion mode, the combination of cascaded FIFOs can be considered a single FIFO. As long as input signals to the cascaded configuration (i.e. writes and reads) adhere to normal setup, hold, and recovery times, the FIFOs will cascade correctly. All of the signals passed between the FIFOs across the $\overline{XI}$ and $\overline{XO}$ lines are transparent to the user. Figure 1 shows a cascaded configuration of 3 FIFOs. The $\overline{FL}$ pin (First Load) of the first FIFO to be written to (after a master reset) is tied to V_{SS}. All of the other FIFOs have their $\overline{FL}$ pin tied to V_{CC}. The $\overline{XO}$ of the first FIFO is tied to the $\overline{XI}$ of the second FIFO. This daisy chain configuration is continued to the desired depth, with the $\overline{XO}$ of the last FIFO tied to $\overline{XI}$ of the first FIFO.

After a master reset, the FIFO with it's $\overline{FL}$ pin tied to Vss can be thought of as possessing both a read "token" and a write "token." During a write operation, only the FIFO with the corresponding token will recognize the write. Similarly, during a read operation, only the FIFO with the read token will recognize and latch input data.

Consider the first FIFO in a cascade of arbitrary depth: After a master reset, only it will be enabled to recognize writes and reads. When the write operation occurs which fills the FIFO, the device will "pass" the write token on to the next FIFO by pulsing it's $\overline{XO}$ line. Similarly, when enough read operations have been performed to empty the FIFO, it will "pass" the read token by pulsing the $\overline{XO}$ line a second time. Further writes and reads will be ignored until the FIFO's $\overline{XI}$ line pulses. This will reenable Write, while the second $\overline{XI}$ pulse will reenable Read.

Noise on the $\overline{XO}/\overline{XI}$ lines may cause a false low to be recognized by a FIFO. This event could insert an additional token into the cascade of FIFOs, and subsequent reads and writes could be recognized by multiple FIFOs. To improve noise margins on the $\overline{XO}$ and $\overline{XI}$ pins, the Am720XA family of High Density CMOS FIFOs uses CMOS levels instead of TTL levels. The V_{IL} and V_{IH} DC characteristics of these pins are given in the datasheet as V_{IHXI} and V_{ILXI}.

The cascade output, $\overline{XO}$, is multiplexed with $\overline{HF}$, so the Half-Full flag may not be used in cascade mode. The Empty and Full flags, however, are functional for the individual FIFOs in a cascaded configuration. As shown in Figure 1, Compound-Full (all FIFOs full) and Compound-Empty (all FIFOs empty) are simple to implement. Individual FIFOs' Empty and Full flags may be tied together to generate various intermediate compound flags. Figure 2 shows a cascade of four FIFOs with various intermediate positions of the read and write pointers, and the FIFOs' individual flag values.

Below are switching characteristics and times for seven cascade parameters. Full descriptions of the $\overline{XO}$ and $\overline{XI}$ pulse timing follow. All parameters timing is 'typical.'

SWITCHING CHARACTERISTICS. All values are 'typical'

Parameter Symbol	Parameter Description	Am720XA -15	Am720XA -25	Am720XA -35	Am720XA -50	Unit
Expansion Timing						
t_{XOL}	Expansion Out Low Delay from Clock	20	25	35	50	ns
t_{XOH}	Expansion Out High Delay from Clock	20	25	35	50	ns
t_{XIS}	$\overline{XI}$ setup to Clock	10	15	15	15	ns
t_{PXI}	Positive $\overline{XI}$ pulse-width during Flow-Through.	10	10	10	15	ns
t_{XI}	Negative $\overline{XI}$ pulse-width	15	25	35	50	ns
t_{PXO}	Positive $\overline{XO}$ pulse-width during Flow-Through	10	10	10	15	ns
t_{XO}	Negative $\overline{XO}$ pulse-width	15	25	35	50	ns

Note:

These parameters are transparent to the user. AMD FIFOs are guaranteed to cascade correctly.

The first three AC parameters are simply delays. t_{XOL} and t_{XOH} are delays from rising and falling clock edge, to $\overline{XO}$ response (as shown in Figure 3). t_{XIS} represents the delay necessary after a token has been passed before a write or read operation can be initiated (as shown in Figure 4).

t_{XI} represents a negative pulse width (see figure 4). $\overline{XO}$ must stay low enough for the next FIFO to recognize the token it is receiving. As long as the minimum Write and Read clock pulse widths (t_{WPW} and t_{RPW}, respectively) are met, t_{XI} will meet its required width.

t_{PXI} represents a positive pulse width requirement. The minimum pulse width will appear only during Read Flow-Through Mode. The reader may wish to read the accompanying application note, "FIFO Boundary Issues" to familiarize himself with this special condition. Referring to figure 5, the last read operation in a FIFO (which has both the read and write tokens) is begun while the part is in an empty state. The write operation is begun while read is active and the part is empty. This is referred to as Flow-Through Mode (this mode is only significant for cascading when the write and read operations in question are the **last of each** for that FIFO). The rising edge of the first $\overline{XO}$ pulse will go high t_{XOH} after the rising edge of the last write. The falling edge, however, is measured from the rising edge of the empty flag instead of the falling edge of read. The $\overline{EF}$ edge indicates that the FIFO is no longer empty, and the read operation can begin only then (and so $\overline{XO}$ will go low t_{XOL} from the rising edge of $\overline{EF}$). Simply put, in Flow-Through mode, where the write and read tokens will be passed immediately after each other, the delay of t_{PXI} guarantees that the following FIFO receiving the pulses will recognize two **distinct** pulses instead of only one.

t_{PXO} and t_{XO} are the minimum $\overline{XO}$ pulse widths generated by the FIFO corresponding to t_{PXI} and t_{XI}, respectively.

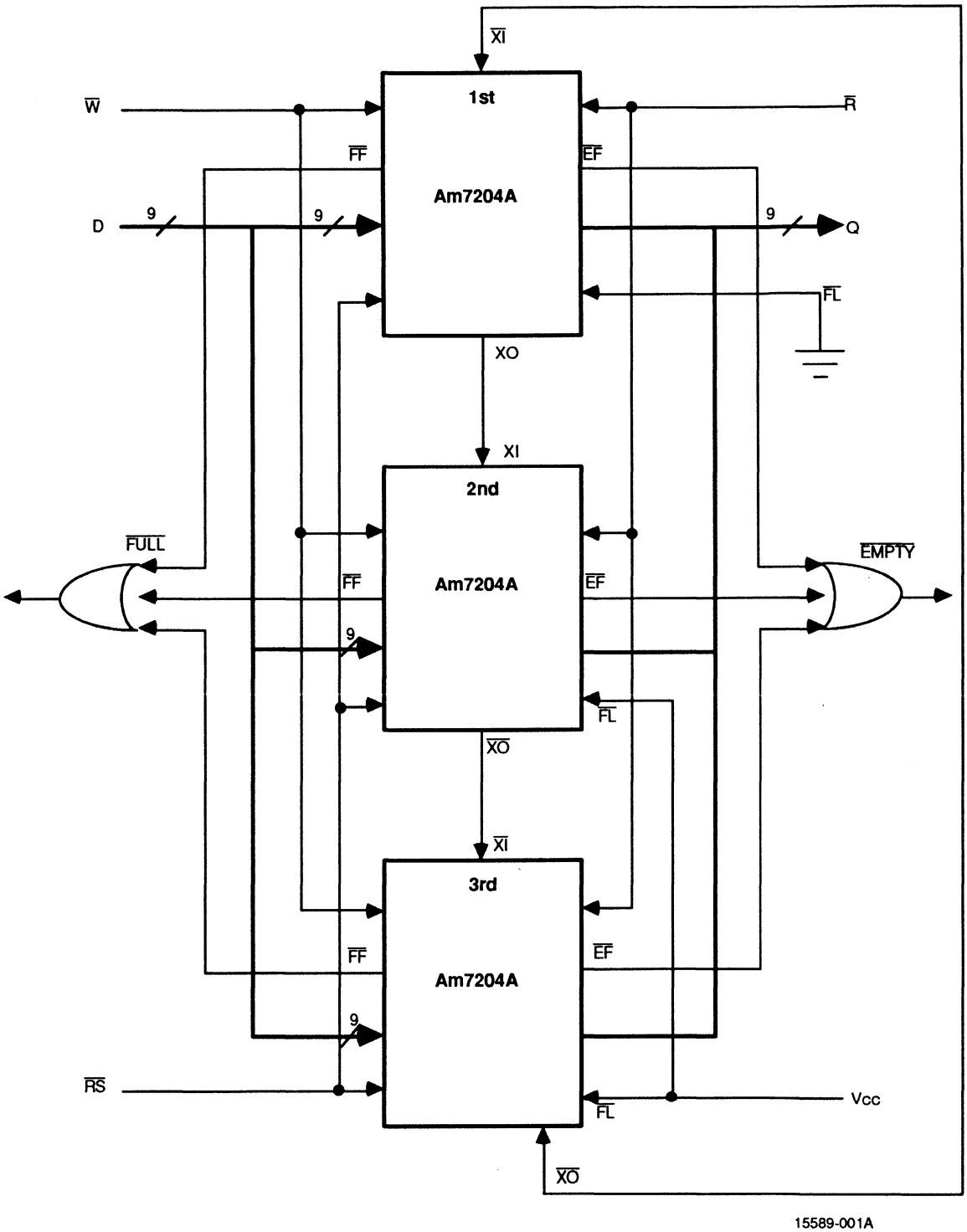


Figure 1. Depth-Expansion to Form a 12,288 x 9 FIFO

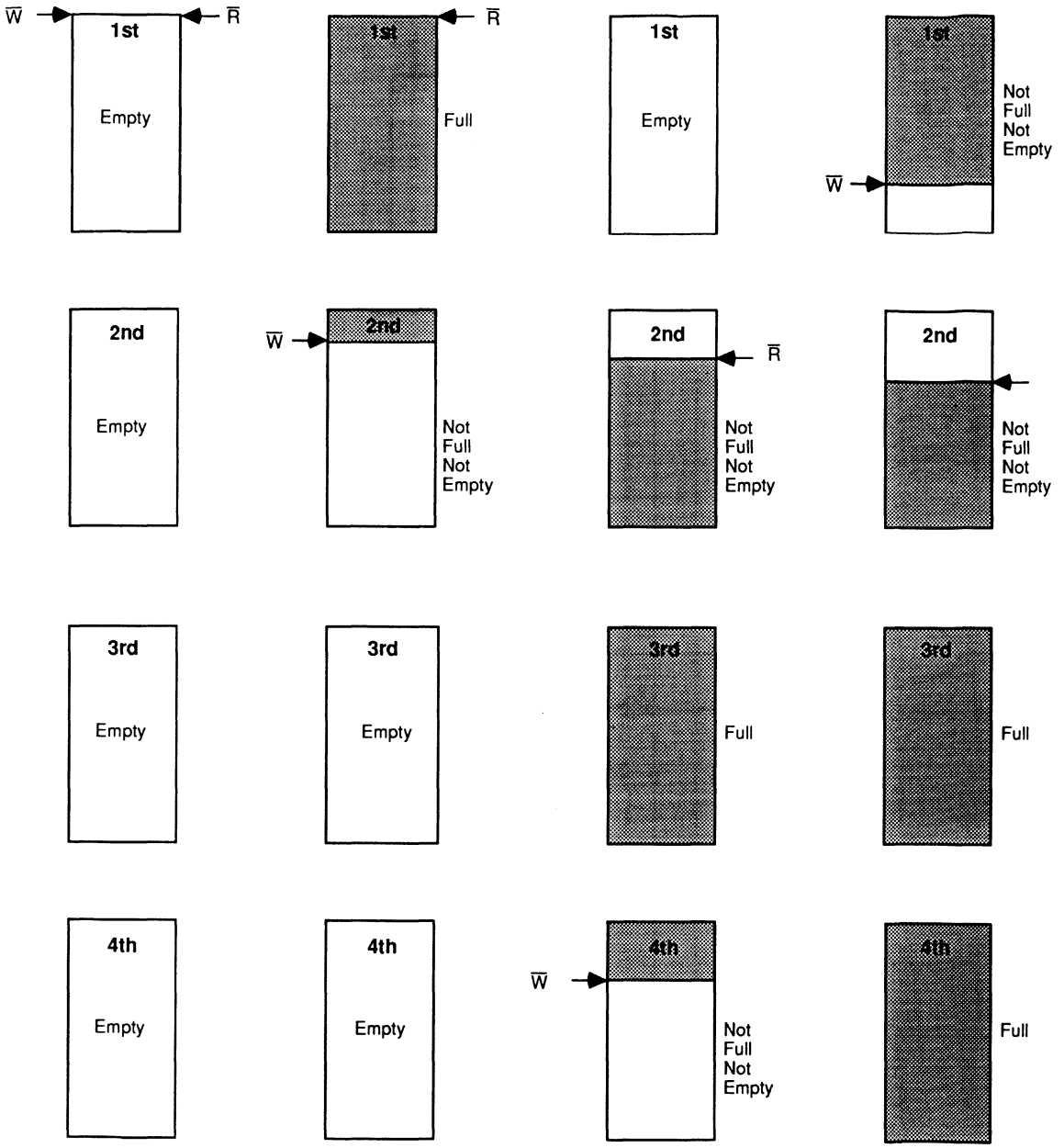


Figure 2. Intermediate FIFO States in Cascaded Configuration

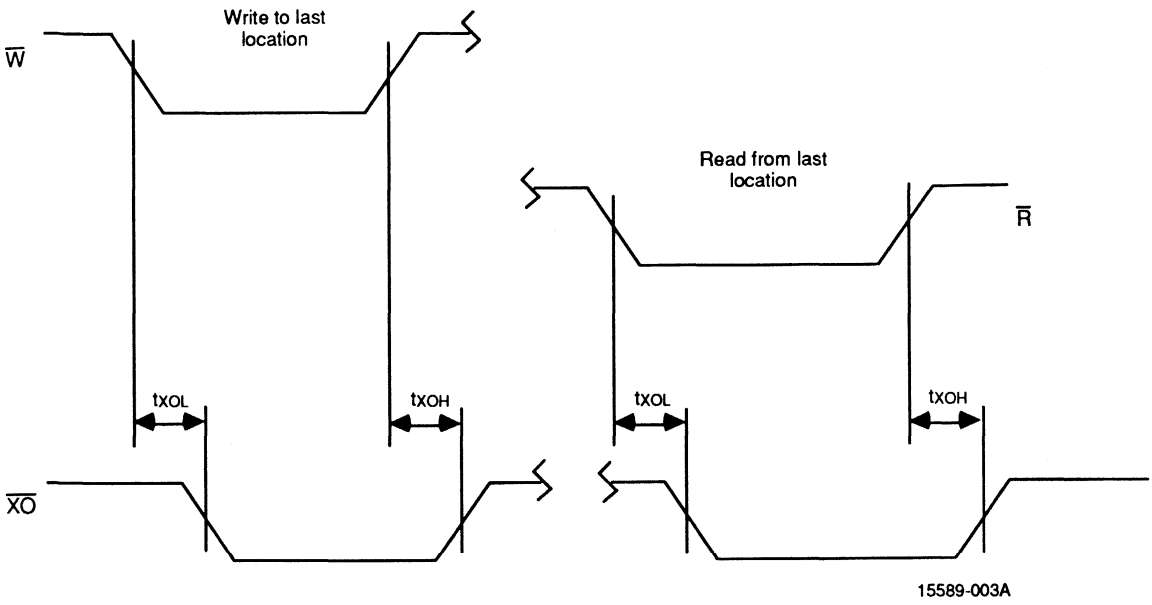


Figure 3. $\overline{XO}$ Delay from Clock

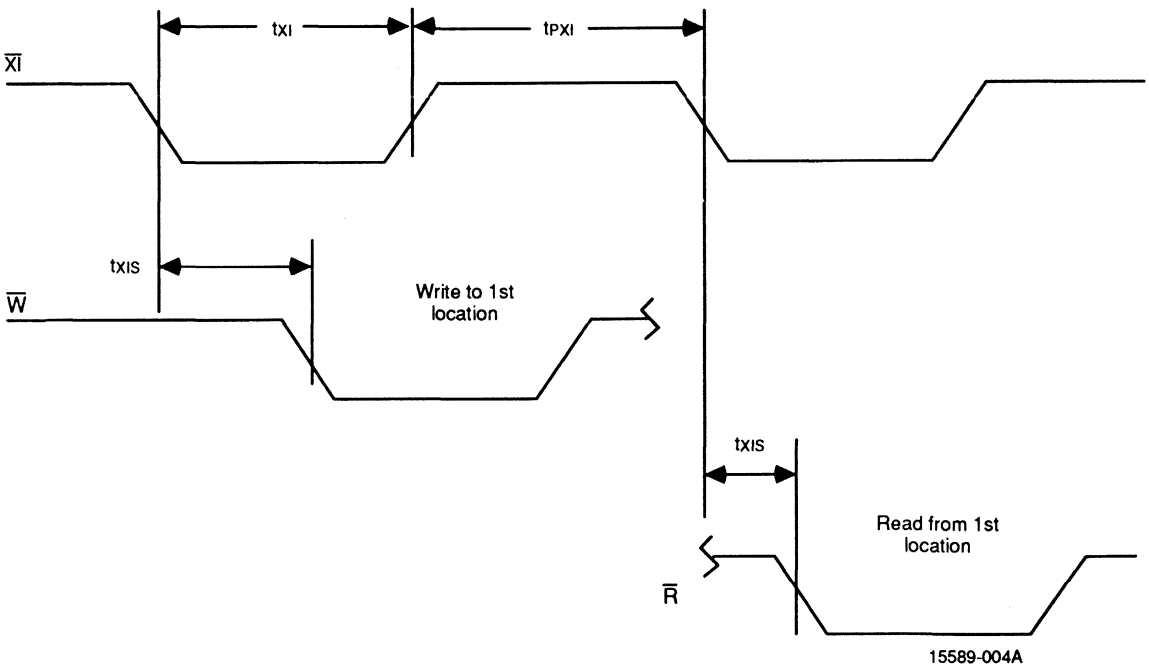


Figure 4. 1st Clock Pulse Delay from $\overline{XI}$

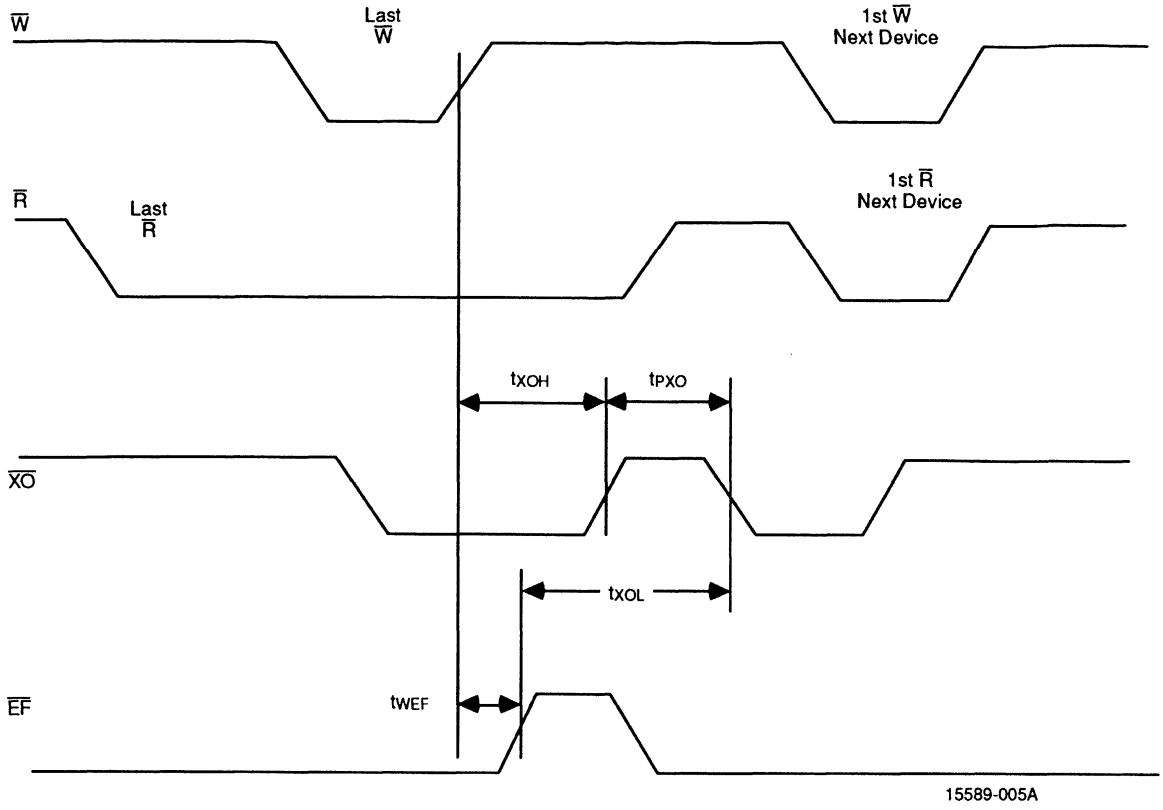


Figure 5. Cascade Timing During Read Flow-Through

Operation Overview

Small FIFOs are controlled by two signals, Shift In (SI) and Shift Out (SO). There are two status signals generated by the FIFO: Input Ready (IR) and Output Ready (OR). A typical small FIFO pinout is shown in Figure 1.

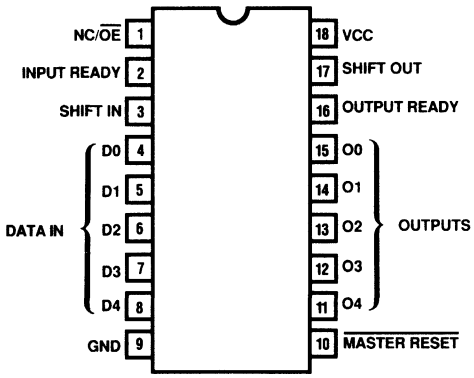


Figure 1. Typical Small-FIFO Pinout

Data is shifted into the FIFO as follows:

1. SI and IR both being HIGH initiates the shift in.
2. The FIFO internally detects a valid shift in by ANDing the SI and IR signals.
3. Data is latched by the FIFO when this valid shift is detected.
4. The FIFO acknowledges the valid shift by bringing IR LOW.
5. The SI line is brought LOW to complete the shift in operation, and to reset the valid shift detect.
6. IR returns HIGH if there is room for new data.

Data is shifted out of the FIFO as follows:

1. SO and OR both being HIGH initiates the shift out.
2. The FIFO internally detects a valid shift out by ANDing the SO and OR signals.
3. The FIFO acknowledges the valid shift out by bringing OR LOW.
4. The SO line is brought LOW to complete the shift out operation.
5. If the FIFO is not empty, OR will return HIGH following SO going LOW. Whenever OR is HIGH, a valid data word is present at the outputs.

The shift in operation is independent of the shift out operation, allowing data to be shifted in at a different rate than it is shifted out. The FIFO indicates that it is full by holding IR LOW after a shift in, and that it is empty by holding OR LOW after a shift out.

Cascading

If a deeper buffer size is required, two or more FIFOs may be cascaded, as shown in Figure 2.

The operation of this buffer is identical to that of the single FIFO buffer. The user controls the shifting of data into the most *upstream* part, and the shifting of data out of the most *downstream* part. This composite buffer has the same handshake (SI, IR, SO, and OR) and data (D0..D4, O0..O4) lines as a single FIFO.

The user has control over the data as it enters and leaves the buffer. The passage of data through the "middle" of the buffer is beyond user control. This data must be capable of being correctly transferred between any of the "middle" devices at a rate greater than or equal to the overall buffer throughput rate.

The point of data transfer between two FIFOs is called the *cascade interface*. There are numerous timing criteria which must be satisfied by the FIFOs on each side of this interface in order to ensure a flawless transfer of data. This is true even for two-FIFO buffers, in which the"middle" of the buffer consists of a single cascade interface. Such criteria must be satisfied at all frequencies within the operating range, and for asynchronous data streams. The following cases illustrate the various timing conditions that may be encountered whenever two or more FIFOs are cascaded.

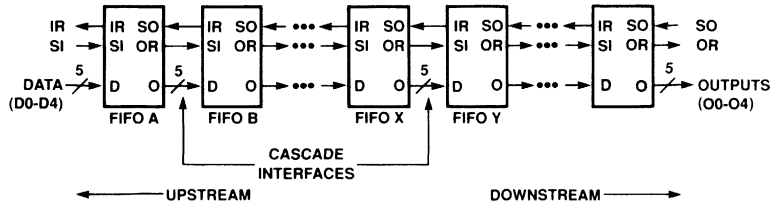


Figure 2. A Cascaded Buffer

Publication #	Rev.	Amendment	Issue Date
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Case 1: Low-Frequency Fallthrough

Monolithic Memories' shallow FIFOs are *fallthrough* devices, that is, the first word shifted into an empty part automatically "falls through" the buffer and it becomes visible at the outputs. Its presence is indicated by the rising edge of OR. The following sequence describes this fallthrough action as a word is shifted into FIFO A (see Figure 2):

1. IR of FIFO A is HIGH because the device is empty.
2. The user brings SI HIGH, latching the data word and commencing a shift in.
3. SI is then brought LOW to release the word for fallthrough.
4. OR of FIFO A will go HIGH within the "fallthrough time" (tPT). OR going HIGH signals a valid word at the outputs.
5. IR of FIFO B is HIGH because it, too, is empty.
6. Because OR of A is tied to SI of B, a valid shift in is begun into FIFO B on the rising edge of OR.
7. Because IR of B is tied to SO of A, a valid shift out is begun (SO*OR = 1) out of A.
8. Data is simultaneously shifted out of A, and into device B. The transfer is thus begun.
9. Because a valid shift out is detected in A, OR goes LOW to acknowledge it. This becomes a falling edge on SI for B.
10. The transfer is now complete. The word falls through B, then through FIFO C, and so on, until it reaches the outputs of the bottom FIFO.

The timing diagram for low-frequency fallthrough is shown in Figure 3.

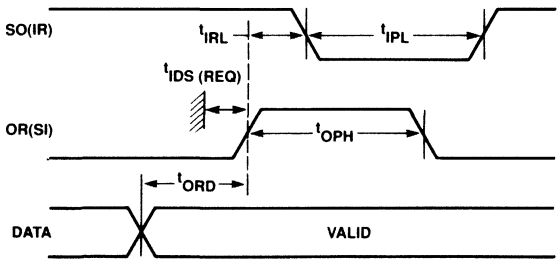


Figure 3. Low-Frequency Fallthrough

The term "low frequency" means that the time between arrival of words is long relative to the time required for a data transfer. There is a basic set of timing requirements that must be satisfied in all fallthrough cases, plus an additional one for high-frequency operation. The basic set will now be discussed.

Consider a cascade interface between FIFOs X and Y of Figure 2. The OR of X goes HIGH, then is quickly reset once a valid shift out is detected. The duration of this OR pulse, termed tOPH, must be long enough to be used by the SI of the downstream FIFO (Y). Specifically,

$$t_{OPH} > t_{SIH(required)}\ [1].$$

This requirement is shown as a function of temperature in Figure 4.

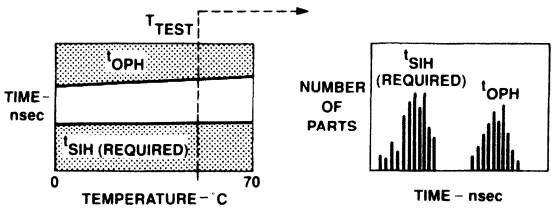


Figure 4. t_{OPH} vs. t_{SIH} at a Particular V_{CC}

The tOPH requirement is derived from histograms generated during the characterization of a broad sample of cascadable parts. The parts are tested individually at a variety of voltage and temperature conditions. AMD specifies its cascadable FIFOs with a reliable margin between the tOPH and tSIH histograms under each condition.

A short logic 1 pulse on SI will produce a short logic 0 pulse (tIPL) on IR. tIPL must be long enough to be recognized as a legitimate SO low pulse by the upstream part X. Thus,

$$t_{IPL} > t_{SOL(req)}\ [2].$$

There is a direct relationship between tSIH and tIPL. The requirements on tIPL from [2] are used to dictate the requirement on tSIH. The parameter tIPL is used only for characterization and internal testing and does not appear in AMD sheets.

Next, there is the need for SO and OR to be simultaneously at a logic 1 long enough for the FIFO to detect a valid shift out. This time requirement, which is not found in the datasheets is termed tSOHR(req), "time for SO to remain high after OR goes high." If IR, which drives SO, goes LOW too soon after a valid shift in is detected in Y, the tSOHR requirement in X may be violated. If so, no shift out will take place. Therefore,

$$t_{IRL} > t_{SOHR(req)}\ [3].$$

The parameter tSOHR is characterized and tested. It is normally small relative to tSOH.

The last requirement for Case 1 pertains to data set-up. When in the fallthrough mode, input data is taken as valid on the rising edge of SI. The set-up time for this data (tIDS) must be met. Note, however, that meeting this set-up time is the responsibility of the upstream part (X). When X brings its OR pin HIGH, it indicates that new data is present. The time from OR HIGH to new data valid is termed tORD. Because this rising edge commences a shift in for the downstream part, the following relationship must hold:

$$-t_{ORD} > t_{IDS(req)}\ [4].$$

In all AMD cascadable FIFOs, tIDS max is specified at zero, while tORD max in never specified greater than zero. By this convention, [4] is always satisfied. The validity of inequality [4], and others documented in this application note, are ensured via the method of separation of parametric distributions, as illustrated in Figure 4.

Case 2: Low-Frequency Bubbleback

The term "bubbleback" is a hangover from the register-based FIFOs. Bubbleback occurs when one or more devices in the composite buffer are full, and a word is clocked out of the most downstream one. A vacancy is created in this bottom FIFO, and is soon filled by the first FIFO upstream from it. The vacancy then "bubbles back" all the way to the most upstream FIFO. In the process, a data transfer is required each time the vacancy crosses a cascade interface, as was the case for fallthrough.

The following sequence describes this bubbleback action:

1. The user shifts data out of the most downstream FIFO.
2. Since this FIFO is no longer full, its IR pin goes HIGH.
3. The first FIFO upstream from it held its OR HIGH, because it was not empty.
4. The IR of the end FIFO is tied to SO of the FIFO above it. The rising edge on IR commences a shift out of the upstream FIFO.
5. Simultaneous shift cycles occur in both FIFOs. IR of the end FIFO goes LOW to acknowledge the valid shift in.
6. IR going LOW in the end FIFO resets the valid shift out of the upstream device. Since this upstream part is not empty, its OR pin returns HIGH.
7. Because this upstream part now contains a vacancy, it commences a shift out of the next higher part. This process continues until the vacancy reaches the *most upstream* device.

The timing diagram for the cascade interface is shown below.

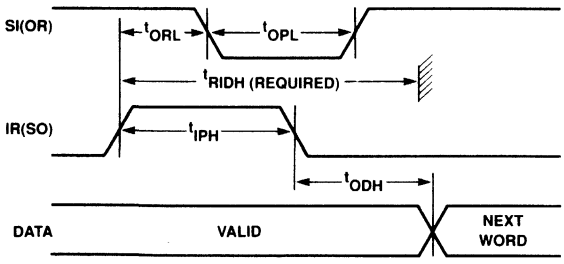


Figure 5. Low-Frequency Bubbleback

In bubbleback it is IR going HIGH which initiates the transfer of data. IR goes HIGH, then is quickly reset once a valid shift in is detected. This is analogous to the fallthrough case in which OR is pulsed HIGH. The first three bubbleback inequalities, then, are merely I/O duals of [1] through [3]:

$$t_{IPH} > t_{SOH(req)}\ [5],$$

$$t_{OPL} > t_{SIL(req)}\ [6],$$

$$t_{ORL} > t_{SIHR(req)}\ [7].$$

There is no data set-up requirement for low-frequency bubbleback since the next data word is present and waiting long before a vacancy arrives for it. This data must, however, satisfy a hold time requirement, as measured from the start of the valid shift in.

As seen in Figure 5, SO is brought LOW in the middle of the data transfer. Bringing SO LOW clears the upstream FIFO, causing its read pointer to advance. A new data word then begins its way toward the outputs. The current word being transferred eventually becomes "old" data, to be replaced by the next word. The time that the "old" data is held after SO goes LOW is called tODH.

The bubbleback hold time requirement (see Figure 5) can be expressed as:

$$t_{IPH} + t_{ODH} > t_{RIDH(req)}\ [8a].$$

The parameter tRIDH is the data hold time, relative to IR going HIGH. It is measured relative to IR because, in the bubbleback case, IR initiates the shifting-in of data.

Testing of [8a] is required to ensure cascadability in all outgoing parts. However, inequality [8a] mixes parameters from both the upstream (tODH) and the downstream (tIPH, tRIDH) parts. It is therefore necessary to rewrite [8a] so that it can be examined on individual parts:

$$[t_{IPH} - t_{RIDH(req)}] > -t_{ODH}\ [8b].$$

The quantity on the left hand side of the equation becomes a new characterization parameter, called t1. If there is a sufficient margin between the test histograms of t1 and tODH (as was the case for tOPH versus tSIH), then criterion [8a] will certainly be satisfied.

Case 3: Higher-Frequency Fallthrough

In Case 3, the frequency of operation becomes high enough such that the data transfer time is no longer negligible when compared to the time between arrivals of any two words. Still, the frequency is low enough such that the operation is clearly fallthrough, i.e., OR going HIGH initiates the transfer of data into a downstream part that is clearly waiting for new data.

The timing diagram for this case is shown in Figure 6.

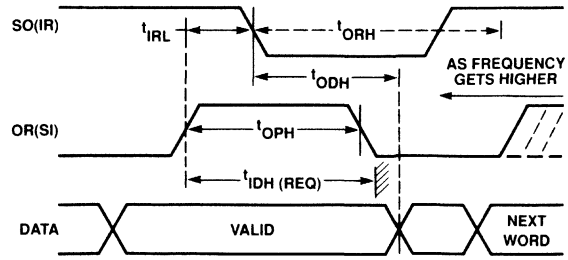


Figure 6. Higher-Frequency Fallthrough

Inequalities [1] through [4] from Case 1 still hold. One more must be added to account for the second rising edge of OR, which now occurs soon after the data transfer.

The falling edge on IR, which occurs after a valid shift in is detected, is seen by the upstream part as a falling edge on SO. This implies a read pointer advance, which could bring new data to the outputs. In the low-frequency case there was no new data to bring, so the current word remained valid for quite some time. At higher frequency, there *is* a new word to bring to the outputs, which reduces the time that the current data is

valid. There is the risk of a data hold time violation unless the following relationship is met:

$$t_{IRL} + t_{ODH} > t_{IDH(req)} \text{ [9]}.$$

The parameter t_{IDH} is the data hold time relative to SI going HIGH.

As the frequency of operation gets continually higher, the second rising edge of OR falls closer to that of IR. The limiting cycle time for true fallthrough, as depicted here, is tIRL + tORH, although this cycle time may not be obtainable due to limitations described in the section on natural frequency.

Case 4: Higher-Frequency Bubbleback

In Case 4 the time between creations of vacancies approaches the time required for data transfer. However, the frequency is assumed low enough such that the operation is clearly bubbleback, i.e., the rising edge of IR initiates a shift out of an upstream part which is clearly waiting with valid data.

The timing diagram for this case is seen below.

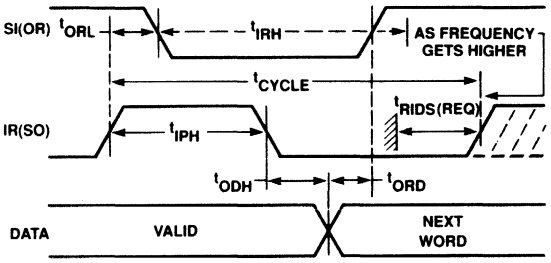


Figure 7. Higher-Frequency Bubbleback

Inequalities [5] through [8] from Case 2 are still pertinent. One more must be added to account for the rising edge of IR, which reappears soon after the data transfer.

As vacancies bubble back at ever increasing rates, there is the risk of violating the data set-up requirement as measured from the edge of IR. Specifically, the following relationship must hold:

$$t_{CYCLE} - t_{IPH} - t_{ODH} > t_{RIDS(req)} \text{ [10]}.$$

The parameter tRIDS is the set-up time relative to IR going HIGH, Inequality [10] tells us that if tCYCLE gets too short, there may be a data set-up violation. As seen in Figure 7, so long as we remain in bubbleback mode, with IR coming high after SI, we will have tIPH + tODH + |tORD| < tCYCLE, implying tCYCLE-tIPH-tODH > |tORD|. However, AMD designs its cascadable devices such that tRIDS(req) < 0, and tORD < 0, thereby ensuring that there is no set-up violation.

As the frequency of operation gets continually higher, the second rising edge of IR falls closer to that of OR. The limiting cycle time for true bubbleback, as defined here, is tORL + tIRH, although this cycle time may not be obtainable, as discussed in the next section.

Case 5: Natural Frequency

As mentioned previously, the user has no control over the handshake operations at the cascade interfaces. If the user shifts words into a relatively empty buffer at low frequency, the cascade interfaces will operate in the fallthrough mode (Case 1). If the user shifts words out of a relatively full buffer at low frequency, then the interfaces will be forced to operate in bubbleback mode (Case 2). For continuous operation at moderately high rates, the interface timing will begin to resemble one of the next two (3 and 4) cases.

As the frequency is increased further, the interface timing may no longer be clearly bubbleback or clearly fallthrough. This is what occurs as the throughput rate approaches the *natural frequency* of the cascade interface. This natural frequency is the maximum frequency at which the handshake signals can negotiate part-to-part data transfers. Consider Figure 8.

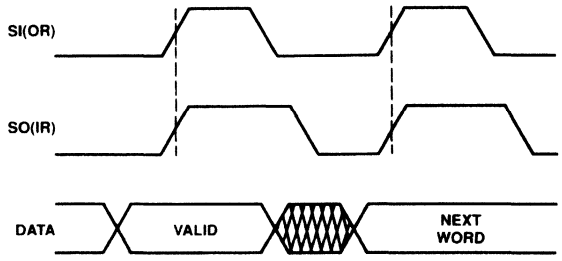


Figure 8. Zero-Phase Incidence

Figure 8 illustrates a perfectly legitimate handshake operation. There is clearly a shift in (SI*IR=1) and a shift out (SO*OR=1), implying a transfer of data. However, none of the previous cases directly apply since it is neither a fallthrough nor a bubbleback case.

In the fallthrough mode SO was clearly high before OR, while IR went high clearly before SI. Thus, SO had *positive phase* relative to OR, while SI had *negative phase*. Likewise, the bubbleback mode has negative phase for SO and positive phase for SI. The relative phases of the SI and SO signals have important implications for the cascading parameters at high frequencies. As explained later, the natural frequency of cascading must be guaranteed higher than the maximum throughput rate applied to the cascaded FIFO system. Predicting and measuring the natural frequency poses some difficulties, as explained below.

The fallthrough parameters tIRL, tOPH, tIDS, etc., are all characterized at positive SO, negative SI phase, whereas the bubbleback parameters tORL, tIPH, tRIDH, etc., are all characterized at positive SI, negative SO phase. When the relative phases approach zero from either side (Figure 8), the meaning of these parameters becomes ambiguous. Take for example the parameter "time from valid shift in (SI*IR=1) to IR going low." For positive phases this quantity approaches the tIPH asymptote, while for negative phases it approaches the tIRL asymptote. When the phase is near zero, this quantity lies somewhere in between, as shown in Figure 9.

As indicated on the graph, a new name is required for this pseudo-parameter. It will be known here as tVSIRL, or "time from valid shift in to IR low." Similar graphs can be generated for

the pseudo-parameter called tVSORL, as well as for t(R)IDS and t(R)IDH. This sort of graphical information is useful when analyzing operating characteristics at or near the natural frequency. At this point there are two approaches one can take to predicting the natural frequency:

1) Take an iterative approach to determine the minimum working values of phase (ϕ), tVSIRL(ϕ), tVSORL(ϕ), t(R)IDS(ϕ), etc., using two figures, 10 and 11.

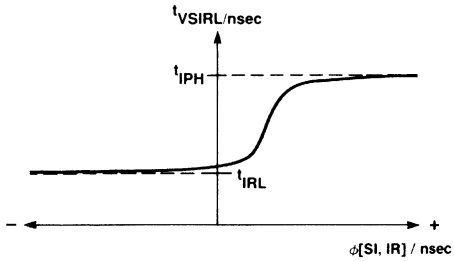


Figure 9. t_{VSIRL} as a Function of Phase

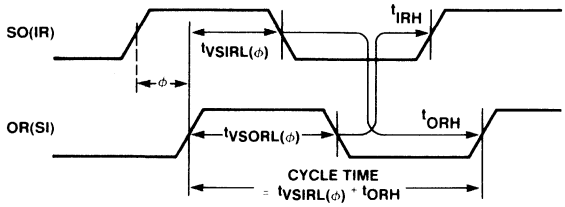


Figure 10. Positive SO/OR Phase at Natural Frequency

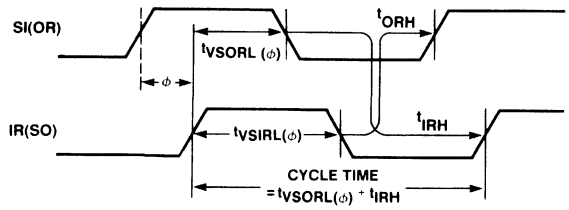


Figure 11. Positive SI/IR Phase at Natural Frequency

One needs to determine which of the two cases (Figures 10, 11) has a lower maximum frequency. In equation form:

$$1/f_{MAX} = \max\{t_{VSIRL}(\emptyset)+t_{ORH},\ t_{VSORL}(\emptyset)+t_{IRH}\}\ [11]$$

2) Approach (1) provides the exact value of the natural frequency, but only after a considerable amount of iteration. There exists a simpler approach to the problem, based upon the results of Cases 3 and 4. This approach yields a conservative estimate of the natural frequency, such that if the composite buffer is operated at or below this frequency, cascadability can be guaranteed.

Figure 6 depicts fallthrough operation based on the assumption that tIRL + tORH is clearly greater than tOPH + tIRH. If this is not the case, then the second rising edge of OR could possibly occur before the second rising edge of IR. Then, the parameter tOPH is no longer valid, and should be replaced by the more applicable tORL. However, tORL pertains to cases where SO arrives substantially after OR. If the rising edges of IR and OR are close to one another, then the applicable value may lie somewhere inbetween tORL and tOPH. To be safe, merely take the greater of these two values.

The same reasoning applies for the breakdown of the fundamental assumption of Case 4. The following is a simple worst-case expression for fMAX at each operating condition:

$$1/f_{MAX(wc)} = \max\{t_{VSIRL(max)}+t_{ORH}, t_{VSORL(max)}+t_{IRH}\}\ [12a],$$

where:

$$t_{VSIRL(max)}=\max\{t_{IRL}, t_{IPH}\}\ [12b],$$

$$t_{VSORL(max)}=\max\{t_{ORL}, t_{OPH}\}\ [12c].$$

Note that using the results of Cases 3 and 4 produced equation [12] which bears great resemblance to the more accurate expression in [11]. One strategy for dealing with cascadability is to design a FIFO with "flat" tVSIRL, tVSORL, t(R)IDS, etc., characteristics. This eliminates the dependence on signal phase, and fMAX can be expressed exactly as:

$$1/f_{MAX} = \max\{t_{IRL}+t_{ORH}, t_{ORL}+t_{IRH}\}\ [13].$$

Such a strategy provides a more reliable cascade interface, and is well worth the price of a lower fMAX.

It should be noted that the natural frequency at each operating condition (VCC, temperature) is unique, and is the limiting frequency regardless of how it is approached, whether by fallthrough or by bubbleback. Consider the following figure.

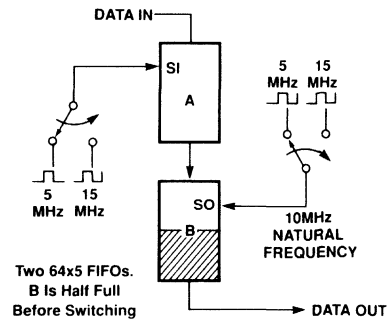


Figure 12. Approach of f_{MAX} from Fallthrough

Let us say that the natural frequency of the cascade interface between A and B is 10 MHz. Data is shifted at low frequency into A, and falls through to B, until B is one-half full. The two-device buffer is then operated for a while with the input, output, and interface working at 5 MHz.

Then, the input and output frequencies are raised to, say, 15 MHz. Immediately thereafter, the composite buffer will continue to function, since the input and output circuitry of a FIFO

can usually operate at frequencies above the natural frequency. The cascade interface, however, will be limited to a rate of 10 MHz. Eventually, the bottom part will empty, and the top part will fill. A cascade limited bottleneck occurs, limiting the overall throughput rate to 10 MHz. Data words from the 15 MHz input stream will be intermittently read at a 10 MHz rate, causing a loss of data.

At some point in time between the frequency increase and the bottlenecking, there will be five or so words in the top part, and twenty-seven or so (half of 64, minus 5) words in the bottom part. The FIFOs will no longer be in fallthrough mode, since there is more than one word in the upstream part, and more than one vacancy in the downstream part. The natural frequency mode will have been entered, and the interface will carry data as fast as possible.

A similar example can be drawn for these FIFOs, with the composite buffer initially three-fourths filled. Eventually, the top part will fill and the bottom part will empty. At some point in between, the FIFOs will no longer be in bubbleback mode, but in the natural frequency mode, because there will exist more than one vacancy in the downstream part and more than one word in the upstream part. The overall steady state throughput rate will again be limited to 10 MHz.

In each of the above cases, the composite buffer went from either fallthrough or bubbleback mode to the natural frequency mode (where both parts were neither full nor empty), then on to an interface limited natural frequency mode, subject to throughput-related errors.

Regardless from which direction the natural frequency was approached, this frequency must be unique since it represents the case where the upstream part contains more than one word and where the downstream part contains more than one vacancy. When this happens the interface has no dependence on what is happening at the system input and output ports and shifts data across it at the maximum possible rate.

The maximum operating frequency of a cascaded FIFO must therefore be specified lower than the worst-case natural frequency in order to avoid asynchronously induced bottleneck errors.

FIFO RAM controller tackles deep data buffering

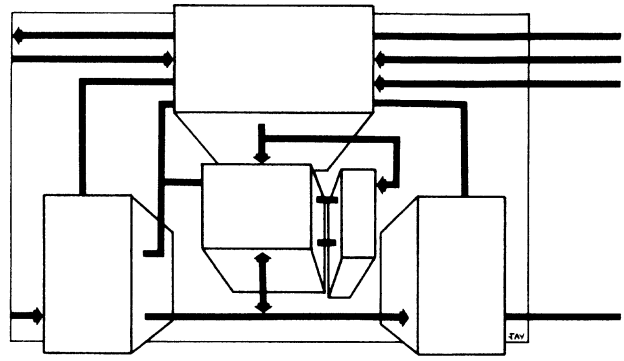
Buffering large amounts of data has long been a source of design headaches. Extra large FIFO buffers minimize system bottlenecks with an implementation as easy as it is cost-effective.

Designers are turning to innovative architectures to extend the performance of computer systems. Pipelining is one of these innovations. In pipeline architectures, data is buffered temporarily between a system's processing elements. This allows these processing elements to work more efficiently. Since data transfers can occur asynchronously, designers can minimize bottlenecks in data paths and boost overall performance.

Data buffering, however, is sometimes difficult and costly to implement. In multiprocessing and data communications applications, for example, designers encounter the problem of how to buffer large blocks of sequential data temporarily with minimum cost and trouble. Often, a few thousand to tens of thousands of words must be buffered.

In multiprocessing applications, large blocks of data and instructions are passed between the various processors. Storing information between the processors for a short time lets a sender pass data on without waiting for a receiver to finish its current task, so the sender can more quickly move on to its next task.

For data communications applications, large blocks of data must be transferred from one node to another along a data channel. Temporary buffering on and off the data channel permits each



device in the network to work more efficiently. Data can be transferred to the buffer when ready, and the device is free to move on to the next task without waiting for the data channel to be free.

Buffering large amounts of data, often called deep data buffering, can be accomplished through several methods. One technique, direct memory access (DMA), sets aside blocks of main memory as temporary data buffers. When a request for data transfer is received, the DMA controller interrupts the processor and takes control of the memory bus. The controller then moves the data into memory that has been allocated for temporary buffering.

Looking at the advantages of this buffering method, DMA controller chips are relatively inexpensive. Since they require little extra logic, the controllers are simple to implement. The DMA.approach, however, has several drawbacks. First, the processor is interrupted every time a data block

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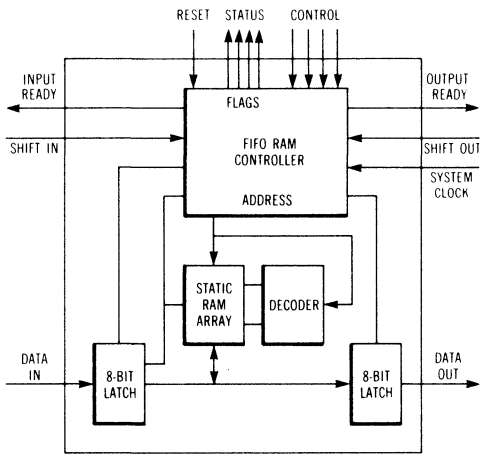


A FIFO RAM controller provides addressing, control and arbitration. In the 674219 buffer, only handshaking, status flags and buffer control lines are visible to the rest of the system.

transfer request is made. To transfer data, the processor must hand over control of the memory bus. When many data block transfers occur, system performance is severely degraded. Large blocks of data degrade performance even more.

DMA also limits rates and formats of data. Using this technique, the maximum data rate is limited to the system bus data rate. Bursts of rapid data can't be directly accommodated. Besides, DMA operation is synchronous with system operation, which means that all data transfers—both input and output—must be synchronous with the system clock. Asynchronous data can't be directly accommodated. Another drawback of DMA is that it doesn't allow for simultaneous input and output operation. This greatly limits the ability of a DMA buffer to act as a pipelining element.

The DMA approach is best suited for systems in which low cost is a top priority, and performance degradation, caused by interruptions to processors during the transfer of data, is tolerable. In effect, designers opting for DMA trade overall system performance, considerations about the rate and format of data and immediate access to information for inexpensive implementation and simple design.

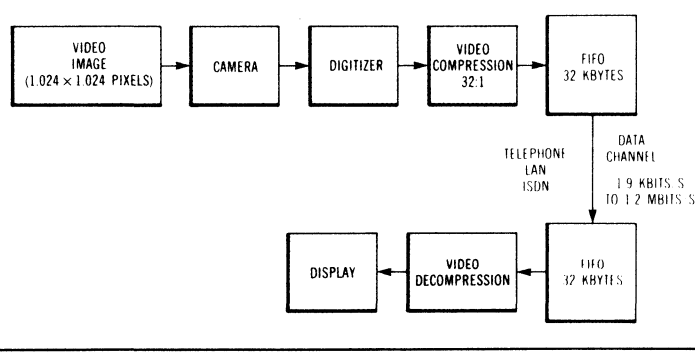
RAM approach eases bottlenecks

Another approach to deep data buffering involves dual-port RAM devices. A dual-port RAM is placed along the data transfer path and acts as temporary storage for incoming or outgoing data. These devices overcome many of the limitations of DMA. Thanks to two independent ports, data transfers can be completely asynchronous and simultaneous. Since one port can be isolated from the data bus, processors don't have to hand over control of the memory bus during data transfer.

Using dual-port RAMs for data buffering does have its disadvantages; to work as a data buffer, it requires a lot of external and control logic. Counters, comparators and control logic must be added to make the dual-port RAM read and write data sequentially and prevent buffer overflows and underflows from occurring. This external logic can add up to large amounts of valuable board real estate and limits the data rate of the buffer.

Another disadvantage is cost. Dual-port RAMs are 10 times the price of comparable conventional static RAMs; a 1-k × 8-bit device costs $25 to $30. Implementing a 4-k × 16-bit buffer will cost approximately $200 for the RAM device alone.

A third method of buffering data uses first-in, first-out buffers between elements as temporary storage sites. These FIFO devices store and output the data sequentially. Like dual-port RAMs, they



In a video teleconferencing system, a video image with a resolution of 1,024 × 1,024 pixels will generate 1 Mbyte of data per image. After a compression of 32:1, there are 32 kbytes of compressed data for each image. For optimal system performance, the data is passed to a FIFO buffer to wait for transmission along the data channel. The system is then free to begin processing the next image.

have two independent asynchronous ports. But one port is dedicated to input, the other to output.

FIFO buffers offer an extremely efficient approach for data buffering. Virtually no external control is required since control and arbitration is performed with on-chip logic. Addressing is eliminated because data is sequential. The streamlined buffering afforded by FIFOs maximizes the data rate, which makes this approach a natural for high-performance systems.

For maximum data rate and design ease, FIFO buffers offer advantages over DMA and dual-port RAM methods. But the devices are geared for data buffering of shallow-to-medium depth. Large data blocks are buffered only by using an array of FIFOs, which requires large amounts of board space, making FIFO buffers too expensive and inefficient for applications with large data amounts.

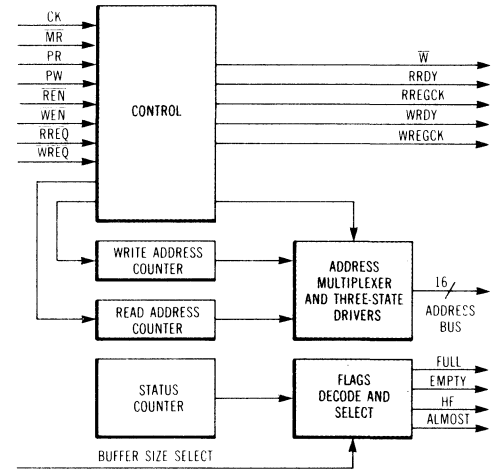
FIFO RAM controllers tackle deep data

When deep buffering is required, very large FIFO RAM buffers reduce the costs and space problems of conventional FIFO techniques. Devices such as the 674219 FIFO RAM controller can accommodate large amounts of data in high-performance systems. These devices provide the addressing, control, and arbitration logic that enables an array of RAMs to function as a FIFO buffer.

One advantage of this kind of device is the large amount of data it can handle. Using inexpensive single-port static RAMs (or dynamic RAMs with additional external logic), designers can implement a fast, fully asynchronous buffer that can temporarily store from 512 to 65,536 words. In the case of the 674219 FIFO RAM controller, a performance of 12 MHz can be attained. During simultaneous input and output operation, a data rate of 6 MHz is possible.

With two registers for data latching, a few logic gates and a RAM array, these devices can replace any system function block calling for large data buffers. All of the control, arbitration and status logic is placed on a single device, greatly simplifying large FIFO buffer designs. Information about the buffer is provided by four status flags: full, empty, half-full and almost-full/almost-empty. The full and empty flags buffer overflow and underflow. When the buffer is full, attempts to write data into the buffer won't be acknowledged. Data already in the buffer, however, won't be lost. Similarly, the empty flag prevents false data from being read out.

Status flags also help increase the efficiency of buffers and optimize system performance. Together, the half-full and almost flags can indicate when the buffer is almost empty and trigger a signal to the source for more data. This ensures a steady stream of data to the receiver. In systems where a receiver, such as a peripheral, is operating at a much slower rate than the source, such as a processor, the processor can send data in high-speed bursts to the buffer and then attend to other tasks while a peripheral accepts the data in a steady, uninterrupted stream.



Two internal counters generate addresses for the RAM array to function in a first-in, first-out manner. A third counter in the FIFO RAM controller generates status information with four flags: full, empty, half-full and almost-full (16 word locations to full)/almost-empty (only 16 words remaining). This counter is programmed by buffer-size select inputs to provide the proper status information for the buffer.

Dual-pointer FIFO architecture

FIFO RAM controllers implement a RAM-based FIFO architecture, which uses two pointers. The write pointer contains the address of the next available location in the RAM array to be written and the read pointer has the address of the next location for data to be read. When either pointer is used to access the memory array, it's incremented automatically to point to the next available location. When the pointer reaches the last location, it's reset to zero and the procedure continues.

A third counter provides status information, generates flag logic and prevents overflow and underflow. The -size select inputs program this counter to give the proper status information to the buffer.

In the cycle of a typical system, the buffer is reset with the Master Reset (MR) pin. This sets the read and write pointers to zero and activates the empty flag. A write cycle is initiated by a Write Request (WREQ). The Write Ready (WRDY) line goes low, acknowledging the request. A Write Register Clock (WREGCK) pulse from the FIFO RAM controller latches the data into the write register. Data is then written to the RAM array at the address location provided by the write pointer. When the buffer has valid data, the empty flag will go low, indicating that a read can take place. The read cycle follows the same sequence as the write cycle.

Since a FIFO RAM controller uses low-cost, single-port RAMs, arbitration is needed to resolve simultaneous read and write requests. On-chip arbitration logic determines which request is serviced first. The second request is acknowledged, but will not be serviced until the first request is completed.

Conventional FIFO buffers are based on shift registers. Data is shifted from register to register to the top of the stack, and then to the output port. The time it takes for a word to move from the input port to the output port is called "fall-through," and it is dependent on the depth of the FIFO buffer.

By contrast, FIFO RAM controllers implement a RAM-based buffer. In this scheme, pointers are incremented as each read or write occurs. Since data doesn't physically move, fall-through time is eliminated. What's more, external control of the RAM array buffer is possible by disabling both the Write Enable (WEN) and the Read Enable (REN) to impose three states on the address lines from the FIFO RAM controller to the RAMs.

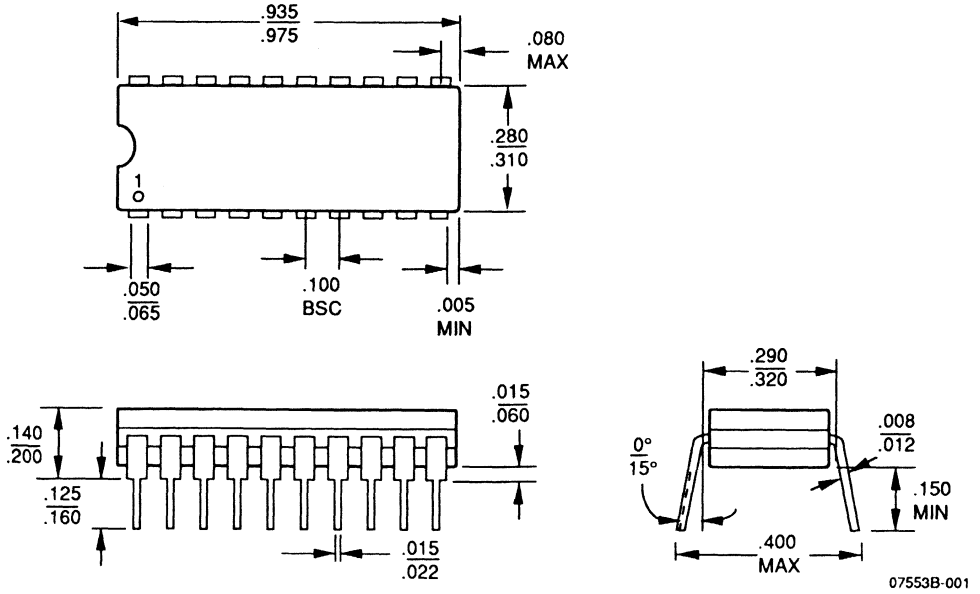
By reducing the cost and space requirements of FIFO buffering, FIFO RAM controllers offer systems designers an efficient and cost-effective method to buffer large amounts of data. Using these devices, designers can minimize system bottlenecks in data paths and processing elements and can boost overall system performance. **CD**

SECTION 7
Physical Dimensions*

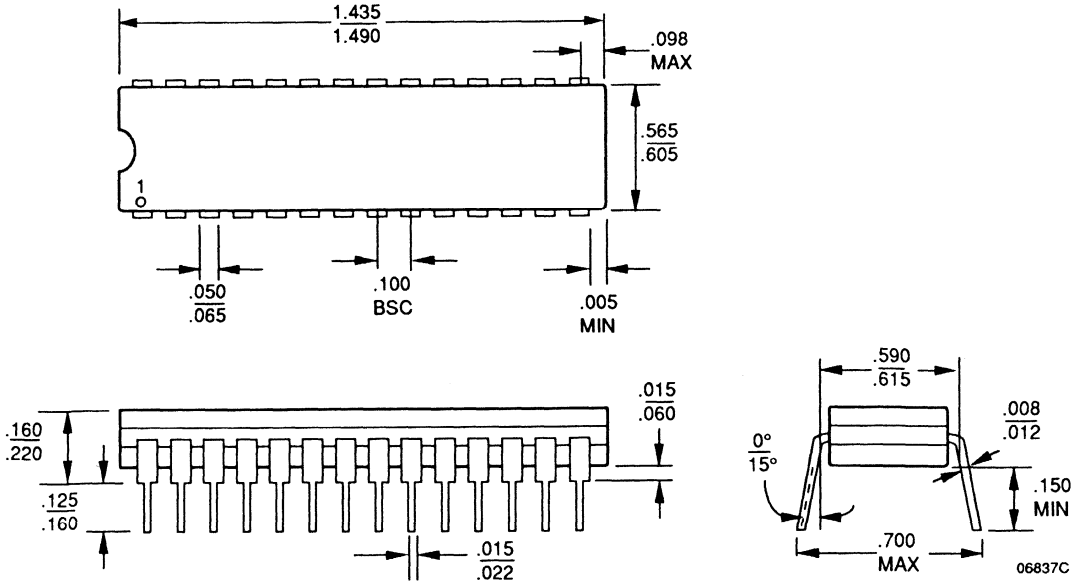
CD 020	20-Pin Ceramic DIP
CD 028	28-Pin Ceramic DIP
CD 032	32-Pin Ceramic DIP
CD 040	40-Pin Ceramic DIP
CD4028	28-Pin 400-mil, Ceramic DIP
CDV028	28-Pin View Ceramic DIP
CDV032	32-Pin View Ceramic DIP
CDV040	40-Pin View Ceramic DIP
CLR032	32-Pin Rectangular Ceramic Leadless Chip Carrier
CLV032	32-Pin View Rectangular Ceramic Leadless Chip Carrier
CLV044	44-Pin View Square Ceramic Leadless Chip Carrier
PD 020	20-Pin Plastic DIP
PD 028	28-Pin Plastic DIP
PD 032	32-Pin Plastic DIP
PD 040	40-Pin Plastic DIP
PD3028	28-Pin 300-mil, Plastic DIP
PDW028	28-Pin Wide 300-mil, Plastic DIP
PL 020	20-Pin Square Plastic Leaded Chip Carrier
PL 032	32-Pin Rectangular Plastic Leaded Chip Carrier
PL 044	44-Pin Square Plastic Leaded Chip Carrier

* For reference only. All measurements are in inches unless otherwise specified. BSC is an ANSI standard for Basic Space Centering.

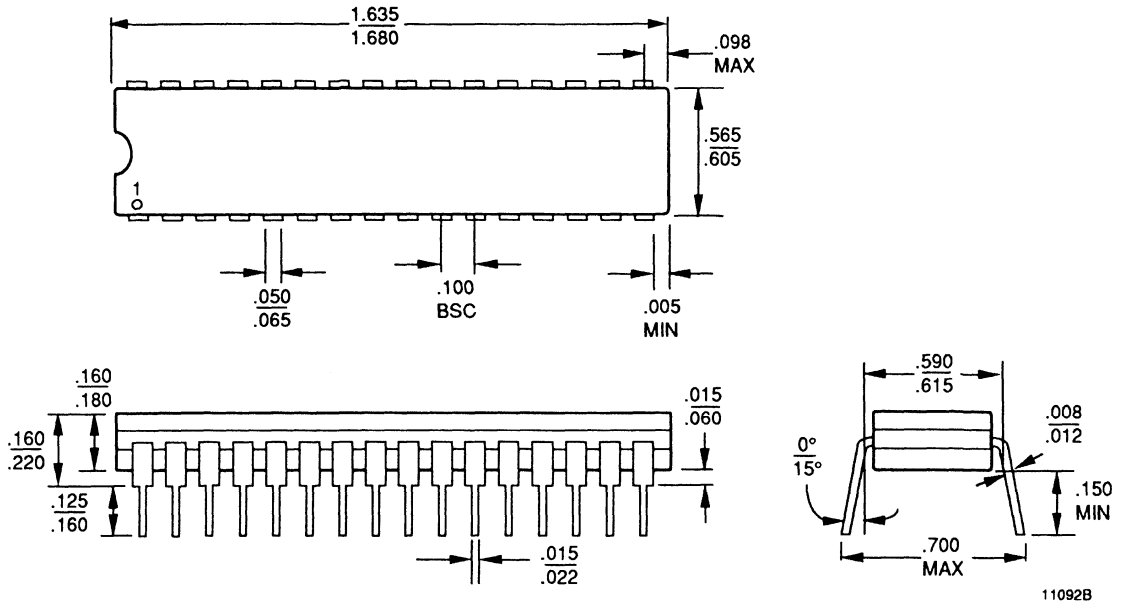
CD 020
20-Pin Ceramic DIP



CD 028
28-Pin Ceramic DIP

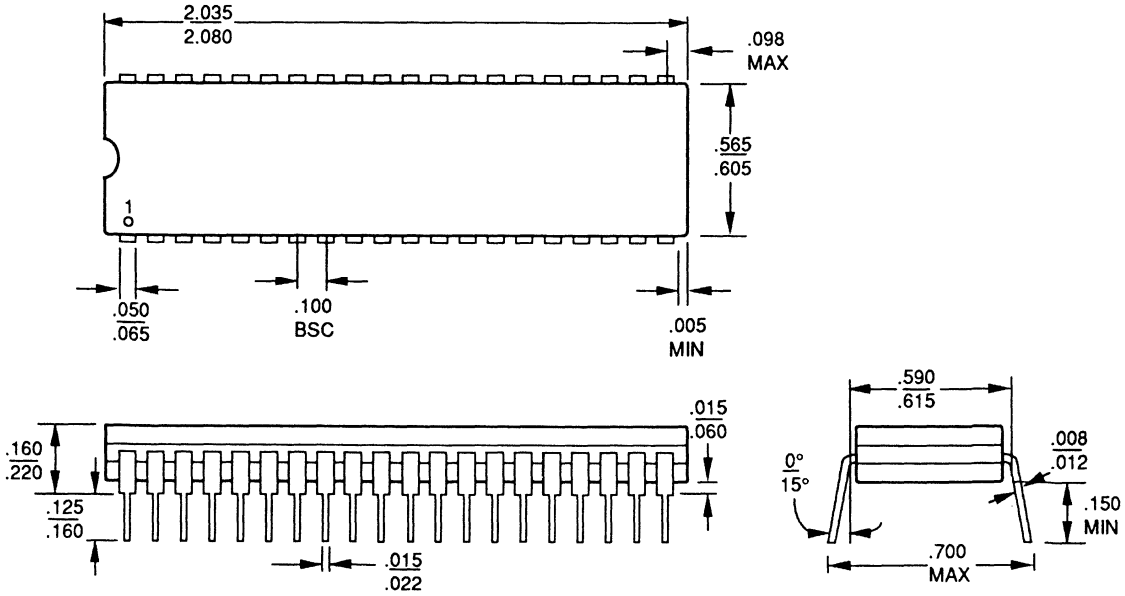


CD 032
32-Pin Ceramic DIP



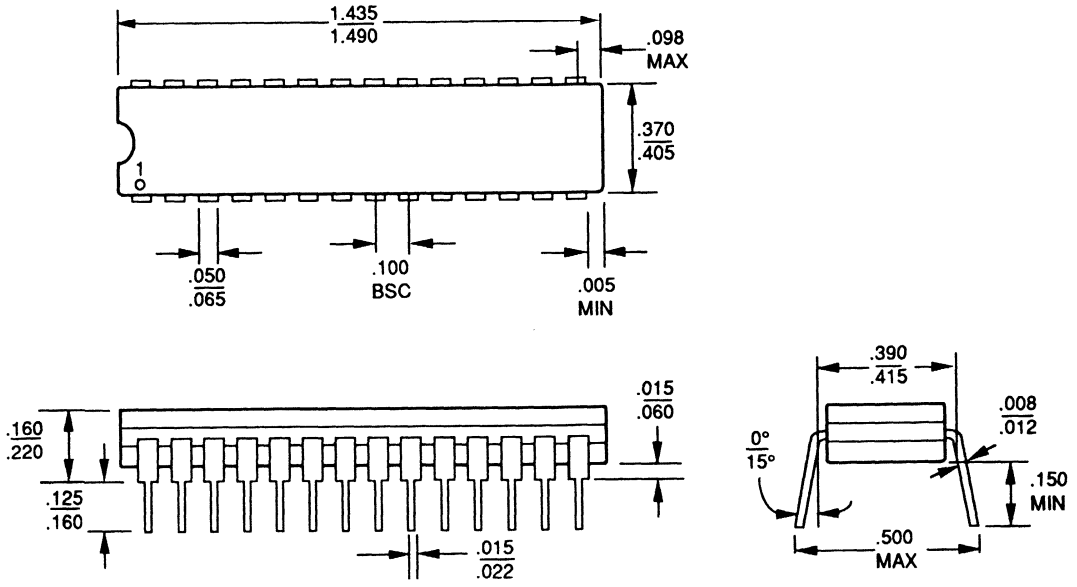
11092B
BK 13
2/25/91 CD

CD 040
40-Pin Ceramic DIP



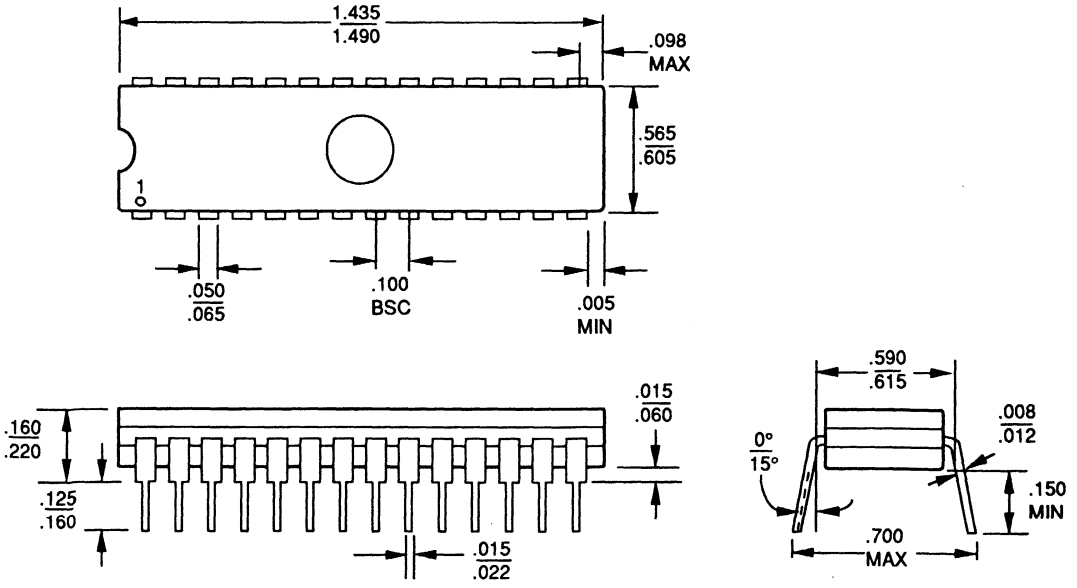
06824C

CD4028
28-Pin, 400-mil, Ceramic DIP



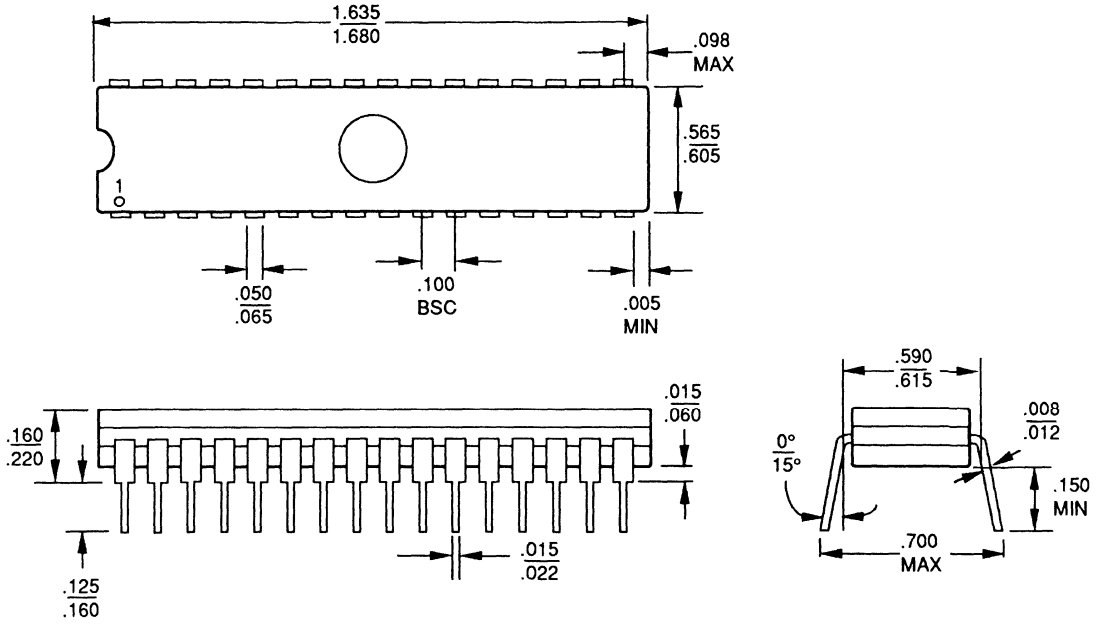
06837C

CDV028
28-Pin View Ceramic DIP



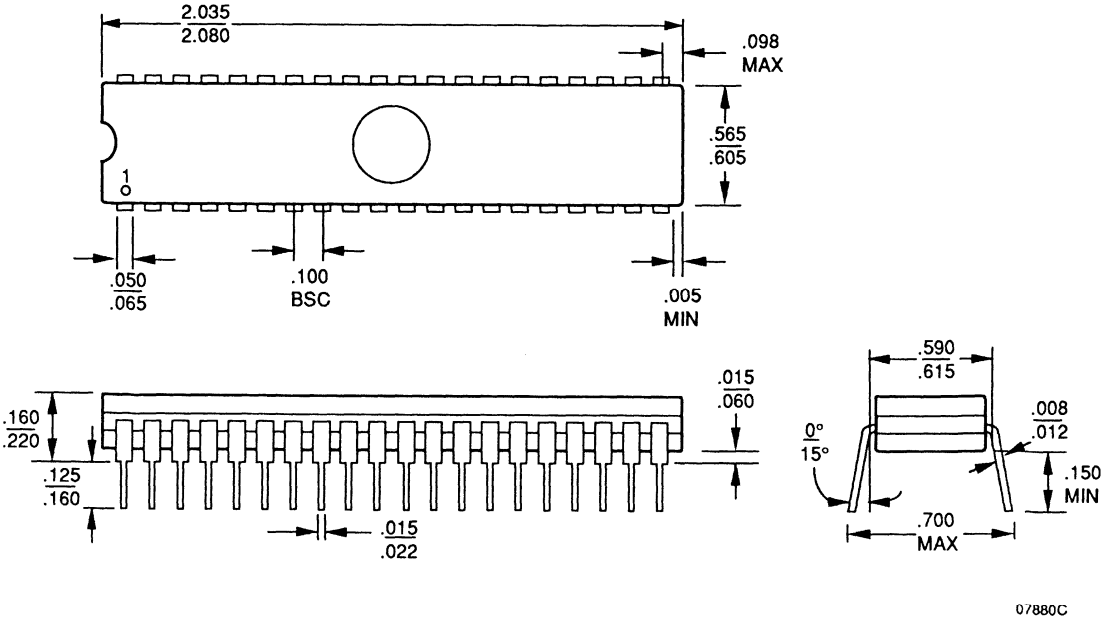
08267B

CDV032
32-Pin View Ceramic DIP



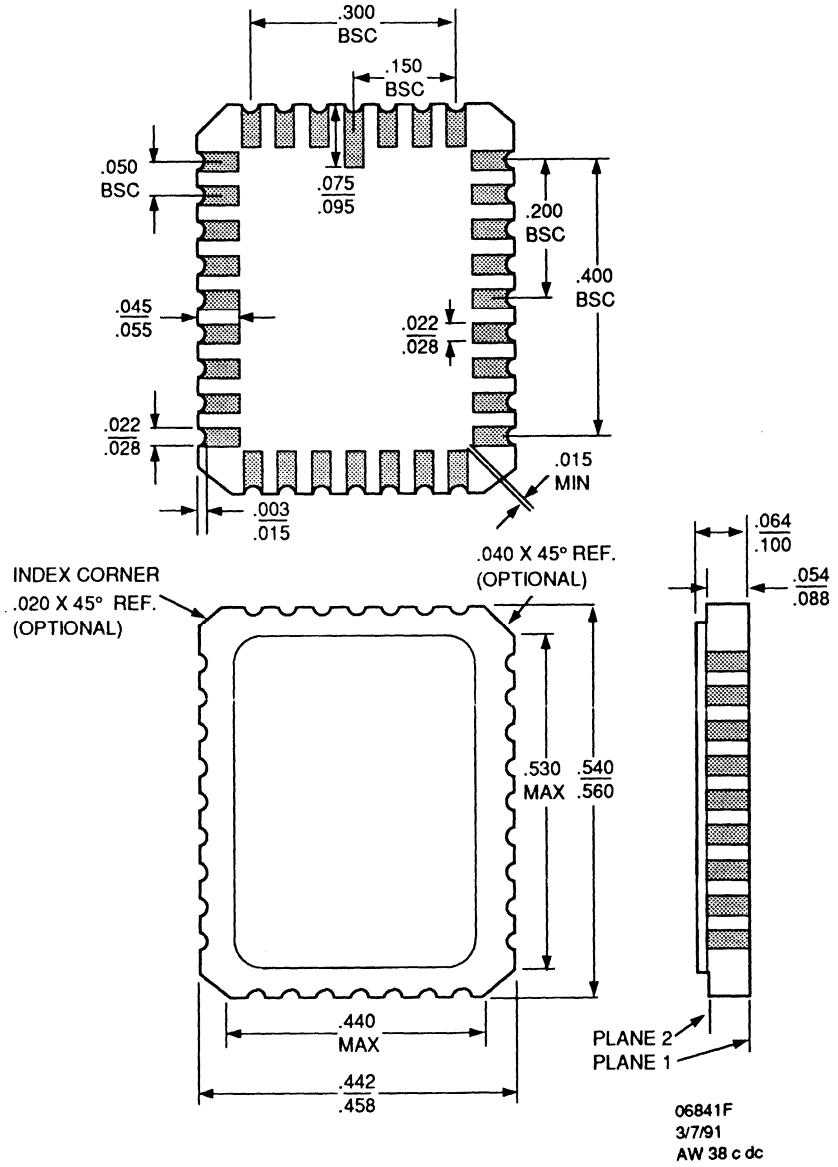
11092A

CDV040
40-Pin View Ceramic DIP

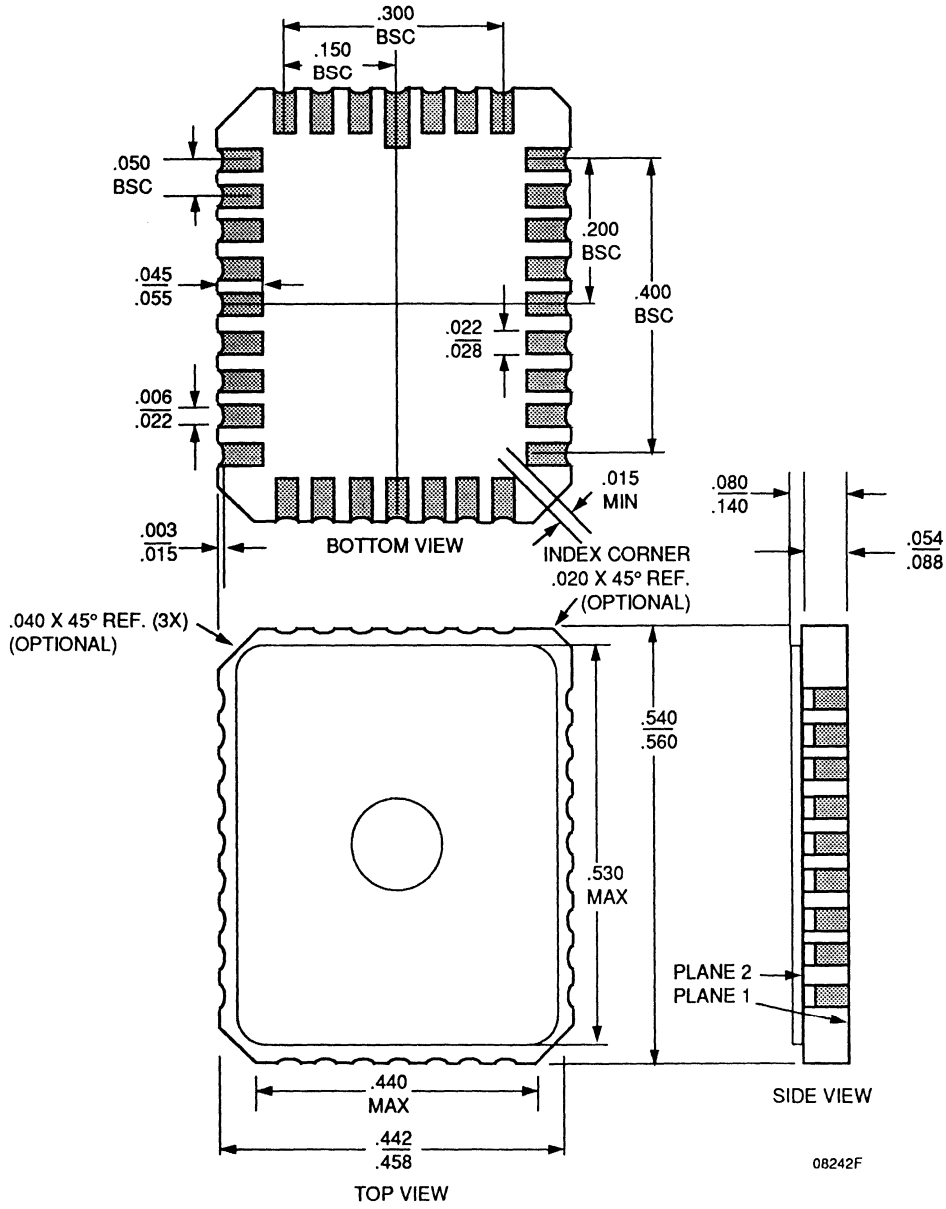


07880C

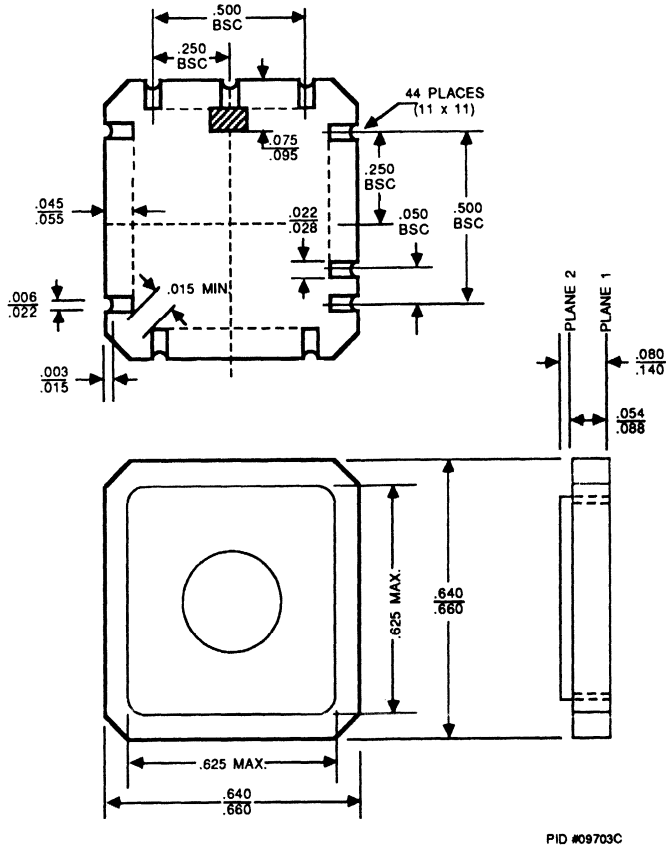
CLR032
32-Pin Rectangular Ceramic Leadless Chip Carrier



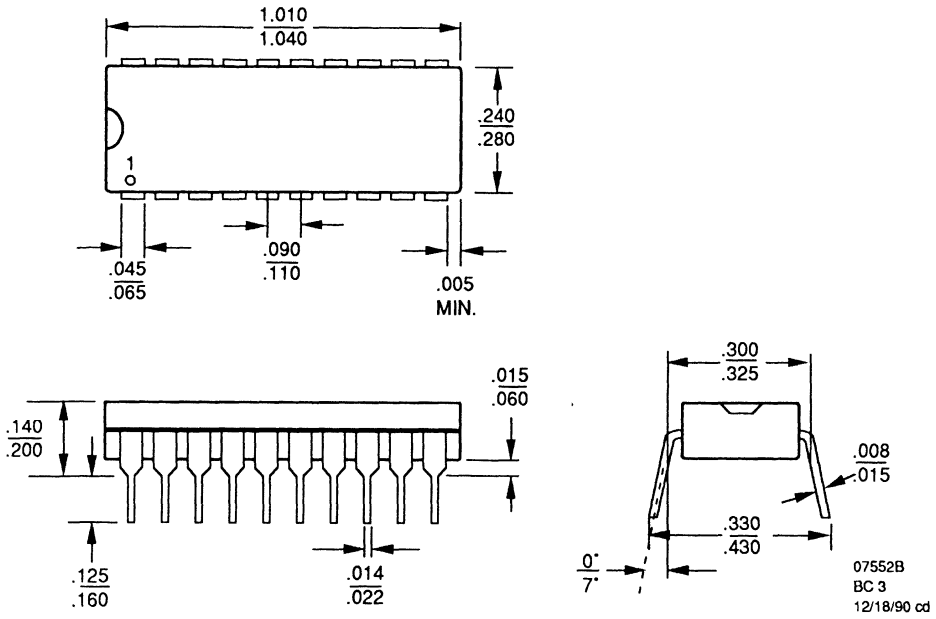
CLV032
32-Pin View Rectangular Ceramic Leadless Chip Carrier



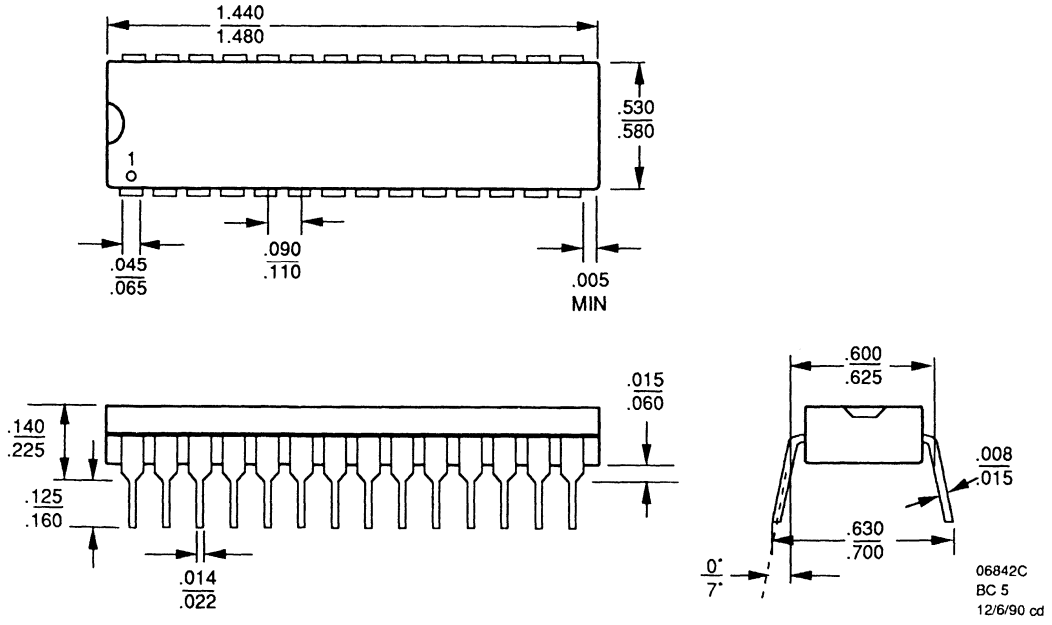
CLV044
44-Pin View Square Ceramic Leadless Chip Carrier



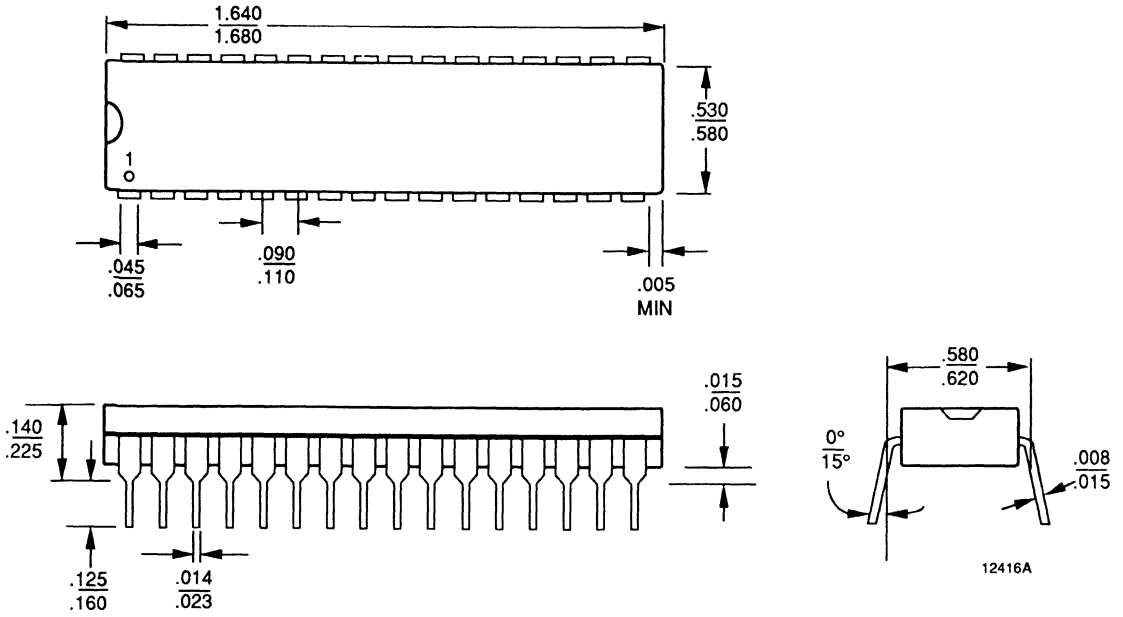
PD 020
20-Pin Plastic DIP



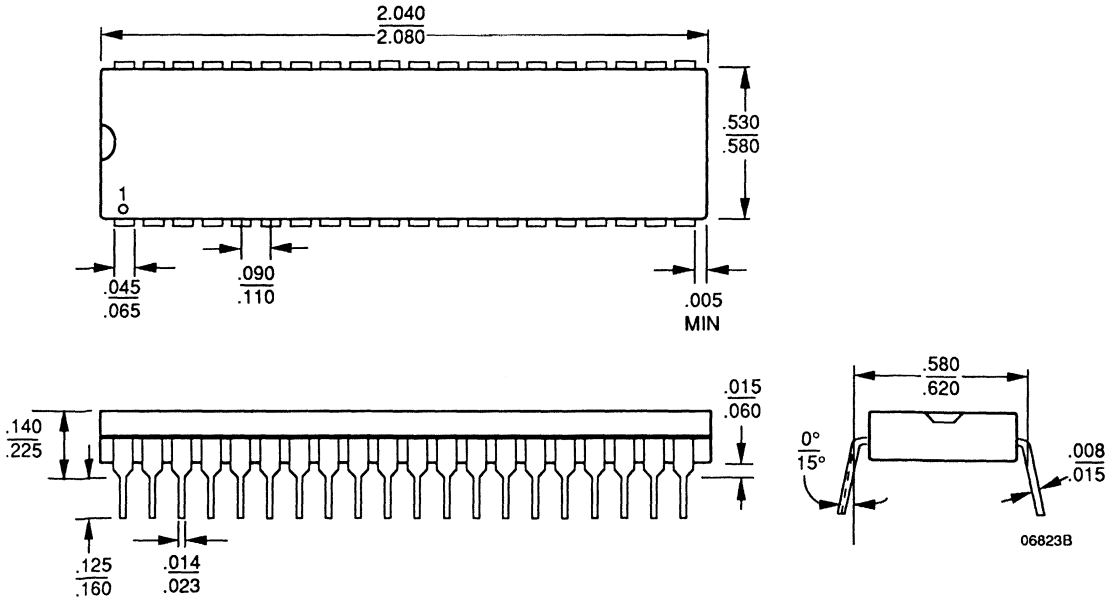
PD 028
28-Pin Plastic DIP



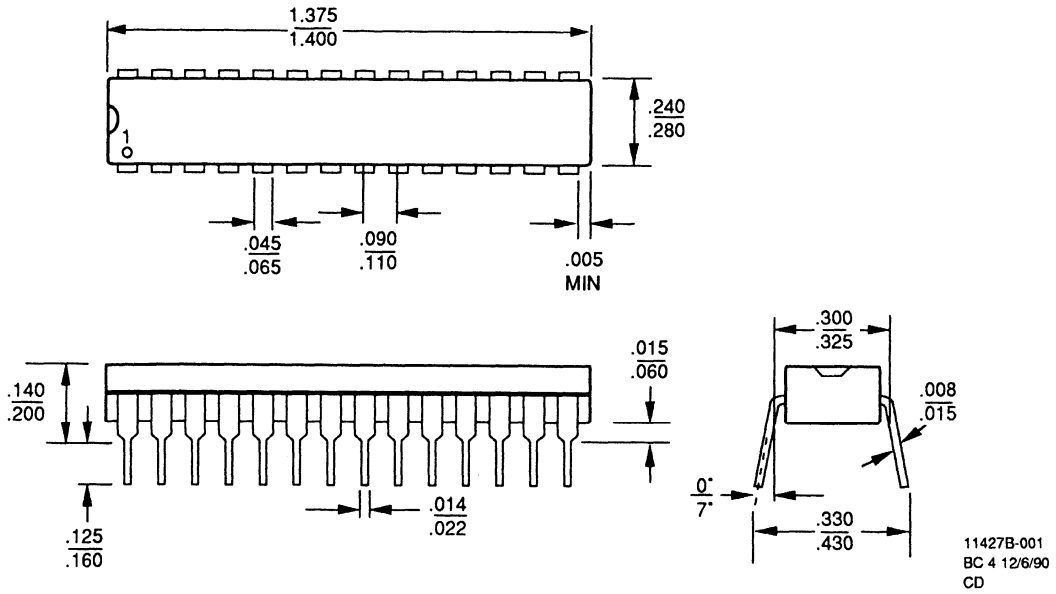
PD 032
32-Pin Plastic DIP



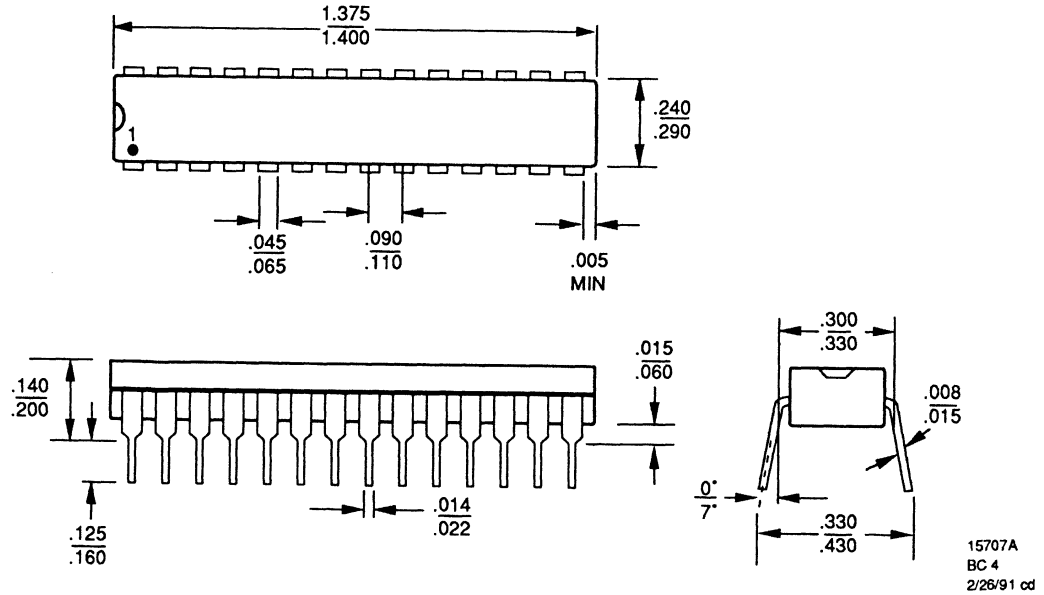
PD 040
40-Pin Plastic DIP



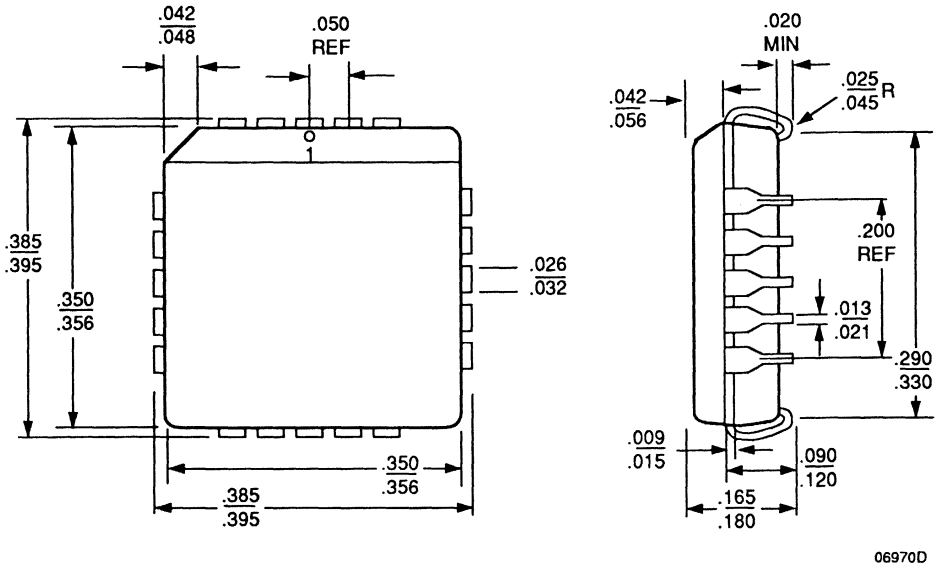
PD3028
28-Pin, 300-mil, Plastic DIP



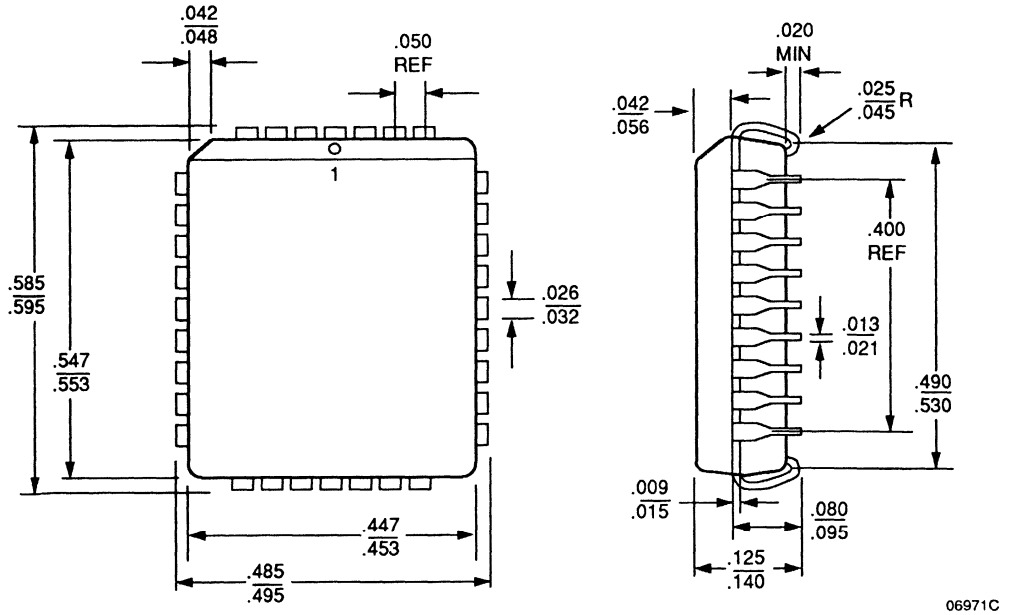
PDW028
28-Pin, Wide 300-mil, Plastic DIP



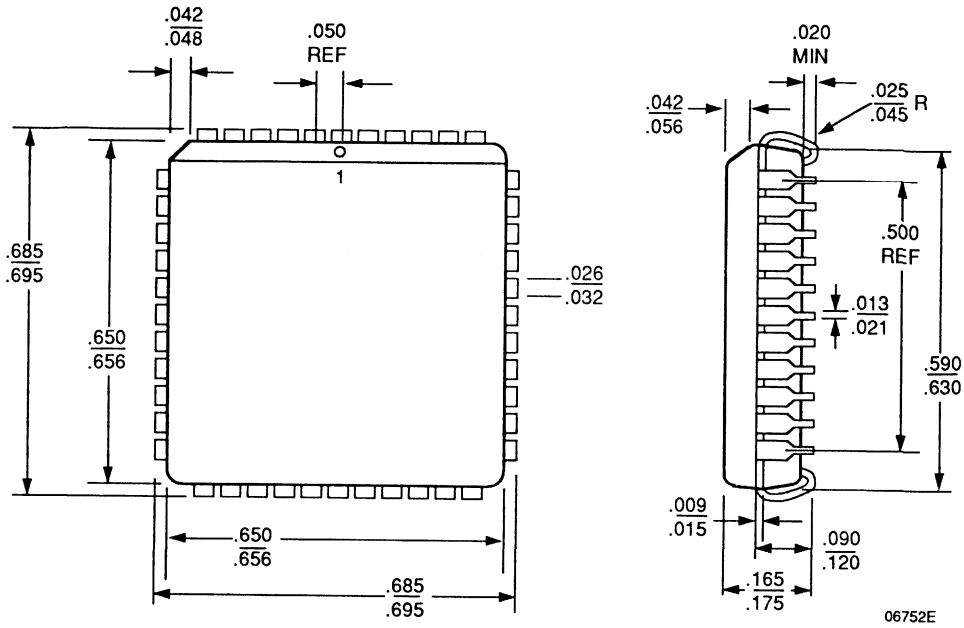
PL 020
20-Pin Square Plastic Leaded Chip Carrier



PL 032
32-Pin Rectangular Plastic Leaded Chip Carrier



PL 044
44-Pin Square Plastic Leaded Chip Carrier



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